



## Research paper

## Design and characterization of a 200 V, 45 A all-GaN HEMT-based power module



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## HIGHLIGHTS

- This work proposes the design, development, and testing of all-GaN power module.
- We develop module package and determine their thermal and electrical properties.
- ID-VDS characteristics are obtained over a wide range of base plate temperatures.
- Self-heating in GaN HEMTs is studied by electrical analysis and IR thermography.

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## ABSTRACT

Emerging gallium nitride (GaN)-based high electron mobility transistor (HEMT) technology has the potential to make lower loss and higher power switching characteristics than those made using traditional silicon (Si) components. This work designed, developed, and tested an all-GaN-based power module. In a 200 V, 45 A module, each switching element comprises three GaN chips in parallel, each of which includes six 2.1 A AlGaIn/GaN-on-Si HEMT cells. The cells are wire-bonded in parallel to scale up the power rating. Static  $I_D$ - $V_{DS}$  characteristics of the module are experimentally obtained over widely varying base plate temperatures, and a low on-state resistance is obtained at an elevated temperature of 125 °C. The fabricated module has a blocking voltage exceeding 200 V at a reverse-leakage current density below 1 mA/mm. Two standard temperature measurements are made to provide a simple means of determining mean cell temperature in the module. Self-heating in AlGaIn/GaN HEMTs is studied by electrical analysis and infrared thermography. Electrical analysis provides fast temperature overviews while infrared thermography reveals temperature behavior in selected active regions. The current distribution among cells was acceptable over the measured operating temperature range. The characterization of electrical performance and mechanical performance confirm the potential use of the packaged module for high-power applications.

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## 1. Introduction

The AlGaIn/GaN high electron mobility transistor (HEMT) is an important state-of-the-art technology for achieving a high breakdown voltage, a wide bandgap, a high power density and a high switching frequency [1,2]. The GaN is now one of the wide bandgap materials used in advanced power electronic devices. The high breakdown field of GaN ( $3.5\text{--}5 \times 10^6$  V/cm) compared to Si ( $0.3 \times 10^6$  V/cm) is attractive because it enables GaN-based devices to operate at high voltages and low leakage currents. The high electron mobility ( $2000 \text{ cm}^2/\text{V}\cdot\text{s}$ ) and electron saturation velocity

( $2.5 \times 10^7$  cm/s) also enable high frequency operation. Because of the close match between its thermal coefficient of expansion and that of insulating ceramics, its reasonable electron mobility, and a thermal conductivity value that does not differ much from that of Si [3,4]. However, although various studies of the power characteristics of GaN HEMTs have considered their performance on-wafer load-pull level, none has considered the effects of practical assembly and packaging [5–9]. Since high power densities substantially increase temperature in the transistor channel, accurate estimates and measurements of junction temperatures are essential for designing power modules. Recently, the enhanced material properties of silicon carbide (SiC) have been exploited to improve the performance of high-power electronic device modules over those of GaN components [10–14]. Although the quality and size of GaN wafers have rapidly improved, some devices that use such

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wafers have inherent material defects, especially when operated in parallel at high power. The processes used to manufacture high quality GaN substrates, *i.e.*, substrates with few defects, are also still in their early stages and are much less mature than those for manufacturing SiC. To evaluate the potential use of GaN technology in high power applications, a power module with multiple parallel GaN HEMT cells is needed. The thermal management requirements and the current distribution during switching affect the operation of the GaN power module and the switch utilization factor of parallel switches. The positive temperature coefficients of GaN switches facilitate current sharing during conduction. This work fabricated a GaN power module with a high current rating by connecting multiple GaN power HEMTs in parallel.

## 2. Fabrication process and structure of AlGaIn/GaN HEMT device

The AlGaIn/GaN heterostructure pattern is formed by metal organic chemical vapor deposition (MOCVD) on a 625  $\mu\text{m}$ -thick silicon substrate. To improve process control, the growth rate, layer thickness, and surface roughness are optically monitored in real time by *in situ* pyrometry to support the molecular beam epitaxial growth of GaN on the Si (111) substrate. Fig. 1 presents the regularly stacked cross-section of the fabricated AlGaIn/GaN HEMT structure. A 4  $\mu\text{m}$ -thick GaN buffer layer, a 25 nm-thick  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$  barrier layer and, finally, a 4 nm-thick GaN capping layer were deposited on the epitaxial structure, which comprised a 120 nm-thick AlN spacer layer. The device was isolated using inductively coupled plasma reactive ion etching (ICP-RIE) with  $\text{Cl}_2$ -based gas. Source and drain Ohmic contacts were formed by evaporating the Ti/Al/Ni/Au (20 nm/120 nm/25 nm/5100 nm) multi-layers and then annealing in a nitrogen atmosphere at 800  $^\circ\text{C}$  for 60 s. An ohmic contact resistance of  $3 \times 10^{-6} \Omega \text{cm}^2$  was obtained by TLM method. The surface of the GaN capping layer used as the main dielectric coating was passivated by low-pressure chemical vapor deposition (LPCVD) of a 50 nm-thick  $\text{Si}_3\text{N}_4$  layer. In the two-step process for defining the gate, a U-groove was etched to penetrate the LPCVD  $\text{Si}_3\text{N}_4$  layer. Schottky contacts were formed from Ni/Au (20 nm/150 nm) multi-layers. The surface was again passivated with a second 100 nm-thick  $\text{Si}_3\text{N}_4$  layer, which was grown by plasma-enhanced chemical vapor deposition (PECVD) at 300  $^\circ\text{C}$  [15]. Source-terminated field plates were deposited to improve the electric field distribution on the drain side near the gate edge to increase the breakdown voltage and to reduce current collapse. The field plate was connected to the source electrode and extended 4  $\mu\text{m}$  over and away from the gate-to-drain region. The source-to-

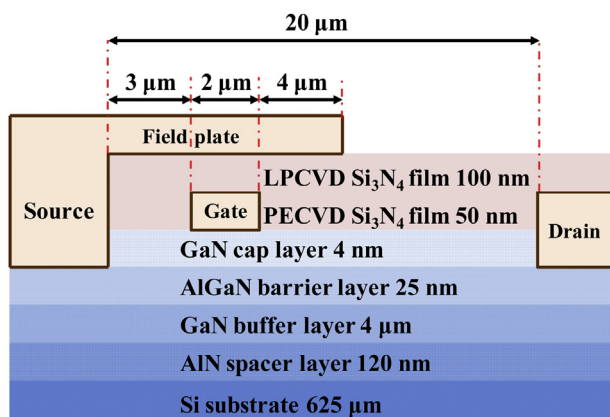


Fig. 1. Cross-section of AlGaIn/GaN HEMT with source field plate structure.

gate distance and channel length between the source and drain were 3  $\mu\text{m}$  and 20  $\mu\text{m}$ , respectively [16,17]. Finally, a 6  $\mu\text{m}$ -thick Au plating process was used to fabricate an air-bridge connecting the two sides of the electrode fingers.

Fig. 2 presents the AlGaIn/GaN HEMT structure comprising Ohmic and Schottky contacts formed by periodically arranging multiple metal fingers. The upper gate structure (gate fingers and interconnects) partially overlap the source structure. The plated air-bridge gate interconnects connect the adjacent gate fingers of the transistor array through bridges that cross over the source and drain fingers. The studied device layout includes 60 gate fingers (6 cell; gate length, 2  $\mu\text{m}$ ; gate width, 500  $\mu\text{m}$ ), and the total width of the gate periphery is 30 mm. The active device area is 0.25  $\text{mm}^2$  with a 50  $\mu\text{m}$  pitch separating adjacent gate fingers and includes source and drain contact regions.

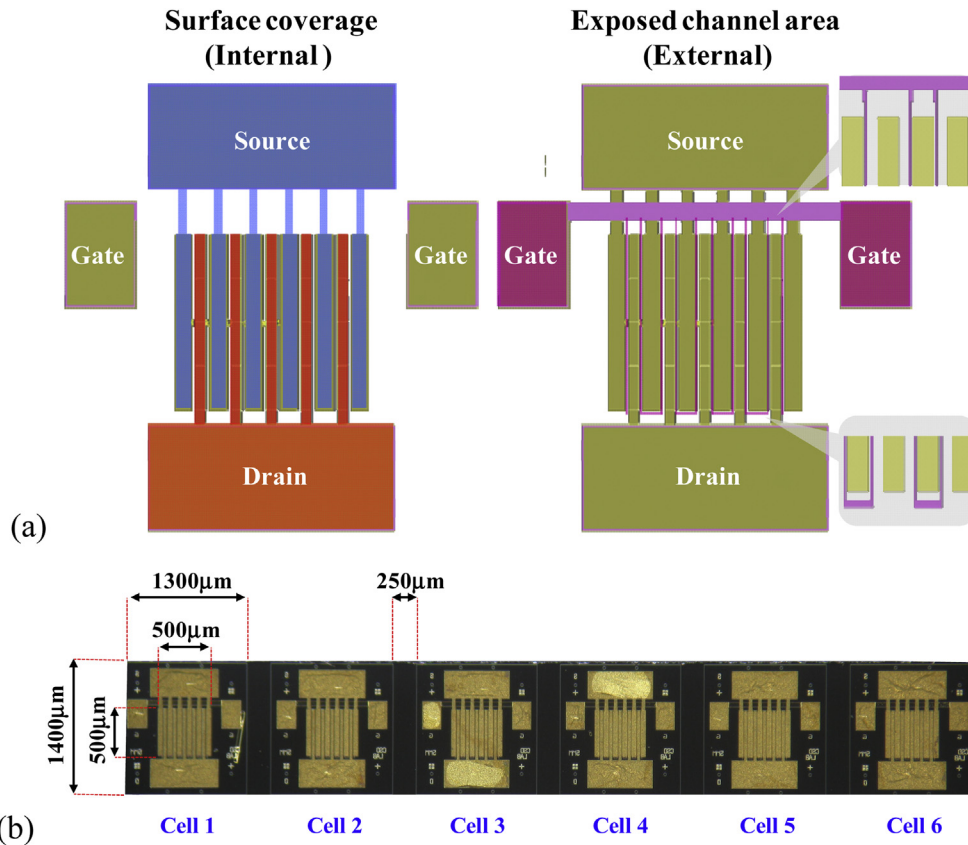
## 3. Multiple-chip gallium nitride power module packaging

### 3.1. GaN power module design

This work elucidates the packaging and thermal management of numerous GaN HEMTs devices connected in parallel. Fig. 3 shows a photograph and schematic diagram of the multiple-chip GaN power module. Owing to the high material and processing costs associated with GaN HEMT devices, GaN-based devices have low yield, and few dies can fit on the wafer compared to silicon-based devices. Therefore, multiple small devices are usually connected in parallel in a power module [18]. Such a module must use a GaN multiple-chip array packaging and layout design to ensure high-power and highly efficient operation. The module packaging design must meet satisfy requirements for parallel interconnection among modules, high current handling capability and low on-state resistance. Fig. 3(b) shows that each module contains an array of 12 GaN HEMT devices arranged in four rows of three devices. Half of the six cells in each device are connected in parallel to form a switch with a high current rating. In the power module, the substrate layout comprises four switch combinations, C1–C4, which constitutes the full-bridge switching circuit. The four switch combinations form two bridge arms: one formed from C1 and C2 and one formed from C3 and C4. This method reduces the size of the module and increases the feasibility of connecting modules in parallel.

### 3.2. Fabrication and assembly of process module

Module packaging and assembly is simplified by applying the module concept used in a standard Insulated Gate Bipolar Transistor (IGBT) (rated 600 V, 75 A) package. Fig. 4 displays the substrates, chip-on-board assemblies and package housing selected for the GaN power module. The GaN HEMT devices are attached to an etched direct bond copper (DBC) aluminum nitride (AlN) substrate. To provide sufficient heat removal capacity, ceramics with a high thermal conductivity (230 W/mK) and high coefficients of thermal expansion (CTE) comparable to those of silicon are used. The circuit is laid out to optimize both the chip arrangement and the electrical interconnect (wire bonding layout and location of auxiliary contact). The power modules are packaged using advanced wire bond interconnection technology, and multiple wire bonds are used to obtain low-induction interconnects. The gold wires have a diameter of 30–50  $\mu\text{m}$  to provide the required current carrying capacity and the required size of the bond pad. Silver sintering-bonding is used to attach two wire-bond assemblies to a stainless steel flat base (heat spreader). Finally, the plastic casing is glued to the DBC substrates, and a silicone gel is coated on the module to provide electrical insulation and physical protection [19].



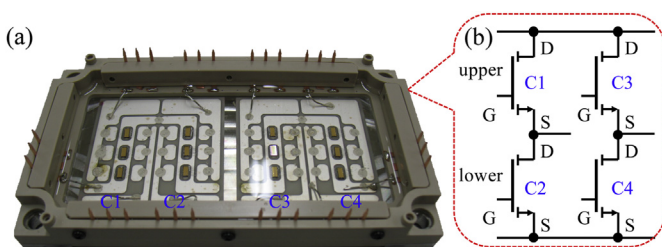
**Fig. 2.** Photograph and schematic diagram of the HEMTs. (a) Photograph of ten-finger HEMT with air-bridge gate interconnection. (b) Overall die size is  $1400 \mu\text{m} \times 1300 \mu\text{m}$  (six cells)  $\times 0.625 \text{ mm}$  (thickness).

### 3.3. Performance testing and evaluation

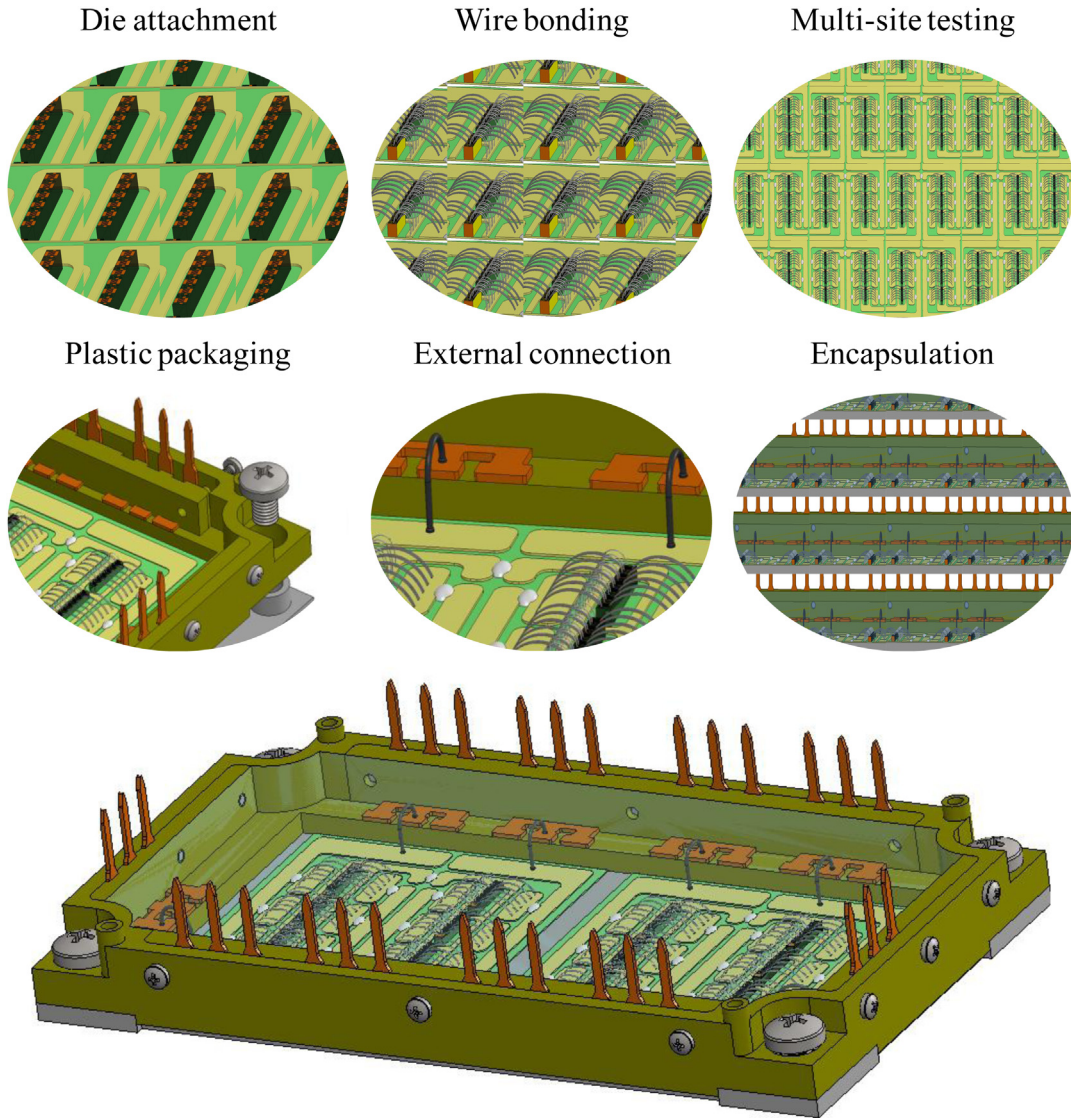
During fabrication of a multiple-chip GaN power module incorporating 36 GaN HEMT cells, six cells became inoperable, which left 30 cells available for use in the module. Preliminary electrical testing showed that eight cells were degraded. Hence, only the test results for a multiple-chip module with 22 GaN HEMT cells are reported. The static electrical characteristics of the prototype module were measured as functions of base plate temperature. Fig. 5 plots the current–voltage ( $I_D - V_{DS}$ ) characteristics of the 12 parallel GaN HEMT devices at  $25^\circ\text{C}$  and  $125^\circ\text{C}$  [20–22]. The measurements were made using a double-channel source meter by pulsing the gate–source voltage ( $V_{GS}$ ) at 100 Hz with a duty cycle of 0.1%. This gate pulse width and duty cycle supported  $I_D - V_{DS}$  measurement with negligible trapping and thermal effects. The  $I_D - V_{DS}$  characteristics were obtained at  $V_{GS}$  from  $-4 \text{ V}$  to  $1 \text{ V}$  in

steps of  $1 \text{ V}$ . As expected, the drain current ( $I_D$ ) through the GaN HEMT devices declined as the base plate temperature increased. Analysis of the static electrical characteristics of the assembled prototype module revealed a low on-state resistance and a high static current capacity of  $45.5 \text{ A}$  at  $25^\circ\text{C}$  and  $31.1 \text{ A}$  at  $125^\circ\text{C}$ . The positive temperature coefficient facilitates the use of these cells in parallel and reduces their overall on-resistance. The shared current must be highly uniform in all cells to prevent an excessive current from overloading the cells. To obtain a uniform distribution of current among all-GaN HEMT cells, all electrical properties, including on-resistance, threshold voltage, and leakage currents, were matched as closely as possible [23,24]. The module remained stable under forward bias with no significant change in characteristics, and the base plate maintained the temperature range of the module at  $25^\circ\text{C} - 125^\circ\text{C}$ .

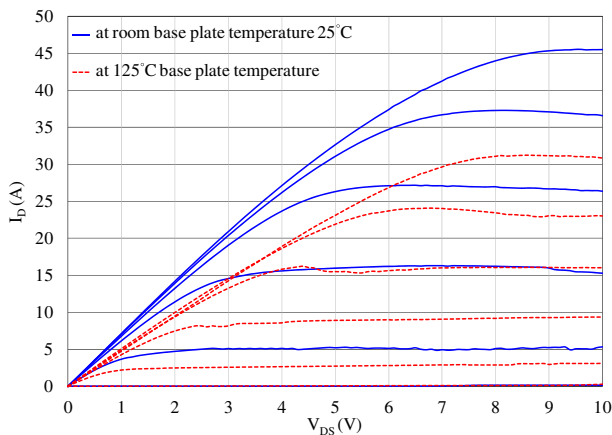
In a switching operation, the GaN HEMT transistors alternate between the on-state, in which the gate opens the channel and allows the current flow, and the off-state, in which the gate closes the channel and blocks the current flow. Efficient power switching is associated with operation at a high off-state blocking voltage and with leakage current below the specified limit. The breakdown voltage, which is measured with a curve tracer, is defined as the voltage at which the leakage current reaches  $1 \text{ mA/mm}$  with the gate biased below the threshold voltage. Fig. 6 plots the off-state leakage current as a function of drain-to-source voltage ( $V_{DS}$ ) under a  $V_{GS}$  of  $-4 \text{ V}$ . As  $V_{DS}$  was swept forward from  $0 \text{ V}$  to  $200 \text{ V}$ , the maximum voltage at which leakage was limited to  $1 \text{ mA/mm}$  increased steadily [25]. The drain ( $I_D$ ) and gate ( $I_G$ ) leakage current densities in the pulsed-mode reached as low as  $278 \text{ nA/mm}$  and  $306 \text{ nA/mm}$  at  $200 \text{ V}$ , respectively, which were three orders of



**Fig. 3.** Development of multiple-chip GaN power module. (a) Photograph of prototype high power density package based on all-GaN-based power devices. (b) Circuit diagram of power module.



**Fig. 4.** Module packaging and assembly procedures. (a) Silver-sintering die-attach on the gold-coated DBC substrate. (b) Wire-bond interconnection installed as needed. (c) Electrical testing. (d) Electronic module housing and assembly with integrated heat sink. (e) External pin connection. (f) Silicone gel encapsulation (potting).



**Fig. 5.** Each static  $I_D - V_{DS}$  curve is plotted ( $V_{GS}$  from  $-4$  V to 1 V) at base plate temperatures from room-temperature ( $25^\circ\text{C}$ ) to  $125^\circ\text{C}$ .

magnitude lower than the maximum on-state current. However, the GaN power devices had high gate leakage currents resulting from their surface states, which included dislocations in the buffer layer and plasma-induced etch damage [26]. The tested prototype GaN power module had a high current carrying capacity and a maximum blocking voltage exceeding 200 V.

#### 4. Thermal management in GaN HEMTs

Infrared (IR) imaging and electrical test method were used to analyze temperature increases caused by self-heating in the GaN power module. Local temperature distributions in the power module were measured by IR thermography; however, the spatial resolution of IR analysis is only  $\mu\text{m}$  to mm, depending on the equipment used [27–29]. Electrical test method is typically used to measure mean channel temperature in the active area of the module [30–32]. Therefore, combining both methods can rapidly identify hot spots and accurately determine temperature in a multiple-chip GaN power module.

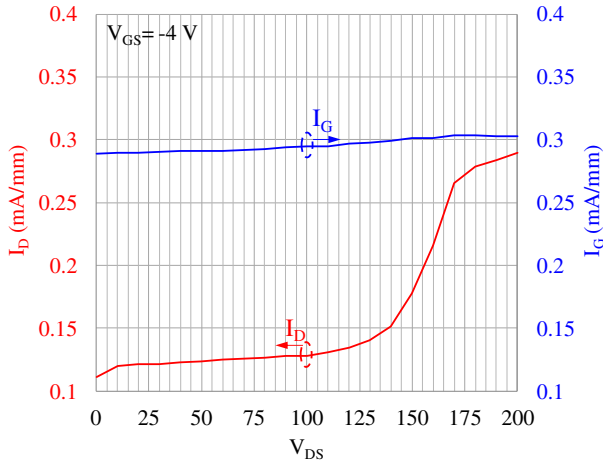


Fig. 6. Three-terminal off-state breakdown characteristics of GaN power module at  $V_{GS} = -4$  V. For  $V_{DS} < 200$  V, the leakage current density is less than the pre-specified benchmark of 1 mA/mm.

4.1. Infrared thermal measurements of surface temperature

Thermal infrared (IR) measurements can determine junction-to-case (package) temperature differentials, which can then be used to calculate the thermal resistance of the package. Thermal IR microscopy performed using a liquid nitrogen-cooled  $256 \times 256$  indium–antimonide (InSb) focal plane array can detect wavelengths from 3 to 5  $\mu\text{m}$ . To perform an IR measurement, the multiple devices under test (DUT) on the AlN substrates are held in the test fixture mounted on top of a temperature-controlled stage. To ensure effective heat dissipation, the air gaps are filled with thin layers of thermal grease to reduce the thermal contact/interfacial resistance. Finally, a sensor thermocouple is attached to monitor substrate temperature. The IR detector and the embedded thermocouple are calibrated against each other.

The interior of the GaN power module was sprayed with a thin coating of boron nitride (BN) to ensure that the emissivity of the component surface was in infrared wavelengths detectable by the IR detector [33]. Each device switch was biased at a gate voltage ( $V_{GS}$ ) of 0 V. Power dissipation from 1 W to 10 W per cell was determined by multiplying the drain currents by their

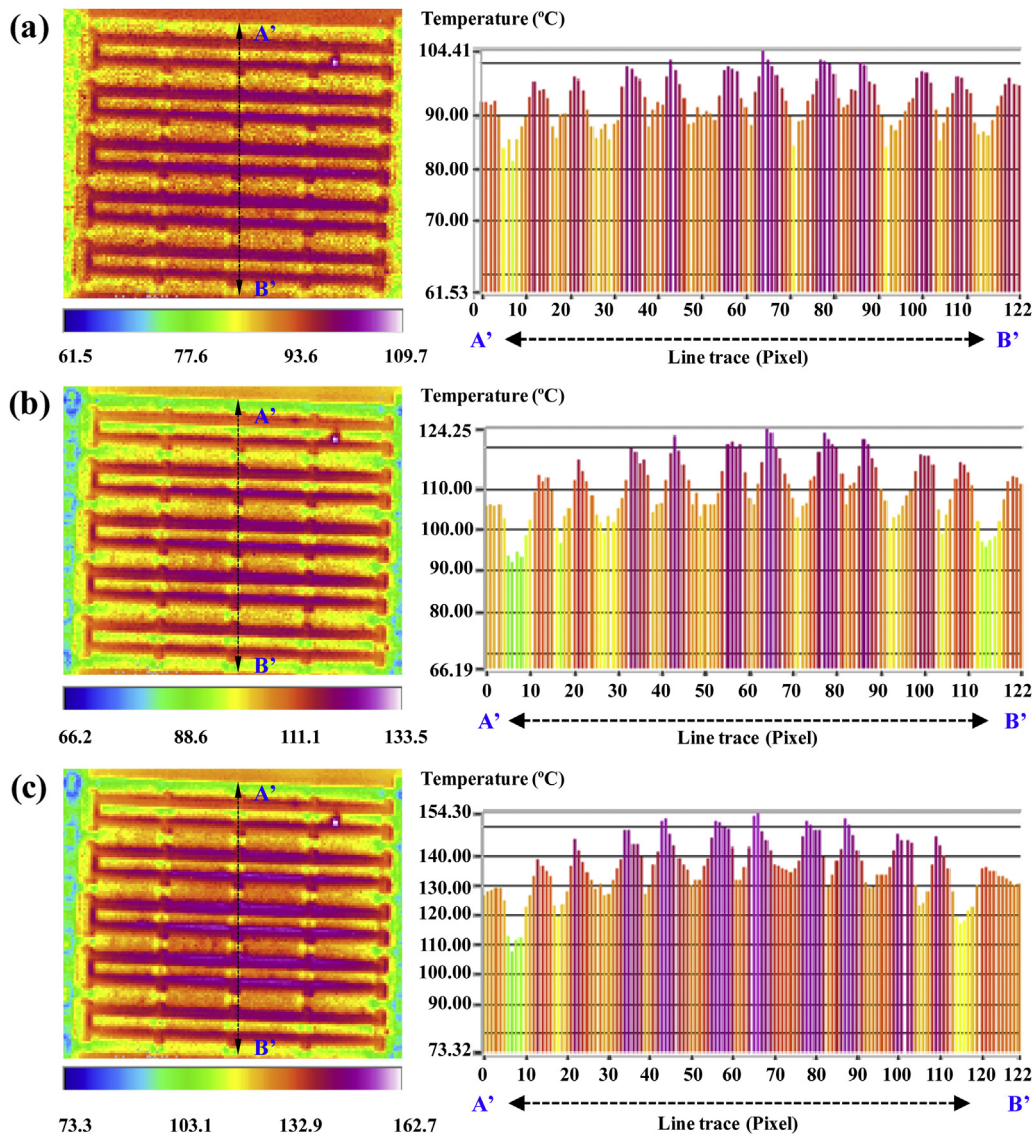


Fig. 7. Thermal maps (left) and line scan profiles (right) based on thermal map for various power dissipations: (a) 5 W, (b) 7 W, (c) 10 W. Temperature line scan recorded along a line (trace A' – B') perpendicular to gate fingers near central region.

corresponding drain-to-source voltage ( $V_{DS}$ ) values. Fig. 7 plots the IR temperature profiles obtained from the maximum cell temperatures within the module. The GaN devices were characterized at three power dissipations, (W) – 5 W, 7 W and 10 W, and at a base plate temperature of 60 °C. Joule heat is generated along narrow strips near the edge of the gates in the gate-to-drain extension regions, where the maximum surface temperature increases from 104.4 to 154.3 °C as the dissipated power increases from 5 to 10 W. At high power dissipation, the line scan profiles (line traces) reveal a steep temperature gradient along the finger between the source and the drain. Here, the effects of heat coupling between the fingers, which induce thermal crosstalk, are negligible.

In each static DC thermal characterization, measured  $I_D$  and  $V_{DS}$  characteristics are recorded along with corresponding surface temperature distributions. InfraScope™ image analysis software is used to measure mean HEMT cell temperatures in each active region (500  $\mu\text{m} \times 500 \mu\text{m}$ ). The individually measurements are then averaged to provide a reference temperature for analyzing the temperature increase in the module. In Fig. 8, the values are used to plot total power dissipation. Although thermal conductivity typically depends on temperature, the relationship between power dissipation and temperatures up to 50 °C is presumably linear since the dependence is weak. A slight temperature variation observed in the parallel cells resulted from a non-uniform current distribution. Thermal placement and increased heat dissipation enhanced the effect. Linear curve fitting showed that the thermal resistance, *i.e.*, the gradient of temperature increase, in the module was 0.3252 °C/W. For reference, the normalized thermal resistance (assuming uniform temperature over the active region) is 1.7886 °C mm<sup>2</sup>/W [34–37]. Since accurate IR temperature measurements were precluded by the silicone potting compound, the module was not encapulated during the measurements. Therefore, the peak voltage stress on the drain and the temperature were limited during testing. After sufficient IR thermal data were collected, the boron nitride coating was removed, and the module was filled with silicone gel for further electrical testing.

#### 4.2. Electrical method for measuring channel temperature

The temperature-dependence of the forward gate-source Schottky junction voltage was used as the temperature-sensitive

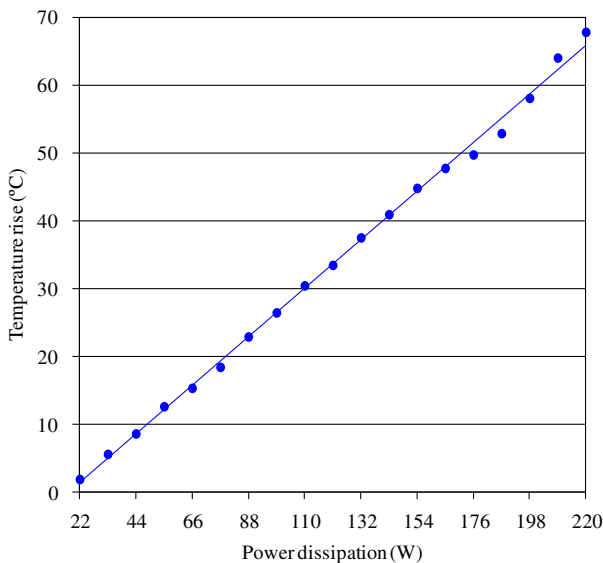


Fig. 8. Experimental IR data indicating a rise in mean cell temperatures at various power dissipations and a base plate temperature of 60 °C.

parameter in the pulsed switching technique [38,39]. However, this technique was difficult to perform because applying a gate bias produces a large forward gate current and a high temperature, which degrades the Schottky contact of the GaN HEMTs. Therefore, channel temperature was estimated in terms of performance-related electrical parameters, *e.g.* maximum drain current  $I_{Dmax}$  and specific drain-to-source resistance  $R_{ON}$  known to be associated with channel temperature [40].

Fig. 9(a) plots the  $I_D - V_{DS}$  characteristics of the packaged module at base plate temperatures of 30 °C–180 °C. The plot was obtained by sweeping  $V_{DS}$  from 0 V to  $V_{DS}$  (max = 4 V) with  $V_{GS}$  set to 0 V. Synchronized gate/drain pulsing is performed in packaged devices to prevent self-heating and carrier trapping [41]. Calibration performed using pulse current as a reference for channel temperature established that, based on  $I_D - V_{DS}$  characteristics, no power was dissipated, and no traps were produced by external electric fields. The maximum drain current  $I_{Dmax}$  (drain current at  $V_{DS} = 4 \text{ V}$  and  $V_{GS} = 0 \text{ V}$ ) declined as the base plate temperature increased because of the reduced electron mobility at elevated temperatures. Fig. 9(b) shows the linearity obtained at a base plate temperature range of 30 °C–180 °C. According to the slope for the pulsed  $I_D - V_{DS}$  curves in Fig. 9(a), the  $R_{ON}$  values for  $V_{DS} = 2 \text{ V}$  are 15.84, 17.63, 20.39, 23.71, 27.82, and 33.23  $\Omega \text{ mm}$ . The extracted pulsed  $I_{Dmax}$  and  $R_{ON}$  are used to determine power dissipation and to generate a lookup table for rapid estimation of actual channel temperature.

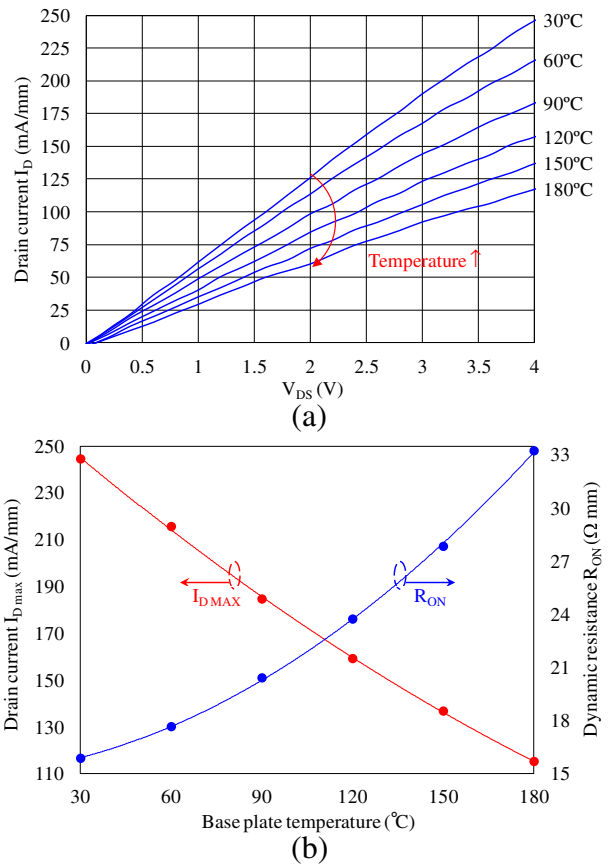
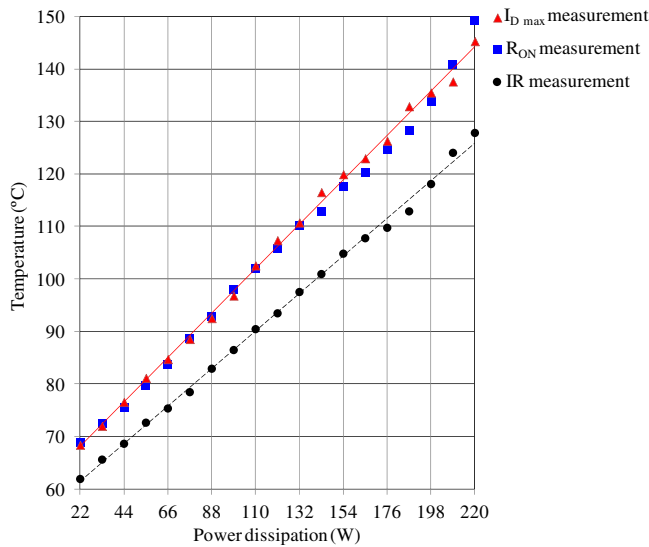


Fig. 9. (a) Pulsed  $I_D - V_{DS}$  measurements from a quiescent bias point ( $V_{DS} = V_{GS} = 0 \text{ V}$ ) without power dissipation at various base plate temperatures. The  $V_{DS}$  is swept from 0 V to 4 V when  $V_{GS}$  is set to 0 V. (b) Extracted  $I_{Dmax}$  and  $R_{ON}$  exhibit a highly linear relationship from 30 °C to 180 °C. Electrical measurements confirmed that channel temperature was related to power dissipation.



**Fig. 10.** Electrical measurements used to estimate module temperatures and IR thermographic measurements used to estimate surface temperatures as functions of power density. Solid line, electrically determined temperature; dashed line, surface temperatures extracted from IR results and averaged across active region.

Fig. 10 presents the cell channel temperatures (solid line) obtained from the pulsed  $I_{Dmax}$  and  $R_{ON}$ . For comparison, the cell surface temperatures (dashed line) extracted from the thermal IR data are also shown. At operating temperatures from 60 °C to 150 °C, the channel temperatures estimated by pulsed  $I_{Dmax}$  measurement agree with those estimated by  $R_{ON}$  measurement, particularly at low power dissipations. The channel temperatures considerably exceed those measured by IR imaging. These experimental results are reasonable because the electrical method averages channel temperatures throughout the active channel region. At elevated base plate temperatures, pulsed  $I-V$  measurements provide an indirect estimate of channel temperature in the packaged module. Although the pulsed  $I-V$  measurements yield a similar temperature rise at low power levels, the temperature begins to diverge from temperature measurements obtained when power dissipation exceeds 8 W per cell. This divergence is attributable to the calibration process and the 180 °C limitation on base plate temperature applied in the electrical method. Since the actual channel temperature exceeds that measured by the electrical method during the calibration process, channel temperature may be underestimated. Instead of providing spatial information about the temperature distribution, the proposed electrical method obtains average temperature across the source–drain opening, which is a non-uniform value in the HEMT cell. However, silicone gels, including those used for insulating and packaging high-voltage modules, distort IR radiation signatures. Hence, a simple method of extrapolating to higher temperatures of an encapsulated module during dynamic operation is needed. The underestimated channel temperature is acceptable for a packaged module in which heat is generated uniformly among cells with no obvious local hot spots. Since the electrical method is not limited by the package encapsulations, the underestimated channel temperature does not limit the use of the electrical method as a fast method of estimating channel temperature in a packaged GAN power module.

## 5. Conclusions

Improvements in GaN HEMT fabrication technology enable fabrication of 400 V cells that can be operated at 2.1 A with low on-state resistance and low switching loss. To support high-power

applications, the cells can be used for parallel interconnections in all-GaN-based power modules with a multiple-chip configuration. The module designs include four power switches in a full-bridge arrangement. Experimental results confirm the high-current capacity of 22 GaN HEMT cells connected in parallel. The static  $I_D - V_{DS}$  characteristics of the module do not significantly differ between base plate temperatures of 25 and 125 °C. The fabricated module has a blocking voltage exceeding 200 V and a leakage current density below 1 mA/mm. Thermal infrared characterizations of thermal resistance and temperature, which rise as a function of power dissipation, are used to determine the surface temperature of the module during operation. In this experiment, the maximum average surface temperature reached 127.7 °C at a base plate temperature of 60 °C, which corresponded to a thermal resistance of 0.3252 °C/W. The electrical technique is also an effective non-destructive method for comparatively analyzing module temperature. It averages channel temperature within the active region of cells by using sub-microsecond pulses to measure  $I_{Dmax}$  and  $R_{ON}$ . The consistent estimates of channel temperature obtained by the technique were confirmed by the close agreement between temperatures determined by  $I_{Dmax}$  and  $R_{ON}$ . These performance evaluations, and the results on which they are based, confirm the feasibility of a multiple-chip GaN power module for high-power applications with parallel interconnections.

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