# Analytic Solution to Product Acceptance Determination for Gold Bumping Process With Multiple Manufacturing Lines

Wen Lea Pearn, Yu Ting Tai, Chia Huang Wu, and Ching Chiang Chuang

Abstract-In recent years, gold bumping process has been applied extensively for the package technology of liquid crystal display driver integrated circuit, which is an essential component in portable devices. Because the increasing requirement of highdefinition display devices, the gold bumping process has become more difficult and it is requested to be of high quality with very low fraction of defectives. Unfortunately, conventional methods for product acceptance determination no longer work because any sample of reasonable size probably contains no defective gold bump product items. In addition, in the globally competitive manufacturing environment, gold bumping processes involving multiple manufacturing lines are quite common in the Science-Based Industrial Park in Hsinchu, Taiwan, because of economic scale considerations. In this paper, we provide analytical solutions to gold bump product acceptance determination, which provide both manufacturers and customers to reserve their own rights by compromising on a rule for gold bumping process with multiple manufacturing lines. For the convenience of inplant applications, we tabulate the number of required inspection units, the critical acceptance values for various manufacturer's risks and consumer's risks, and various number of manufacturing lines. For illustration purpose, a real application in a gold bumping factory, which is located in the Science-Based Industrial Park in Hsinchu, Taiwan, is included.

*Index Terms*—Gold bumping, manufacturing quality, process capability, product acceptance determination.

## I. INTRODUCTION

L IQUID crystal display (LCD) driver integrated circuit (IC) is a critical component in portable devices. In recent years, since increasing demand on higher resolution display in portable devices, such as smart phones and tablet PC, the requirement of precision process on display-related components have played an essential role. It is noted that the packaging technology of LCD driver IC has a significant influence on display performance [1]. For chip-on-glass (COG) package of LCD driver IC, gold bumping process is commonly used in many practical applications [2]. The COG technology

Manuscript received May 1, 2013; revised August 6, 2013; accepted August 20, 2013. Date of publication September 23, 2013; date of current version October 28, 2013. Recommended for publication by Associate Editor B. Dang upon evaluation of reviewers' comments.

W. L. Pearn, C. H. Wu, and C. C. Chuang are with the Department of Industrial Engineering and Management, National Chiao Tung University, Hsinchu 300-10, Taiwan (e-mail: wlpearn@mail.nctu.edu.tw; duckboy614583@gmail.com; freeloop.ms96@g2.nctu.edu.tw).

Y. T. Tai is with the Department of Information Management, Kainan University, Taoyuan 33857, Taiwan (e-mail: yttai@mail.knu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2013.2279889

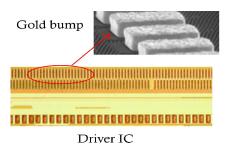


Fig. 1. Diagram of driver IC and bump.

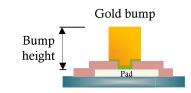


Fig. 2. Bump cross-sectional configuration.

directly bonds the driver IC onto the thin film transistor glass substrate via anisotropic conductive adhesive Fig. 1 shows the part of a LCD driver IC and gold bump. To provide high-definition display devices, a sophisticated gold bumping process is applied to form fine pitch bonds in response to increased demands for more I/Os in smaller spaces. For instance, the LCD driver IC of full high definition (FHD,  $1920 \times 1080$  RGB) resolution needs 2200–2300 pads on outer lead bonding side and ~200 pads on inner lead bonding side.

In gold bumping process, precise height of gold bump is needed to achieve high-resolution display [3]. While some pads with nonuniform gold bump heights, that should induce malfunction of display. Bump height is the height between the top of bump and the top of pad. The bump cross-sectional configuration is shown in Fig. 2. The stagger gold bumps in outer lead bonding side are shown in Fig. 3. Because the gold bumping process requires very low fraction of defectives in parts per million (ppm), traditional methods for calculating the fraction nonconforming no longer work. For instance, the required fraction for defectives of gold bump is often <0.01%. Hence, any sample of reasonable size will probably contain no defective product items.

Process capability indexes (PCIs) are the alternative methods that have been popularly employed in manufacturing yield assessment and quality assurance when process requires very

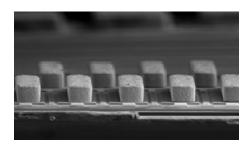


Fig. 3. Diagram of stagger gold bumps.

low fraction of defectives and reaches ppm level. Capability measures for processes with a single manufacturing line have been investigated extensively [4]-[7]. In the gold bumping process, inevitable process variance changes or mean shifts may not be detected within short time. In [3] and [8], the yield assessment methods are incorporated the magnitudes of the undetected variance changes or mean shifts to avoid overestimating manufacturing yield. Additionally, gold bumps have multiple characteristics having effects on the process yield. To obtain accurate yield assessment [9] proposed a overall yield measure index  $C_{pk}^T$ , which is a generalization of the index  $C_{pk}$ , and a natural estimator  $\hat{C}_{pk}^T$  of  $C_{pk}^T$ . The existing literature on gold bumping processes is, however, restricted to discuss single manufacturing line. In most of the globally competitive packaging factories, a gold bumping process with multiple manufacturing lines is common, particularly, for the factories in the Science-Based Industrial Park in Hsinchu, Taiwan. In those packaging factories, a gold bumping process with multiple manufacturing lines consists of multiple parallel independent manufacturing lines, with each manufacturing line having a machine or a group of machines performing necessary identical job operations.

In this paper, we provide an analytical solution to product acceptance determination based on the exact yield index  $S_{pk}^{M}$ for the gold bumping process with multiple manufacturing lines because product acceptance determination is an important part of the supply chain management. This paper is organized as follows. The gold bumping manufacturing process is first presented in Section II. To be practical and convenient to obtain the analytic solution in product acceptance determination for the gold bumping process with multiple manufacturing lines, we provide an implementation procedure and closedform formulas to obtain analytic solutions in Section III. In Section IV, to demonstrate the applicability of the method, we consider a real-world application taken from a gold bumping factory, which is located in the Science-Based Industrial Park in Hsinchu, Taiwan. Finally, Section V provides the conclusion.

### **II. GOLD BUMPING MANUFACTURING PROCESS**

In a gold bumping process, it uses thin film deposition, photolithography, and electroplating processes to form gold bumps on pads. There are eight operations involving RF clean, TiW/Au sputter, photoresist (PR) coating, photo process, Au plating PR stripping, Au/TiW etching, and thermal anneal. Through these operations, the heights

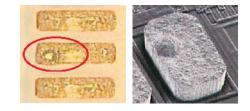


Fig. 4. Diagrams of inconsistent bump height.

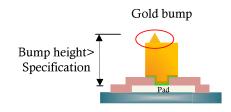


Fig. 5. Diagram of gold bump overhang.



Fig. 6. Side view of nonuniform bump height.

of gold bumps are decided. In the gold bumping manufacturing process, bump height is one of the most critical specifications because pads with inconsistent heights of gold bump should induce malfunction of display and poor display performance.

Because high-definition display devices have become the current trend, the requirements of high-pin-count LCD driver ICs will increase the difficulties of gold bumping manufacturing processes. In FHD  $1920 \times 1080$  RGB products, any pad of these 2200 pads with shorter or higher bump height would induce open failure while mounting the driver IC onto a glass substrate. Figs. 4 and 5 show the inconsistent bump heights and overhang, respectively. These situations may induce higher resistance. In addition, the cost of gold becomes more expensive in recent years. This phenomenon makes that the designers of LCD driver IC accelerate to reduce the cost of gold in gold bumping manufacturing process to be competitive. Therefore, specifications of gold bump height would set to be tighter (from 12 to 9  $\mu$ m). This change also, however, enhances the difficulties of the gold bumping manufacturing process. Fig. 6 shows that nonuniform gold bumps occur.

To make sure thousands of bumps of a die being fall within the tighter specification, the customers (driver IC design house) desire that all the bumps are inspected. These requests, however, cause that gold bumping manufacturers pay more efforts. Then, the outsourcing fee may be raised. Therefore, to make sure the gold bump products to be of high quality with very low fraction of defectives to produce the qualified LCD driver IC for high-definition display devices with tighter specifications, a more accurate product acceptance determination is very critical in the supply chain to determine whether the gold bump product is acceptable or not.

It is also noted that, because of economic scale considerations, in most of the gold bumping manufacturing factories, multiple manufacturing lines are commonly used for gold bumping processes to form specified bumps. Therefore, in this paper, we focus on the product acceptance determination with multiple manufacturing lines for gold bumping manufacturing processes.

## III. PRODUCT ACCEPTANCE DETERMINATION FOR GOLD BUMPING PROCESS WITH MULTIPLE MANUFACTURING LINES

Product acceptance determination is the problem of determining whether the manufactured product should be accepted or rejected based on the inspected sample data, under the designated risks given by the manufacturer and the customer. Because bump height is an essential characteristic of a gold bumping process, which requires very low fraction of defectives in ppm, a well-designed sampling plan is significantly critical for product acceptance determination in global supply chain management. In the product acceptance determination, it cannot avoid the manufacturer's risk of rejecting good product ( $\alpha$ -risk) or customer's risk of accepting bad product ( $\beta$ -risk). For product quality protection and company's considerations, both the manufacturer and customer would focus on two designated points on operating characteristic (OC) curve to reflect their benchmarking risk [10].

Product acceptance determination has been widely discussed and investigated by many quality assurance practitioners and has received substantial research attention. Suresh and Ramanathan [11] and Arizono *et al.* [12] presented the classical acceptance sampling plans. Pearn and Wu [13], [14] developed an effective procedure to deal with the product acceptance determination problem for normally distributed processes with one-sided and two-sided specifications. Wu and Pearn [10] presented a variables sampling plan based on  $C_{pmk}$  for product acceptance determination. The existing research has however, focused on processes with single manufacturing line. Unfortunately, their results cannot be applied in the gold bumping process with multiple manufacturing lines directly.

A yield measurement index  $S_{pk}$  for normal processes with single manufacturing line is provided in [15]. For exact manufacturing yield calculation, [16] proposed a new overall capability index  $(S_{pk}^M)$  for processes with multiple independent lines, which is defined as follows:

$$S_{\rm pk}^{M} = \frac{1}{3} \Phi^{-1} \left\{ \left[ \frac{1}{k} \sum_{j=1}^{k} \left( 2\Phi(3S_{\rm pkj}) - 1 \right) + 1 \right] \middle/ 2 \right\}$$
(1)

where  $S_{pkj}$  is the  $S_{pk}$  value of the *j*th lines for j = 1, 2, ..., kand *k* is the number of manufacturing lines. The function  $\Phi$ is the cumulative distribution function of the standard normal distribution. It is noted that the exact distribution of the overall yield index  $\hat{S}_{pk}^{M}$  defined above is analytically intractable. Tai *et al.* [16] used the Taylor expansion technique to obtain the asymptotic distribution of  $\hat{S}_{pk}^M$ . Tai *et al.* [16] also showed that the conservative lower confidence bound can be obtained by setting  $S_{pki} = (1/3))\Phi^{-1}\{[k(2\Phi(3S_{pk}^M) - 1) - (k-2)]/2\}$ and  $S_{pkj} \ge 2.5$ , for all  $j \ne i$ ,  $a_j = \sqrt{2} \times \{3S_{pkj}\phi(3S_{pkj})\}$ , and  $b_j = 0$  for all j = 1, 2, ..., k. With the above parameters setting, the sampling distribution of  $\hat{S}_{pk}^M$  can be rewritten in a shorter simple form as follows:

$$\hat{S}_{\rm pk}^{M} \sim N\left(S_{\rm pk}^{M}, \frac{D^2\phi^2\left(3D\right)}{2k^2n\phi^2\left(3S_{\rm pk}^{M}\right)}\right) \tag{2}$$

where

$$D = \left(\frac{1}{3}\right) \Phi^{-1} \left\{ \left[ k \left( 2\Phi \left( 3S_{\text{pk}}^M \right) - 1 \right) - (k-2) \right] / 2 \right\}.$$

Because the gold bumping manufacturing process is commonly with multiple manufacturing lines in factories, the  $S_{pk}^M$ index can be used as a quality benchmark for gold bump product acceptance. Consider a sampling plan for the gold bump products with the very low fraction of nonconforming parts. A gold bump acceptance determination procedure focuses on two designated points: 1) acceptable quality level (AQL,  $1-\alpha$ ) and 2) lot tolerance percent defective (LTPD,  $\beta$ ) on the OC curve. It should be noted that AQL and LTPD are levels of the product fraction of defectives that correspond to acceptable and rejectable quality levels.

Because the AQL is a standard that is used to determine whether the gold bump products should be accepted or not, it is hoped that the manufacturer's process is considerable better than the AQL. To determine whether a given gold bumping process is capable, the null hypothesis with process fraction of defectives,  $H_0$ :  $p \leq AQL$ , is equivalent to test PCI with  $H_0$ :  $S_{pk}^M \geq C_{AQL}$ , where  $C_{AQL}$  is the level of acceptable quality for  $S_{pk}^M$  index corresponding to the gold bumping process or process fraction of defectives AQL. For manufacturers and customers, two conditions are considered

Pr {Reject the gold bump product  $| p \le AQL$ }

= Pr {Reject the gold bump product  $|S_{pk}^M \ge C_{AQL}$ }  $\le \alpha$  (3)

Pr {Accepting the bump product  $| p \ge LTPD$  }

= Pr {Accepting the bump product  $S_{pk}^{M} \le C_{LTPD}$ }  $\le \beta$  (4)

where  $C_{\text{LTPD}}$  is the gold bump capability requirement corresponding to the LTPD on the basis of  $S_{\text{pk}}^M$  index.

That is, the probability of rejecting acceptable gold bump products is no more than  $\alpha$ . Simultaneously, the probability of accepting unqualified gold bump products is no more than  $\beta$ . Our purpose is to solve the two simultaneous equations mentioned earlier, and then obtaining the required inspection sample size *n* and the critical acceptance value  $c_0$  of  $S_{pk}^M$ . These two conditions can be satisfied by the following two equations:

$$S_{1}(n, c_{0}) = \int_{c_{0}}^{\infty} \frac{1}{\sqrt{2\pi \left(\frac{D_{1}^{2}\phi^{2}(3D_{1})}{2k^{2}n\phi^{2}(3C_{AQL})}\right)}}$$
$$\times \exp\left[-\frac{\left(x - C_{AQL}\right)^{2}}{2\left(\frac{D_{1}^{2}\phi^{2}(3D_{1})}{2k^{2}n\phi^{2}(3C_{AQL})}\right)}\right] dx - (1 - \alpha).$$
(5)

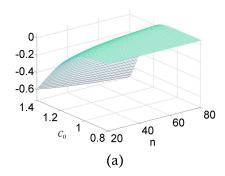


Fig. 7. (a) Surface plot of  $S_1(n, c_0)$ . (b) Contour plot of  $S_1(n, c_0)$ .

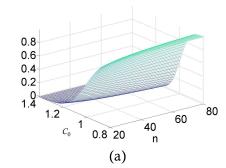


Fig. 8. (a) Surface plot of  $S_2(n, c_0)$ . (b) Contour plot of  $S_2(n, c_0)$ .

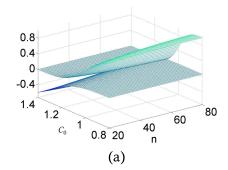
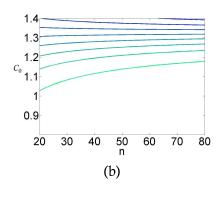


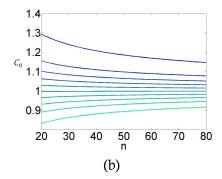
Fig. 9. (a) Surface plot of  $S_1$  and  $S_2$ . (b) Contour plot of  $S_1$  and  $S_2$ .

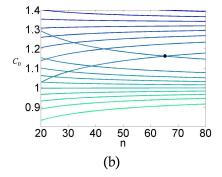
$$S_{2}(n, c_{0}) = \int_{c_{0}}^{\infty} \frac{1}{\sqrt{2\pi \left(\frac{D_{2}^{2}\phi^{2}(3D_{2})}{2k^{2}n\phi^{2}(3C_{\text{LTPD}})}\right)}} \times \exp\left[-\frac{(x - C_{\text{LTPD}})^{2}}{2\left(\frac{D_{2}^{2}\phi^{2}(3D_{2})}{2k^{2}n\phi^{2}(3C_{\text{LTPD}})}\right)}\right] dx - \beta.$$
(6)

For  $C_{AQL} = 1.33$  and  $C_{LTPD} = 1.00$ , Figs. 7(a) and (b) and 8(a) and (b) show the surface and contour plots of (5) and (6), respectively, with  $\alpha$ -risk = 0.05 and  $\beta$ -risk = 0.01.

Fig. 9(a) and (b) shows the surface and contour plots of (5) and (6) simultaneously with  $\alpha$ -risk = 0.05 and  $\beta$ -risk = 0.01, respectively. From Fig. 9(b), we can obtain that the interaction of  $S_1(n, c_0)$  and  $S_2(n, c_0)$  contour curves at level 0 is  $(n, c_0) =$  (66, 1.1632), which is the solution to nonlinear simultaneous







(5) and (6). That is, in the case, the minimum required sample size n = 66 and critical acceptance value  $c_0 = 1.1632$  of the sampling plan based on the capability index  $S_{pk}^M$ . Using the approximate distribution of  $\hat{S}_{pk}^M$ , two conditions can be expressed as

$$P\left(\hat{S}_{pk}^{M} < c_{0} \mid S_{pk}^{M} \ge C_{AQL}\right) \le P\left(Z < \frac{c_{0} - C_{AQL}}{\frac{D_{1}\phi(3D_{1})}{\sqrt{2}k\sqrt{n}\phi(3C_{AQL})}}\right) \le \alpha$$

$$(7)$$

$$P\left(\hat{S}_{pk}^{M} \ge c_{0} \mid S_{pk}^{M} \le C_{LTPD}\right) \le P\left(Z \ge \frac{c_{0} - C_{LTPD}}{\frac{D_{2}\phi(3D_{2})}{\sqrt{2}k\sqrt{n}\phi(3C_{LTPD})}}\right) \le \beta$$

$$(8)$$

where  $D_1$  and  $D_2$  are the values of parameters D with  $S_{pk}^M = C_{AQL}$  and  $S_{pk}^M = C_{LTPD}$ , respectively.

<i>k</i> =3		$C_{AQL} = 1.33$		$C_{AQL} = 1.50$		$C_{AQL} = 1.67$		$C_{AQL} = 2.00$	
		$C_{LTI}$		$C_{LTPD} = 1.33$		$C_{LTPD} = 1.50$		$C_{LTPD} = 1.67$	
α	$\beta$	п	$c_0$	п	$C_0$	п	$\mathcal{C}_0$	п	$C_0$
0.01	0.01	96	1.1344	593	1.4087	780	1.5796	291	1.8183
	0.025	84	1.1209	510	1.4016	669	1.5724	251	1.8044
	0.05	75	1.1087	443	1.3944	581	1.5653	219	1.7906
	0.075	69	1.0992	402	1.3892	526	1.5600	200	1.7808
	0.1	64	1.0904	372	1.3848	486	1.5555	186	1.7728
0.025	0.01	79	1.1483	497	1.4160	655	1.5869	243	1.8325
	0.025	68	1.1342	421	1.4088	554	1.5797	207	1.8185
	0.05	60	1.1215	361	1.4015	473	1.5722	178	1.8043
	0.075	54	1.1102	324	1.3960	425	1.5669	160	1.7936
	0.1	51	1.1039	297	1.3914	389	1.5622	148	1.7854
0.05	0.01	66	1.1632	421	1.4234	556	1.5943	205	1.8470
	0.025	56	1.1489	352	1.4163	463	1.5871	172	1.8329
	0.05	48	1.1344	297	1.4088	390	1.5797	146	1.8186
	0.075	44	1.1257	264	1.4033	346	1.5741	130	1.8078
	0.1	40	1.1157	239	1.3984	314	1.5693	118	1.7983
0.075	0.01	58	1.1743	375	1.4290	496	1.5999	182	1.8578
	0.025	49	1.1606	310	1.4219	408	1.5927	151	1.8439
	0.05	41	1.1448	258	1.4144	340	1.5853	126	1.8291
	0.075	37	1.1350	227	1.4087	299	1.5797	112	1.8188
	0.1	34	1.1266	205	1.4040	269	1.5748	101	1.8092
0.1	0.01	52	1.1836	342	1.4338	452	1.6046	165	1.8671
	0.025	43	1.1690	279	1.4267	369	1.5976	135	1.8531
	0.05	37	1.1564	231	1.4195	304	1.5903	112	1.8387
	0.075	32	1.1433	202	1.4139	265	1.5846	99	1.8284
	0.1	29	1.1339	180	1.4088	237	1.5797	89	1.8190

TABLE IRequired Sample Sizes (n) and Critical Acceptance Values ( $c_0$ ) for Various  $\alpha$  and  $\beta$ -Risks WithMANUFACTURING LINES k = 3 and Selected  $C_{AOL}$ ,  $C_{LTPD}$ 

Equations (7) and (8) imply that

$$\frac{c_0 - C_{\text{AQL}}}{\frac{D_1 \phi(3D_1)}{\sqrt{2k}\sqrt{n}\phi(3C_{\text{AQL}})}} = Z_{1-\alpha} = -Z_\alpha \tag{9}$$

$$\frac{c_0 - C_{\text{LTPD}}}{\frac{D_2\phi(3D_2)}{\sqrt{2k}\sqrt{n}\phi(3C_{\text{LTPD}})}} = Z_\beta.$$
(10)

From (9) and (10), we have

$$c_0 - C_{\text{AQL}} = -Z_\alpha \frac{D_1 \phi(3D_1)}{\sqrt{2k\phi(3C_{\text{AQL}})}} \times \frac{1}{\sqrt{n}}$$
(11)

$$c_0 - C_{\text{LTPD}} = Z_\beta \frac{D_2 \phi(3D_2)}{\sqrt{2}k\phi(3C_{\text{LTPD}})} \times \frac{1}{\sqrt{n}}.$$
 (12)

Subtracting (11) by (12) yields

$$C_{\text{AQL}} - C_{\text{LTPD}} = \frac{1}{\sqrt{n}} \left\{ \frac{Z_{\alpha} D_1 \phi(3D_1)}{\sqrt{2}k\phi(3C_{\text{AQL}})} + \frac{Z_{\beta} D_2 \phi(3D_2)}{\sqrt{2}k\phi(3C_{\text{LTPD}})} \right\}.$$
(13)

Therefore, from (13), we establish the required inspection sample size n and the corresponding critical

value  $c_0$  as

$$n = \left[ \left( \frac{\frac{Z_{a}D_{1}\phi(3D_{1})}{\sqrt{2k\phi(3C_{AQL})}} + \frac{Z_{\beta}D_{2}\phi(3D_{2})}{\sqrt{2k\phi(3C_{LTPD})}}}{C_{AQL} - C_{LTPD}} \right)^{2} \right]$$
(14)  

$$c_{0} = C_{AQL} - Z_{\alpha} \frac{D_{1}\phi(3D_{1})}{\sqrt{2k\phi(3C_{AQL})}} \times \frac{1}{\sqrt{2k\phi(3C_{AQL})}} \left( \frac{\frac{Z_{\alpha}D_{1}\phi(3D_{1})}{\sqrt{2k\phi(3C_{AQL})}} + \frac{Z_{\beta}D_{2}\phi(3D_{2})}{\sqrt{2k\phi(3C_{LTPD})}}}{C_{AQL} - C_{LTPD}} \right)^{2} \right]$$
(15)

The symbol  $\lceil n \rceil$  means the ceiling function that obtains the least integer greater than or equal to *n*.

Table I shows  $(n, c_0)$  values for  $\alpha$ -risk = 0.01, 0.025, 0.05, 0.075, 0.1 and customer's  $\beta$ -risk = 0.01, 0.025, 0.05, 0.075, 0.1 with manufacturing lines k = 3 and various benchmarking quality levels,  $(C_{AQL}, C_{LTPD}) = (1.33, 1.00)$ , (1.50, 1.33), (1.67, 1.50), and (2.00, 1.67). For practical purposes, we provide a useful procedure for the proposed sampling plan as follows.

Step 1: Decide process capability requirements (i.e.,  $C_{AQL}$  and  $C_{LTPD}$ ), manufacturer's risk ( $\alpha$ -risk), and customer's risk ( $\beta$ -risk).

- Step 2: Obtain required sample sizes (*n*) and critical acceptance values ( $c_0$ ) based on the designated values of  $\alpha$ -risk,  $\beta$ -risk, number of manufacturing lines *k*,  $C_{AQL}$ , and  $C_{LTPD}$  from Table I or (14) and (15).
- Step 3: Calculate the value of  $\hat{S}_{pk}^M$  from these *n* inspected samples.
- Step 4: Make a decision to accept the entire gold bump products if the estimated  $\hat{S}_{pk}^M$  value is greater than the critical value  $c_0$ . Otherwise, we reject the entire products.

For example, if the benchmarking quality level ( $C_{AQL}$ ,  $C_{LTPD}$ ) is set to (1.33, 1.00) with  $\alpha$ -risk = 0.05 and  $\beta$ -risk = 0.01, the corresponding sample size and critical value can be obtained as  $(n, c_0) = (66, 1.1632)$ , which can be obtained in Table I. The gold bump product will be accepted if the 66 inspected product items yield measurements with  $S_{pk}^M \ge 1.1632$ , which is corresponding to the contour plots we have mentioned above.

## IV. APPLICATION FOR PRODUCT ACCEPTANCE DETERMINATION OF GOLD BUMPING PROCESS WITH THREE MANUFACTURING LINES

To demonstrate the applicability of the proposed product acceptance determination of gold bumping process with multiple manufacturing lines, we consider a factory application taken from a gold bumping factory located in the Science-Based Industrial Park at Hsinchu, Taiwan. For a newly mass production product, FHD1080H (FHD, 1920 × 1080 RGB), a quality practitioner of IC design house employs a sampling plan for the gold bump product acceptance determination. Because the manufacturer's factory involves three manufacturing lines, the inspection data are collected from the lines separately. In current factory practices, five designate die sites are inspected on a wafer at the location of top, center, bottom, left, and right. In addition, four bump sites including left side of top, right side of top, left side of down, and right side of down are inspected on one die site.

The upper specification limit, target, and lower specification limit on bump height for the FHD1080H product we investigated are 10.5, 9, and 7.5  $\mu$ m, respectively. An acceptance sampling plan is applied to decide the gold bump product is accepted or rejected. It is noted that if the characteristic data do not fall within the tolerance (USLLSL), the reliability of the product will decrease. In the contract, the  $C_{AOL}$  and  $C_{LTPD}$  are set to 1.33 and 1.00, respectively, with  $\alpha$ -risk = 0.05 and  $\beta$ -risk = 0.05. In Table I, we can obtain the acceptance critical value and inspected sample sizes of sampling plan  $(n, c_0) = (48, 1.1344)$ , which are obtained using the closed-form formulas shown in Section III. The inspected sample sizes and critical acceptance values are used to provide the desired levels of protection for both manufacturers and customers. In the case, the 48 observations of the bump height are collected from each manufacturing line in the gold bumping process. Table II shows the calculated statistics of the bump height in these three manufacturing lines.

With the data, the quality practitioner would accept the entire products because the value of sample estimator

TABLE II CALCULATED STATISTICS OF THE THREE MANUFACTURING LINES (UNIT: µm)

Lines	$\overline{X}_{_j}$	S <sub>j</sub>	${\hat S}_{_{pkj}}$
1	8.125	0.2027	1.0947
2	9.735	0.1351	1.9267
3	8.991	0.3286	1.5210

 $\hat{S}_{pk}^{M} = 1.1936$ , which is greater than the value of critical acceptance  $c_0 = 1.1344$ .

#### V. CONCLUSION

The gold bumping is an essential process that mainly affects the display performance of high-definition display devices, such as smart phones and tablet PC. Because the requirement of high-pin-count LCD diver IC chips would increase the difficulties of manufacturing the gold bumps, in this paper, we provided a useful product acceptance determination method for gold bumping process with multiple manufacturing lines. The proposed acceptance sampling plans are very practical and effective tools for quality assurance applications in gold bumping factories, which provide a feasible inspection policy. The policy can be applied to gold bumping process with multiple manufacturing lines. In this paper, we presented the closed-form formulas to obtain the required number of inspection sample size and the corresponding critical values based on commonly used manufacturer's risks, consumer's risks, and designated  $C_{AOL}$ ,  $C_{LTPD}$  for various numbers of gold bumping manufacturing lines. The results obtained could help the gold bumping practitioners to make more reliable decisions on whether the gold bump products are acceptable or not for the gold bumping processes with multiple manufacturing lines.

#### REFERENCES

- U. B. Kang and Y. H. Kim, "A new COG technique using low temperature solder bumps for LCD Driver IC packaging applications," *IEEE Trans. Compon. Packag. Technol.*, vol. 27, no. 2, pp. 253–258, Jun. 2004.
- [2] Y. W. Yen and C. Y. Lee, "Driver IC and COG package design," *IEEE Trans. Compon. Packag. Technol.*, vol. 31, no. 2, pp. 399–406, Jun. 2008.
- [3] W. L. Pearn, Y. T. Tai, and W. L. Chiang, "Measuring manufacturing yield for gold bumping processes under dynamic variance change," *IEEE Trans. Electron. Packag. Manuf.*, vol. 33, no. 2, pp. 77–83, Apr. 2010.
- [4] C. W. Wu, W. L. Pearn, and S. Kotz, "An overview of theory and practice on process capability indices for quality assurance," *Int. J. Prod. Econ.*, vol. 117, no. 2, pp. 338–359, 2009.
- [5] W. L. Pearn and C. H. Wu, "Supplier selection for multiple characteristics processes with one-sided specifications," *Qual. Technol. Quant. Manag.*, vol. 10, no. 1, pp. 133–140. 2013.
- [6] D. Grau, "Process yield, process centering and capability indices for one-sided tolerance processes," *Qual. Technol. Quant. Manag.*, vol. 9, no. 2, pp. 153–170, 2012.
- [7] D. Grau, "On the choice of a capability index for asymmetric tolerances," *Qual. Technol. Quant. Manag.*, vol. 7, no. 3, pp. 301–319, 2010.
  [8] W. L. Pearn, H. N. Hung, Y. T. Tai, and H. H. Hou, "Process capability
- [8] W. L. Pearn, H. N. Hung, Y. T. Tai, and H. H. Hou, "Process capability evaluation for square bumps with mean shift," *J. Test. Evaluat.*, vol. 39, no. 5, pp. 918–927, 2011.

- [9] W. L. Pearn, J.-J. H. Shiau, Y. T. Tai, and M. Y. Li, "Capability assessment for processes with multiple characteristics: A generalization of the popular index C<sub>pk</sub>," Qual. Rel. Eng. Int., vol. 27, no. 8, pp. 1119–1129, 2011.
- [10] C. W. Wu and W. L. Pearn, "A variables sampling plan based on C<sub>pmk</sub> for product acceptance determination," *Eur. J. Oper. Res.*, vol. 184, no. 2, pp. 549–560, 2008.
- [11] R. P. Suresh and T. V. Ramanathan, "Acceptance sampling plans by variables for a class of symmetric distributions," *Commun. Stat., Simul. Comput.*, vol. 26, no. 4, pp. 1379–1391, 1997.
- [12] I. Arizono, A. Kanagawa, H. Ohta, K. Watakabe, and K. Tateishi, "Variable sampling plans for normal distribution indexed by Taguchi's loss function," *Naval Res. Logist.*, vol. 44, no. 6, pp. 591–603, 1997.
- [13] W. L. Pearn and C. W. Wu, "Critical acceptance values and sample sizes of a variables sampling plan for very low fraction of defectives," *Omega*, vol. 34, no. 1, pp. 90–101, 2006.
- [14] W. L. Pearn and C. W. Wu, "An effective decision making method for product acceptance," *Omega*, vol. 35, no. 1, pp. 12–21, 2007.
- [15] R. A. Boyles, "Process capability with asymmetric tolerances," *Commun. Stat., Simul. Comput.*, vol. 23, no. 3, pp. 615–643, 1994.
- [16] Y. T. Tai, W. L. Pearn, and C. M. Kao, "Measuring the manufacturing yield for processes with multiple manufacturing lines," *IEEE Trans. Semicond. Manuf.*, vol. 25, no. 2, pp. 284–290, May 2012.



Yu Ting Tai received the Ph.D. degree in industrial engineering and management from National Chiao-Tung University, Hsinchu, Taiwan.

She is an Associate Professor with the Department of Information Management, Kainan University, Taoyuan, Taiwan. Her current research interests include scheduling, semiconductor manufacturing management, and quality management.



**Chia Huang Wu** received the Ph.D. degree in industrial engineering and management from National Chiao-Tung University, Hsinchu, Taiwan.

He is currently a Post-Doctoral Researcher with National Chiao-Tung University. His current research interests include queueing theory, optimization theory, process capability index, and applied statistics.



Wen Lea Pearn received the Ph.D. degree in operations research from the University of Maryland, College Park, MD, USA.

He is a Professor of operations research and quality assurance with National Chiao-Tung University (NCTU), Hsinchu, Taiwan. He was with Bell Laboratories, Murray Hill, NJ, USA, as a Quality Research Scientist before joining NCTU. His current research interests include process capability, network optimization, and production management. His publications have appeared in the

Journal of the Royal Statistical Society, Series C, Journal of Quality Technology, European Journal of Operational Research, Journal of the Operational Research Society, Operations Research Letters, Omega, Networks and International Journal of Productions Research.



**Ching Ching Chuang** received the M.S. degree in industrial engineering and management from National Chiao-Tung University, Hsinchu, Taiwan. She is an Engineer with the Taiwan Semiconductor Manufacturing Company, Hsinchu. Her current research interests include process capability.