Three–Dimensional Metal Gate–High-κ–GOI CMOSFETs on 1-Poly-6-Metal 0.18-μm Si Devices

D. S. Yu, Albert Chin, *Senior Member, IEEE*, C. C. Liao, C. F. Lee, C. F. Cheng, M. F. Li, *Senior Member, IEEE*, Won Jong Yoo, *Senior Member, IEEE*, and S. P. McAlister, *Senior Member, IEEE*

***Abstract*—We demonstrate three-dimensional (3-D) self-aligned [IrO_2–IrO_2–Hf]–$LaAlO_3$–Ge-on-Insulator (GOI) CMOSFETs above 0.18-μm Si CMOSFETs for the first time. At an equivalent oxide thickness of 1.4 nm, the 3-D IrO_2–$LaAlO_3$–GOI p-MOSFETs and IrO_2–Hf–$LaAlO_3$–GOI nMOSFETs show high hole and electron mobilities of 234 and 357 cm^2/Vs respectively, without depredating the underneath 0.18-μm Si devices. The hole mobility is 2.5 times higher than the universal mobility, at 1 MV/cm effective electric field. These promising results are due to the low-temperature GOI device process, which is well-matched to the low thermal budget requirements of 3-D integration. The high-performance GOI devices and simple 3-D integration process, compatible to current very large-scale integration (VLSI) technology, should be useful for future VLSI.**

***Index Terms*—Ge-on-insulator (GOI), $LaAlO_3$, metal–gate, MOSFET, three-dimensional (3-D).**

I. Introduction

ONE of the biggest challenges for very large-scale integration (VLSI) technology is the ac power consumption [1] caused by the interconnect parasitic capacitance ($C_v{}^2 f/2$), which becomes a major limit for VLSI ICs beyond the implementation of metal–gates and high-κ nano-CMOS to solve the dc power in gate leakage [2]. Increasing operational frequency (f) of circuits with denser interconnects makes the ac power consumption even worse. A potential solution is three-dimensional (3-D) integration which can effectively shorten the interconnect distances and therefore reduce the ac power consumption. Such 3-D integration can also provide a way to increase the IC density [3] (equivalent to scaling down) once the quantum–mechanical scaling barrier is reached. However, the technology challenges are how to realize 3-D ICs [4]–[6] with a low thermal budget and small impact on lower multiple interconnect and CMOSFET layers. Using the inherent low-temperature process of the Ge-on-insulator (GOI) technology [7]–[13], we have integrated self-aligned IrO_2-IrO_2–Hf dual-gated–$LaAlO_3$–GOI CMOSFETs on 1-Poly-6-Metal (1P6M) 0.18-μm Si devices. The process yields GOI CMOSFETs with high hole and electron mobilities, without degrading the underlying Si devices. This approach is promising for future high-performance VLSI ICs.

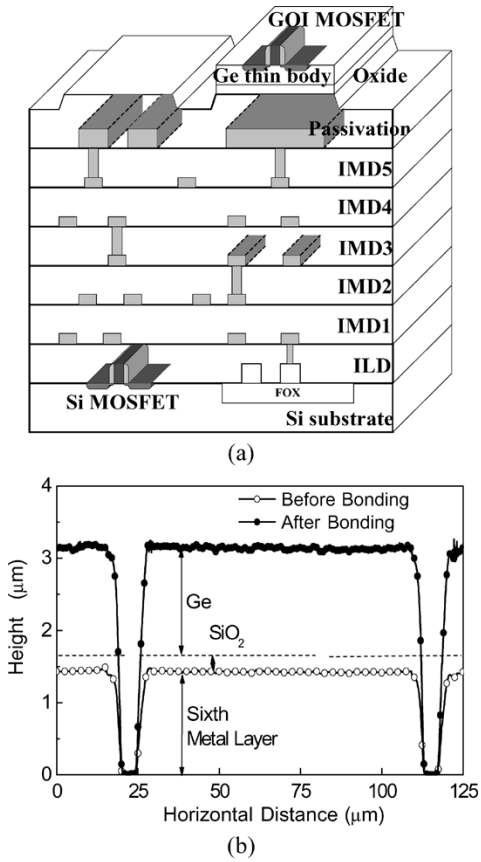

Fig. 1. (a) Schematic the structure of GOI CMOS and (b) the surface profiles of the fabricated wafer, before and after GOI bonding. The thickness is 300 μm for Si substrate and 1.6 μm for Ge thin body. The gate length is 0.18-μm for lower layer Si MOSFETs and 10-μm for top layer GOI MOSFETs.

II. Experimental Details

The self-aligned 3-D GOI CMOSFETs were formed by depositing 200-nm plasma-enhanced chemical vapor deposition oxide on both H^+-implanted Ge (5×10^{16} cm^{-2} dose at 200

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D. S. Yu, C. C. Liao, C. F. Lee, and C. F. Cheng are with the Nano Science Technology Center, Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

A. Chin is with the Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260, on leave from the Nano Science Technology Center, Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail albert_achin@hotmail.com).

M. F. Li and W. J. Yoo are with the Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260.

S. P. McAlister is with the National Research Council of Canada, Ottawa, ON K4C 1B6, Canada

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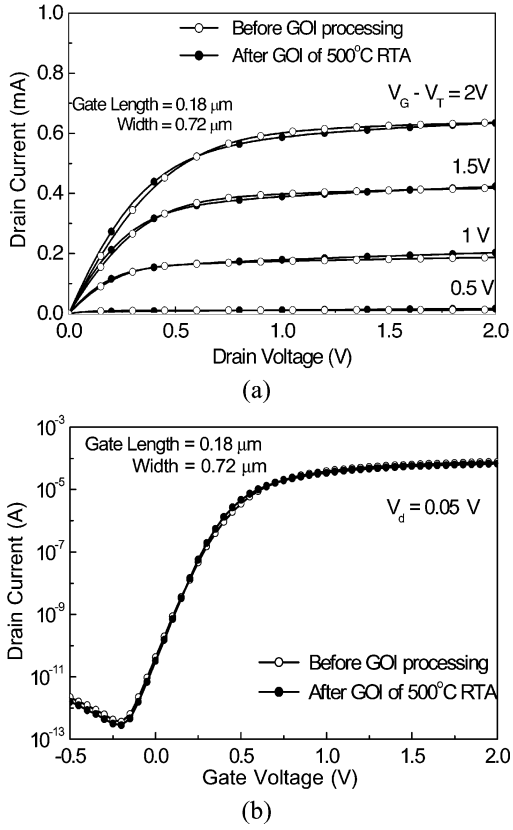

Fig. 2. (a) I_d-V_d and (b) the I_d-V_g characteristics of lower layer Si 0.18-μm MOSFETs, before and after GOI bonding.

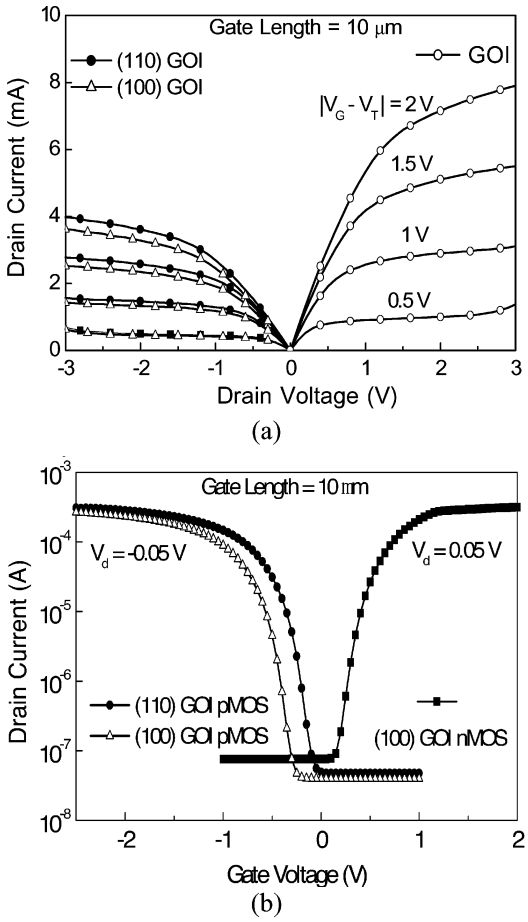

Fig. 3. (a) I_d-V_d and (b) the I_d-V_g characteristics for the top layer [IrO_2-IrO_2–Hf]–$LaAlO_3$–GOI CMOSFETs. The gate length was 10-μm.

KeV) and 1P6M 0.18-μm MOSFETs wafers, O_2 plasma-enhanced bonding, a 300 °C "smart cut," 400 °C annealing for 0.5 h, and then slight polishing [7]–[9], [12], [13]. Both (100) and (110) n-Ge and (100) p-Ge substrates were used for the 3-D GOI. The $LaAlO_3$ gate dielectric was deposited by PVD from a $LaAlO_3$ source ($\kappa = 25.1$) followed by 400 °C oxidation [12], [13]. Then a 150-nm IrO_2 or 150-nm IrO_2–15-nm Hf gate was deposited on the $LaAlO_3$ by PVD for the p- or nMOSFETs, respectively. Low work-function Hf was used for nMOSFETs, similar to fully silicided NiSi:Hf–Al_2O_3 devices [12], [13]. The IrO_2–$LaAlO_3$ p-MOSFETs or IrO_2–Hf–$LaAlO_3$ nMOSFETs was formed by self- aligned 25 keV boron or 35 keV phosphorus implantation, followed by a 500 °C rapid thermal annealing (RTA) .

III. Results and Discussion

Fig. 1 shows the schematic the structure of GOI CMOS. Because the top metal (M6) was 2 μm thick and not planarized, the GOI can only be formed on the selective area above the metal pads. This is evident from the surface profile shown in Fig. 1(b), where there is no Ge beyond the metal pads. The measured Ge thickness of 1.6-μm is close to that of our previous reports [12], [13].

It is important to characterize the effect of the GOI processing on the lower layer of Si devices. Fig. 2(a) and (b) shows the I_d-V_d and I_d-V_g characteristics of the lower Si MOSFETs. We have used additional metal contact area, outside the top GOI transistor, to connect the lower layer Si CMOSFETs. Further developing the more dense contact, similar to a VLSI backend interconnect, is under development. The 500 °C RTA thermal budget for ion implantation of the self-aligned [IrO_2-IrO_2–Hf]–$LaAlO_3$–GOI CMOSFETs did not result in any significant degradation of the subthreshold swing ($\sim$ 80 mV/decade) and I_{off} (5×10^{-11} A/μm) in underneath 0.18-μm Si MOSFETs. Besides, the thermal budget used here is even lower than that of 10-nm MOSFETs [2] and suitable for further 3-D integration with ultrasmall devices. The thermal budget constrain also makes the 3-D integration of Si-on-insulator (SOI) over interconnect and bottom MOSFETs impossible, because of the high RTA temperature (1000 °C–1050 °C) required for the ion implantation anneal of the top layer SOI CMOSFETs. This will damage the bottom layer silicide junction and interconnects. It is also contrary to the trend toward low thermal budgets for nano-CMOS [2].

Fig. 3(a) and (b) shows I_d-V_d characteristics for a family of $|V_g - V_t|$ values, and I_d-V_g of 3-D $LaAlO_3$–GOI CMOSFETs with metal-like IrO_2–Hf and IrO_2 dual gates. An EOT of 1.4-nm was obtained from the C-V measurements. To the best of our knowledge these good results are the first demonstration of 3-D integration, using a process compatible with current VLSI technology, which does not degrade the lower layer MOSFETs. The (110) p-MOSFETs had higher drive current than the (100) devices – such hole mobility enhancement has been reported in the literature [14].

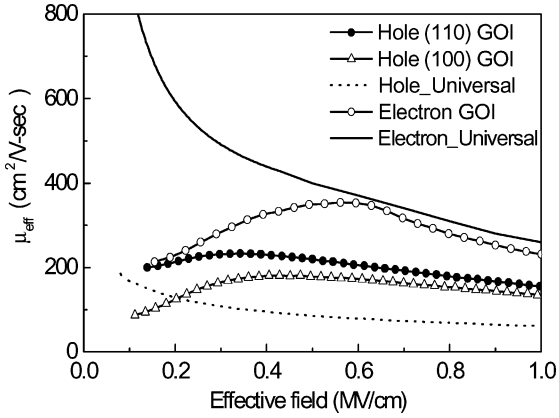

Fig. 4. Electron and hole mobilities of IrO_2–Hf–$LaAlO_3$–GOI nMOSFETs and IrO_2–$LaAlO_3$–GOI p-MOSFETs.

The IrO_2–Hf–$LaAlO_3$–GOI nMOSFETs have a peak electron mobility of 357 cm^2/Vs and values close to universal electron mobility at higher E_{eff} (Fig. 4). Peak hole mobilities of 181 and 234 cm^2/Vs were measured for the IrO_2–$LaAlO_3$–GOI p-MOSFETs on (100) and (110) substrates, respectively. These hole mobilities are higher than universal mobility values. The 136 and 156 cm^2/Vs values at E_{eff} of 1 MV/cm are 2.2- and 2.5-times higher than that of the universal hole mobility. Such mobility enhancement reflects the smaller Ge effective mass than Si [11].

IV. Conclusion

We have fabricated the [IrO_2-IrO_2–Hf]–$LaAlO_3$–GOI CMOSFETs on 1P6M 0.18-μm Si devices. At the 1.4-nm EOT, the peak electron and hole mobilities are 357 and 234 cm^2/Vs, the hole mobility being 2.5 times higher than the universal mobility at 1 MV/cm E_{eff}. These high mobility self-aligned 3-D metal-gate/high-κ–GOI devices and their successful 3-D integration are promising for future VLSI.

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