Germanium pMOSFETs With Schottky-Barrier Germanide S/D, High-κ Gate Dielectric and Metal Gate

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***Abstract*—Schottky-barrier source/drain (S/D) germanium p-channel MOSFETs are demonstrated for the first time with HfAlO gate dielectric, HfN–TaN metal gate and self-aligned NiGe S/D. The drain drivability is improved over the silicon counterpart with PtSi S/D by as much as ∼5 times due to the lower hole Schottky barrier of the NiGe–Ge contact than that of PtSi–Si contact as well as the higher mobility of Ge channel than that of Si.**

***Index Terms*—Germanium, high-κ, metal gate, MOSFET, Schottky.**

I. Introduction

GERMANIUM is an attractive channel material due to its high low-field carrier mobility. Germanium p-channel MOSFETs with enhanced mobility have been demonstrated using germanium oxynitride, ZrO_2, Al_2O_3 and HfO_2 as the gate dielectric [1]–[4]. Another technology bottleneck for future scaling of MOSFET is the fabrication of ultra-shallow source/drain (S/D) with low series resistance [5]. A Schottky-barrier S/D transistor (SSDT) structure has been proposed to solve this problem [6], [7]. However, an SSDT is difficult to use to achieve high drive current due to the relatively high potential barrier (Schottky barrier) between the source and the channel [8]. This problem may be overcome, or at least alleviated, by using a Ge substrate because of the low Schottky-barrier height of germanide–Ge contact and the high carrier mobility of Ge. In this letter, p-channel SSDTs with HfAlO gate dielectrics, HfN–TaN metal gates, and NiGe S/Ds are demonstrated for the first time using a simplified low-temperature process. The highest temperature in the entire fabrication process was 600 °C.

Manuscript received October 26, 2004; revised November 17, 2004. The review of this letter was arranged by Editor B. Yu.

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Digital Object Identifier 10.1109/LED.2004.841462

II. MOS Device Fabrication

The starting substrates are N-type Ge (100) wafers with a resistivity of $2 \sim 5\ \Omega\cdot$cm. After cleaning in a diluted HNO_3 solution and dipping in a diluted HF (DHF) solution, the wafers were loaded in a metal–organic chemical vapor deposition system and annealed in pure NH_3 ambient at 600 °C for 30 s for surface nitridation. Then ∼6 nm HfAlO was deposited at 400 °C, followed by an *in situ* annealing in N_2 ambient at 600 °C for 1 min. The wafers were transferred into a sputtering system with a base pressure of $\sim 1.5 \times 10^{-7}$torr. HfN (∼50 nm) and TaN (∼100 nm) were deposited sequentially at room temperature as a metal gate electrode [9]. The deposited wafers were patterned using conventional photolithography and reactive ion etching procedures. Immediately after dipping in the DHF solution to remove the remaining HfAlO film in the S/D region, the patterned wafers were loaded in the sputtering system again and a Ni film of ∼100 nm was deposited. Because HfN can be etched by DHF, but TaN cannot, a "hole" between S/D and gate was formed due to the lateral etching of the HfN layer of the HfN–TaN gate stack during the DHF dipping, which acts as a spacer to separate the gate and S/D [10], [11]. Each transistor was surrounded by a guard ring, thus can be electrically separated from other devices, as shown in the inset of Fig. 4. The Ni germanidation was performed by rapid thermal annealing (RTA) at 600 °C for 1 min. Then, unreacted Ni was removed by wet etching in RCA1 ($NH_4OH : H_2O_2 : H_2O = 1 : 2 : 5$) solution. Because both the NiGe and Ge substrates will be attacked by the RCA1 solution slowly, the selective etching time should be carefully optimized.

III. Device Characterization and Discussion

Fig. 1 shows the gate capacitance–voltage (*C–V*) characteristics measured at 1 MHz as well as the cross-sectional transmission electron microscope (TEM) image of the TaN–HfN–HfAlO–n-Ge(100) gate stack of the final PSSDT. The TEM picture shows smooth interface between HfAlO and Ge substrate and the physical thickness of the amorphous HfAlO film is ∼5 nm. However, the equivalent SiO_2 thickness (EOT) extracted from the accumulation capacitances is ∼3.8 nm. The well-behaved *C–V* with small hysteresis of 18 mV was observed with no significant frequency dispersion, implying that HfAlO is a potential gate dielectric for Ge MOSFETs.

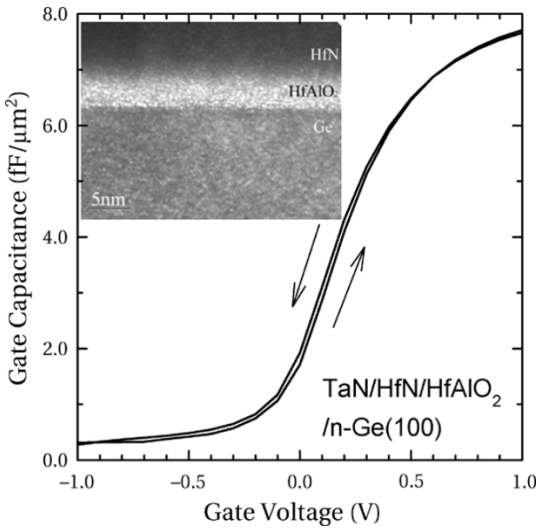

Fig. 1. Capacitance measured at 1 MHz on the fully processed Ge-PSSDT. Inset shows the cross-sectional TEM image of the TaN–HfN-$HfAlO_2$/n–Ge(100) stack.

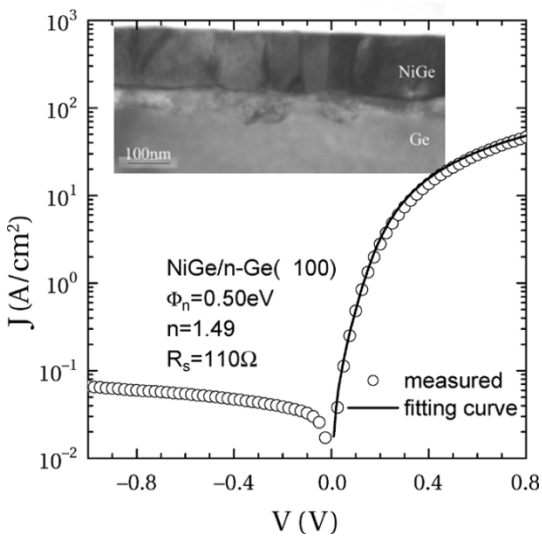

Fig. 2. *I–V* curves of the NiGe–n-Ge(100) diode, the solid line is a fitting curve based on the TE model. Inset is the cross-sectional TEM image of the NiGe–n-Ge(100) contact.

Fig. 2 shows the measured current–voltage (*I–V*) curve of the Schottky diode with NiGe–n-Ge(100) contact and its cross-sectional TEM image. The traditional thermionic emission (TE) model [12] was used to fit the experimental forward current *I–V* data, from which apparent Schottky-barrier height (Φ_n), ideality factor (n) and series resistance (R_s) were extracted to be 0.50 eV, 1.49 and 110 Ω, respectively. The corresponding hole barrier height (Φ_p) can be calculated to be ∼0.16 eV, assuming that the sum of electron and hole barrier heights approximately equals to the Ge gap energy (∼0.66 eV). The reverse leakage current of the Schottky diode at -1 V is $\sim 6 \times 10^{-2}$ A/cm^2. The value is reasonable in view of germanide–Ge Schottky contact [13]. The NiGe layer has a thickness of ∼140 nm, thinner than the expected thickness of 250 nm if the deposited Ni (100 nm) is completely reacted with Ge to form NiGe due to the partially etching of NiGe by the RCA1 solution during the selective etching process. The TEM image shows that there is an intermediate layer between NiGe and Ge substrate with a quite rough interface between the intermediate layer and Ge substrate. Energy dispersive X-ray (EDX) analysis shows that this intermediate layer is a Ge-rich NiGe layer. This may be the main reason for the significantly large ideality factor, the relatively high reverse leakage current and the low apparent barrier height of the NiGe–n-Ge diode compared with the reported value [13]. It is expected that the rectifying property of the NiGe–Ge contact can be improved by reducing this intermediate layer.

Fig. 3 shows the I_d–V_d curves of Ge-PSSDT with channel width/length $= 400/8$ μm. The threshold voltage is ~ -0.41 V from the linear fitting of the $I_{\rm ds}^{1/2} \sim V_g$ curve at $V_{\rm ds} = -0.1$V. The drain current of the device at $V_d = V_g$–$V_{\rm th} = -1$ V is $\sim 6.5\ \mu$A/μm. For comparison, control silicon PSSDTs with PtSi S/D were also fabricated using the similar process and same device size [10], [11], their $I_{\rm d}$–V_d curves are also shown in Fig. 3. For the control Si PSSDT, EOT $= 2.0$ nm, $V_{\rm th} = -0.50$ V and the drain current at $V_d = V_g$–$V_{\rm th} = -1$ V is $\sim 2.6\ \mu$A/μm. Therefore, the Ge device has $\sim 4.8\times$ larger drain drivability

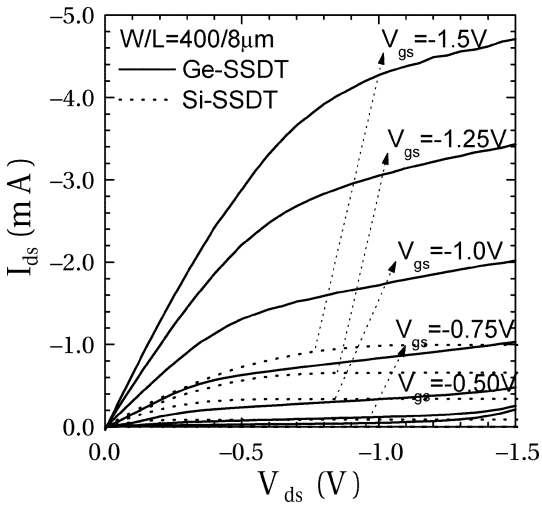

Fig. 3. $I_{\rm d}$–V_d curves of the Ge-PSSDT with NiGe S/D. The channel width and length are 400 and 8 μm, EOT $=\sim 3.8$ nm, $V_{\rm th} =\sim -0.41$ V. For comparison, the $I_{\rm d}$–V_d curves of corresponding Si-PSSDT with PtSi S/D are also shown (dotted lines), which has the same size and EOT $= 2.0$ nm, $V_{\rm th} =\sim -0.50$ V.

than the Si counterpart if they are scaled to the same EOT. Although the drive current improvement can be partly attributed to the fact that Ge has higher hole mobility than Si, the main reason is believed due to the smaller hole barrier between source and channel of Ge-PSSDT (∼0.16 eV) than that of Si-PSSDT ($\Phi_{\rm p} =\sim 0.24 - 0.26$ eV for PtSi/Si [11], [14]). In the case of Si-PSSDT, it is probably difficult to reach the hole barrier height as low as that of Ge [15] because of the large hole band-offset (0.4 eV) or difference of valence electron ionization energy (0.2 eV) between Ge and Si [16]. This is one of the major motivations of Ge-PSSDT. Fig. 4 shows the $I_{\rm d}$–V_g curves of Ge-PSSDT. It shows relatively large off-state current, $I_{\rm off}$. The $I_{\rm on}/I_{\rm off}$ ratio is $10^2 \sim 10^3$, about five orders of magnitude smaller than that of Si-PSSDT. The large $I_{\rm off}$ is mainly caused by the relatively low electron barrier height ($\Phi_{\rm n}$, ∼0.5 eV in our experiment) at the drain/substrate contact that forms a reverse-biased NiGe–n-Ge

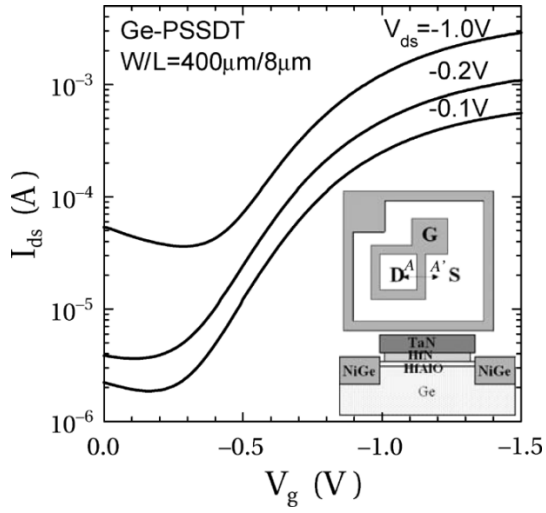

Fig. 4. $I_{\rm d}$–V_g curves of the Ge-PSSDT with NiGe S/D, $V_{\rm ds}$ are -0.1, -0.2, and -1 V, respectively. The $I_{\rm on}/I_{\rm off}$ ratio reaches $10^2 \sim 10^3$. The inset shows schematics of the device layer and cross-sectional structure.

diode. The reverse saturation current of the contact with an area of 1×10^{-4} cm^2 is calculated to be $\sim 4 \times 10^{-6}$ A, close to the value of $I_{\rm off}$ in Fig. 4. Conventional Ge MOSFET with p–n junction S/D suffers from the same problem because the narrow gap energy of Ge also results in large p–n junction leakage [1]–[4]. The large $I_{\rm off}$ can be effectively reduced by using ultrathin germanium on insulator substrate [3] because the contact area can be dramatically reduced.

It has been pointed out that Schottky-barrier heights of metals and germanides on n-Ge are pinned at between 0.54 and 0.61 eV over a wide range of metal work function [13]. Erbium germanide (ErGe) was also used to fabricate Ge-PSSDTs in our experiment and show similar electrical characteristics as displayed in Figs. 3 and 4. The quality of the NiGe film and the NiGe–Ge interface is sensitive to the annealing condition. Furnace annealing at 420 °C results in poorer rectifying property than that after RTA. However, very few data have been reported in the literature about the formation of germanide by solid-state reaction as well as the Schottky-barrier properties of various metal–Ge or germanide–Ge contacts. Systematically studies are still on-going in order to improve the quality of germanide–Ge contact by optimizing the fabrication parameters.

In conclusion, the first germanium PSSDT with HfAlO gate dielectric, HfN/TaN metal gate and NiGe S/D was fabricated using a simplified low temperature process. The drive current is about 4.8× larger than that of the silicon counterpart due to the high hole mobility of Ge and the low hole Schottky-barrier height of the germanide–Ge contact.

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