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ORIGINAL ARTICLE

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A linear programming model for the control wafers downgrading problem

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Abstract This paper considers the control wafers downgrading problem (CWDP) in the wafer fabrication photolithography area. The objective of the research is to minimize the total cost of control wafers, while maintaining the same level of production throughput. For the problem under a pulling control production environment, a linear programming model is presented to set the supply rate of new control wafers and the recycle and downgrading rates so as to minimize the total cost of control wafers. A numerical example is given to illustrate the practicality of the model. The sensitivity of the linear programming model solution to changes in the underlying parameter values is also investigated. The results demonstrate that the proposed model is an effective tool for determining the control wafers downgrading policy.

This paper presents a linear programming model that considers the cost of new control wafers, recycle and downgrading control wafers in wafer fabrication. The proposed model improved the performance of control wafers management, and served as the basis for setting the usage rates of control wafers.

Keywords Control wafers · Downgrading · Linear programming model · Performance · Pull control

List of symbols

TR_n	The actual process quantity of product n
$\mathfrak{R}$	The system throughput quantity in a planning period
π_n	The product mix ratio for product n among all products
γ	The average rework rate in the system
S	The set of product types
TC_{nj}	The number of times of using the jth grade control wafers in the process of product type n
PC_{nj}	The expected amount of the jth grade control wafers needed in the process of product type n
PT	The length of planning period
j	The sequencing grade numbering for control wafers
Z	The total cost of control wafers
A_{0j}	The supply of new control wafers per day
c_{0j}	The new control wafers cost per unit
c_{jj}	The recycle cost in loop j per unit
c_{ij}	The downgrading cost from loop i to loop j per unit
λ_j	The supply rate of control wafers per day
d_j	The demand of control wafers per day
P_{jj}	The recycle ratio
P_{ij}	The downgrading ratio
P_{jD}	The discard ratio
Pr_j	The maximum recycle ratio
Pd_j	The minimum discard ratio

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1 Introduction

Control (monitor) wafers are employed for monitoring machine parameters including a series of precision parameters for the production processes in semiconductor wafer fabrication, and for maintaining manufacturing conditions. Control wafers are not only used to control the machine manufacturing capability, but also to increase the process yield. Each grade of control wafers is repeated for use in the same process until being downgraded or discarded. Any shortage of control wafers may result in a halt of machine operations and as a result may seriously affect the process yield and production planning. To avoid such situations from occurring, a large number of control wafers are usually prepared and stored for use. Consequently, it unnecessarily increases the work-in-process (WIP) level of control wafers. In order to simplify the development of an effective management system, we shall restrict our investigation of control wafers to the photolithography area of the wafer fabrication. In addition, the purpose of this research is to determine the minimum total cost of control wafers and to set the new supply rate of control wafers and the recycle and downgrading rates in each grade.

The rates calculated above can be used as target values for management. In practice, if the rates obtained in the floor are higher than the target values, a production planner can lower the usage rates to meet the target and to minimize the cost. On the other hand, if the actual rates are lower than the target rates, a production planner needs to consider the quality of raw control wafers and monitor the recycle process in order to increase the usage rates to meet the target. If relevant costs change as a result, target values must be recalculated.

For most factories, the WIP level of control wafers are set to 30%–50% of that for normal products [1]. An increase of the current control wafers level would result in an increase in the holding cost but with a decrease in the shortage cost. Therefore, a tradeoff must be made. Most common decisions in current industrial practice often result in maintaining each grade of control wafer at its maximum service level. How to determine the management parameters of control wafers for each grade is important to performance measure for the control wafers downgrading problem (CWDP).

Spearman et al [2] first introduced the concept of the push system and developed the CONWIP pull system. They pointed out that CONWIP system is a suitable pull system in many dynamic environments. Chen and Lee [3] investigated the effect of control/dummy (C/D) wafers with downgrading features on the push and the pull systems. Their result indicated that the pull system is preferable if the machine delay time is the primary concern, whereas the push system leads to better utilization of C/D wafers, and hence can significantly lower C/D wafer WIP level. Chung et al. [4] suggested a due date assignment model of fabs and discussed flow time control parameters for performance evaluation. Kroese and Nicola [5] proposed a two-node tandem Jackson network model, and conducted a simulation study on the arrival and service parameters to estimate the overflow probability in the second buffer. Kumar and Kumar [6] introduced the application of queuing network models to design and analyze semiconductor wafer fabs. They surveyed some of the sequencing rules and released policies used in semiconductor manufacturing. Lin [1] studied the effectiveness of C/D wafers management system with repeated use policy in the furnace area using the pull system. They have assumed, however, that the distribution of C/D wafers quality approximately follows a discrete uniform distribution, and developed a method to obtain the optimal WIP level of C/D wafers.

The purpose of this paper is to obtain the minimum total cost of control wafers. Under the production control of a pulling system, a linear programming model, which considers the inventory level to set the control wafers supply rate for each grade, is proposed.

The remainder of this paper is organized as follows. Section 2 introduces the control wafers loop system. Section 3 describes the construction of the linear programming model. In Sect. 4, a numerical example is investigated using the proposed linear programming model. The results are analyzed to show the effectiveness of the proposed model. In Sect. 5, some concluding remarks are made.

2 An overview of the control loop system

In the wafer fabrication photolithography field, control wafers are utilized for monitoring and measuring the particle content, measuring photo-resistant coat thickness and uniformity, checking critical dimension, examining alignment and inspecting exposure [7]. The diagram of the operation of control wafers is depicted in Fig. 1. The use of control wafers can assure that the manufacturing process operations in photolithography satisfy the required manufacturing specifications. The control wafers are repeatedly used until their immaculacy and thickness no longer conform to the process requirement. After passing through the in-use stage, the surface of control wafers will be contaminated or damaged. If the contamination of control wafers is too serious that they cannot recover from their clarity, the reuse of control wafers will further contaminate the clarity of machines and will no longer accomplish the function of monitoring. Therefore, for control wafers that do not conform to the process requirements, they are downgraded or discarded. To avoid contamination to the factory machines due to misusing control wafers, managers often apply a control wafers supply rule to different machines according to the requirement of processing circumstances, such as the required immaculacy degree. In this paper, we will base the surface condition on the control wafers to judge whether the control wafers should be recycled, downgraded or discarded. The immaculacy degree is set to be grade one if the particle number is less than 1 in 1 m^3, grade two if less than 10 in 1 m^3, grade three if less than 100 in 1 m^3, and grade four if less than 1000 in 1 m^3.

The process of control wafers in a photolithography machine is similar to that of normal products, and the main purpose of control wafers is to test and monitor relevant process parame-

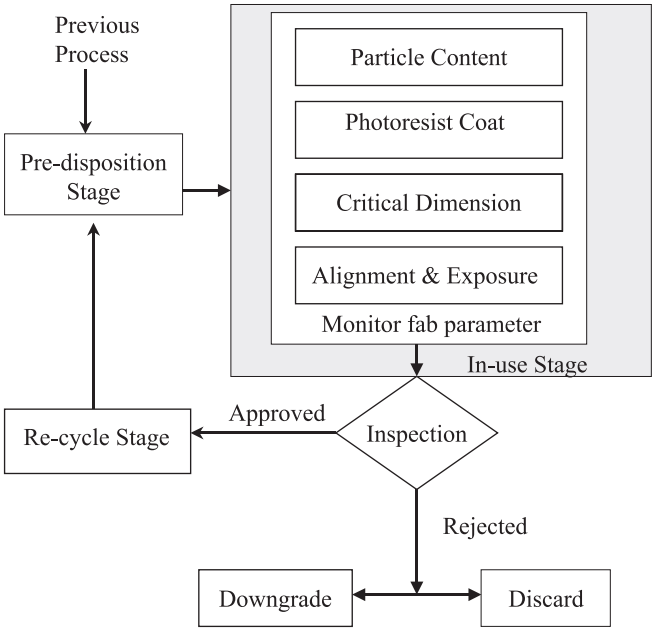


Fig. 1. The operation of a control wafer

ters. If the observed parameters conform to the parameter setting, products can be processed. On the other hand, if the observed parameters no longer conform to the setting, fab parameters must be adjusted first. The process of control wafers is shown in Fig. 2. In a typical photolithography machine, ultraviolet (UV) light from a light source passes through lenses and refracts to masks. UV light next passes through the masks and onto the wafer stage, while control wafers are put on the wafer stage to examine the relevant parameters of the process.

The loop system concept may be conveniently applied to illustrate the PUR process of control wafers, and is largely employed in manufacturing systems, and computer/communication networks. The loop system and analysis presented here were originally developed by Jackson [8], and a tandem Jackson related network model was developed by Kroese and Nicola [5]. In general, the reuse status of control wafers can be divided into (1) pre-disposition, (2) in-use, and (3) recycle [3]. This is termed the PUR process. The in-use control wafers in the photolithography area provide functions for product monitoring, equipment monitoring, breakdown and recovery monitoring, and preventive maintenance [1]. Control wafers can be categorized into several grades depending on their quality, that is, the amount of particle content on them.

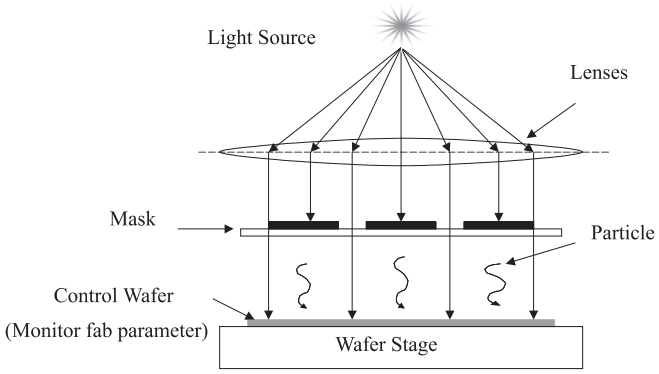


Fig. 2. A simple typical diagram of a control wafer's position in a machine

The diagram of multi-loop control wafers system is depicted in Fig. 3. In Fig. 3, loop 0 contains new control wafers, loop D is the discard wafers collection, and A_{0j} is the new wafers supply rate to each loop j. Each loop j can be considered as a neuron, and the jth loop can be considered as the jth grade of the control wafers process. The demand rate of jth grade control wafers is d_j, the recycle rate is P_{jj}, the downgrading rate is P_{ij} (for $i < j$), the discard rate is P_{jD}, and the supply rate is λ_j. Because control wafers are used during the fabrication of regular products, certain amount of control wafers must be consumed each time the normal wafer products are produced. Therefore, the demand of control wafers is closely related to the system throughput, product mix ratio , and expected depletion amount of the jth grade control wafers.

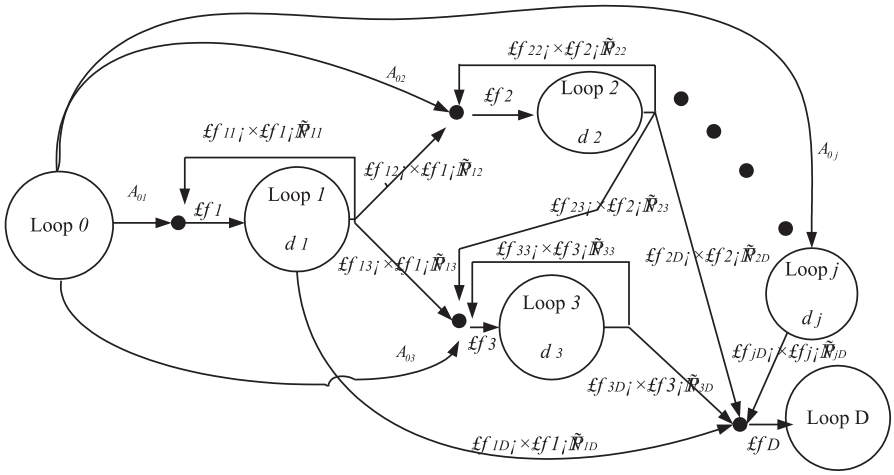
The model developed here is based on the following assumptions:

1. The monthly throughput target is known
2. The product mix is known
3. The control wafers demand is spread evenly throughout the planning period so that the demand rate is reasonably constant
4. A shortage of control wafers is not allowed
5. Each PUR process consists of three stages of operation
6. The control wafers are classified into c grades
7. The maximum recycle ratio of control wafers for each grade is known
8. The minimum discard ratio of control wafers for each grade is known

3 A linear programming model

In the following, we develop a linear programming model to determine the supply rate, the recycle rate, and the downgrading rate for each grade of control wafer. The proposed model can be divided into three phases: (1) Calculating control wafers demand rate, (2) Analyzing control wafers supply rate and cost, and (3) Formulating the control wafers downgrading problem. The demand for each grade of control wafers depends on the through-

Fig. 3. The multiple loop control wafers system



put target, the product mix ratio of normal products, and the rework of the workstation that processes control wafers.

A multi-loop system shall supply new control wafers when the total quantity of the recycle control wafers and the downgrading control wafers are insufficient in the loop. Under the minimum discard ratio, the supply rate is equal to the demand rate, and we can calculate the supply rate of new control wafers, the recycle rate and the downgrading rate for each grade of control wafers. The total cost of control wafers for each grade is calculated by adding the costs of new control wafers, recycle control wafers, and downgrading control wafers.

Finally, the CWDP is formulated as a linear programming model, and its objective is to find the minimum total cost of control wafers. The principal constraint is that the supply rate for each grade of control wafer must equal the sum of the new supply rate of control wafers, the recycle supply rate and the downgrading supply rate. The procedures for the four phases will be described in the next sections.

3.1 Control wafers demand of grade j

Note that in a stabilized manufacturing system, the expected arrival rate equals to the expected throughput rate. In addition, in the planning period, the throughput level equals to the release quantity. Therefore, with the throughput target, the product mix ratio and the rework rate for normal products, we can calculate the actual process quantity in the planning period:

$$TR_n = \Re \times \pi_n \times (1+\gamma)\,, \quad \text{for each } n\,. \tag{1}$$

Control wafers can be categorized into several grades depending on their quality, that is, the amount of particle content in them. For every grade of control wafers, no matter what product type it is producing or what layer it is on, the PUR process is the same. The demand rate for grade j control wafers is calculated as follows:

$$d_j = \sum_{n\in S} TR_n \times TC_{nj} \times PC_{nj} \times \frac{1}{PT}\,, \quad j = 1, 2, \ldots, c\,. \tag{2}$$

3.2 Control wafers supply of grade j

The loop system of control wafer is constructed by a pulling control system, downgrade supply rate and PUR process procedures. In the jth loop, the supply and depletion of control wafers continue repeatedly, and a balanced production and exhaustion loop system is adequate to solve CWDP. The basic structure of the control wafers PUR process and pull control is depicted in Fig. 4.

In Fig. 4, the loop consists of three stages, and each stage consists of one machine for processing. X_{j1} represents the pre-disposition stage, X_{j2} represents the in-use stage, and X_{j3} represents the recycle stage. At the pre-disposition stage, operations must be completed to make the control wafers complied with the manufacturing condition before they can be used. At the in-use

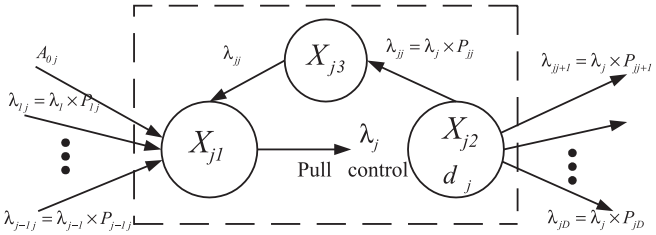


Fig. 4. The relationship between pull control and PUR process in the jth loop system

stage, control wafers are employed in wafer fabrication to monitor and control some machine functions. After control wafers pass through the pre-disposition and in-use stages, they either enter the recycle state, are downgraded, or are discarded. In the jth loop, the new control wafers supply rate is A_{0j}, the recycle supply rate is λ_{jj}, the downgrading supply rate is λ_{ij} (for $i < j$), downgrading leave rate is λ_{jk} (for $j < k$), and the discard rate is λ_{jD}. If these control wafers enter the recycle state, they will be repeatedly used and remain in the PUR process.

When the jth loop declares a need of control wafers, control wafers can be supplied from the pre-disposition stage. The pre-disposition stage (X_{j1}) supplies recycle or downgrading control wafers to meet the demand. If control wafers are not sufficient to meet the demand, the system can pull new control wafers for use. Therefore, in a stabilized system, the arrival rate of control wafers is equal to the leaving rate of control wafers. By equalizing the supply rate to the demand rate derived in Eq. 3, we can determine the supply rate of new control wafers, the recycle supply rate and the downgrading supply rate. Therefore, the supply rate for control wafers is calculated as follows:

$$\lambda_j = A_{0j} + \lambda_j P_{jj} + \sum_{i=1}^{j-1} \lambda_i P_{ij}\,, \quad j = 1, 2, \ldots, c\,. \tag{3}$$

The total cost of control wafers consists of the purchase cost for new control wafers, recycle process cost and downgrading process cost. New control wafers have the highest clarity and are suitable for all classes of production. As a result, the cost of new control wafers is the highest. Recycle control wafers are produced by the single loop of the same grade. The grades must be considered in determining the cost. Downgrading control wafers are transferred from a higher grade to a lower grade, and the relationship between the two grades must be studied to set the cost. Control wafers of a higher grade have higher recycle and downgrading costs, and control wafers of the same grade have the same recycle/downgrading costs. The costs of new, recycle and downgrading control wafers will be discussed in the next section.

3.3 Formulation of the control wafers downgrading problem

In this paper, a production planner's objective is to minimize the total cost of control wafers in the system and to determine the optimal supply rate of control wafers in the jth grade. A multi-loop system must supply enough control wafers for use in time, and shortage is not allowed. The operative constraints are as follows.

First, the demand rate of control wafers is equal to the supply rate of control wafers. The demand rate of control wafers is calculated by Eqs. 1 and 2. Second, as previously discussed, the supply rate of control wafers is equal to the supply rate of new control wafers plus the control wafers recycle rate and downgrade rates from upstream loops. Third, the sum of all ratios in the jth grade are equal to one. Fourth, the recycle ratio is less than a positive real number. Fifth, the discard ratio is more than a positive real numbers. Sixth, all supply rates and ratios are nonnegative real numbers.

The objective and constraints are as follows:

$$\text{Minimize} \quad Z = \sum_{j=1}^{c} c_{0j} A_{0j} + \sum_{j}^{c} \sum_{i=1}^{j} c_{ij} \lambda_i P_{ij} \tag{4}$$

$$\text{subject to} \quad d_j = \lambda_j \,, \quad j = 1, 2, \ldots, c \tag{5}$$

$$\lambda_j = A_{0j} + \sum_{i=1}^{j} \lambda_i P_{ij} \,, \quad j = 1, 2, \ldots, c \tag{6}$$

$$\sum_{j \geqslant i}^{c} P_{ij} + P_{jD} = 1 \,, \quad j = 1, 2, \ldots, c \tag{7}$$

$$P_{jj} \leqslant Pr_j \,, \quad j = 1, 2, \ldots, c \tag{8}$$

$$P_{jD} \geqslant Pd_j \,, \quad j = 1, 2, \ldots, c \tag{9}$$

where all variables are nonnegative. (10)

3.4 Strategy discussion

In order to justify the applicability of the proposed linear programming model, we consider some strategies to investigate the effects of different downgrading level policy on the system, and to optimize the control wafers managing strategy. The basic information for four situations (1) without recycling and downgrading, (2) with recycling but not downgrading, (3) downgrading with one level, and (4) downgrading with multi-levels, are presented here. In the first model, the initial supply node is considered, and the downgrading level is 0. That is, only new control wafers are supplied, and neither recycling nor downgrading is permitted. In the second model, the downgrading level is also 0. The model consists of new and recycled control wafers in the system, but downgrading is not allowed. In the third model, the downgrading level is 1. The model has new, recycle, and downgrading control wafers in the system. However, downgrading is only allowed for one level. Finally, the fourth model consists of multi-loops and the downgrading level is c. The model is similar to the third model, but the control wafers of a specific level can be downgraded to several other levels.

Strategy I: Without recycling and downgrading

In Strategy I, we let the supply node be loop 0, and loop 0 contains only new control wafers. The recycle and the downgrading events do not happen in this model. The model is matched with a pulling control system and the demand rate equals the supply. The constraint of Eq. 6 for this model becomes

$$\lambda_j = A_{0j} \,, \quad j = 1, 2, \ldots, c \,. \tag{11}$$

Strategy II: With recycling but not downgrading

In Strategy II, the downgrading event does not happen in the model, but the recycle event does. The model is also matched with a pulling control system. The supply rate is calculated by adding up new control wafers supply rate and the recycle supply rate. Equation 6 for this model becomes

$$\lambda_j = A_{0j} + \lambda_j P_{jj} \,, \quad j = 1, 2, \ldots, c \,. \tag{12}$$

Strategy III: Downgrading with one level

In Strategy III, both recycle and downgrading events happen in the model. However, downgrading is permitted for only one level. The supply rate is calculated by adding the new control wafers the supply rate, the recycle supply rate and the downgrading supply rate. The constraint of Eq. 6 for this model becomes

$$\lambda_j = A_{0j} + \lambda_j P_{jj} + \lambda_{j-1} P_{j-1\,j} \,, \quad j = 1, 2, \ldots, c \,. \tag{13}$$

Strategy IV: Downgrading with multi-levels

In Strategy IV, both recycle and downgrading events happen in the model. The multi-loop model considers all events and the interaction effect among loops. The model is matched with a pulling control system, and the supply rate is calculated by adding the new control wafers supply rate, the recycle supply rate and the downgrading supply rate. The constraint is as in Eq. 6.

4 Numerical example

The linearly programming model is implemented by using the software LINDO 5.01 to solve the CWDP. Each strategy aims to determine the minimum total cost of control wafers including the new control wafers cost, recycle process cost and downgrading process cost.

4.1 Basic input information

To investigate the effect of the management system on the planning, actual data is taken from a wafer fabrication factory located in the Science-Based Industrial Park in Hsinchu, Taiwan.

1. Production information. In our production system, we have five products A, B, C, D, and E. Product A and B are logic, while product C, D and E are memory products. The process of each product is different and unique.
2. Workstation information. There are 83 workstations in our production system.
3. Master production scheduling (MPS) information. The product mix for product A, B, C, D, and E is 5, 7, 3, 4, and 1, respectively. The monthly output target ($\mathfrak{R}$) is 630 lots. In order to achieve the throughput target and the mix, CONWIP rule is adopted and the WIP level of normal wafers for

Table 1. The number of times for control wafers demand for each lot of normal product and each grade

	A	B	C	D	E
Grade 1	6	4	6	7	5
Grade 2	5	6	5	6	9
Grade 3	9	7	8	6	5
Grade 4	3	4	6	5	3

Table 2. The unit cost of c_{0j}, c_{jj} and c_{ij} of control wafers in each grade

	C_{ij}				
	$i=0$	$i=1$	$i=2$	$i=3$	$i=4$
$j=1$	100	80			
$j=2$	100	70	70		
$j=3$	100	60	60	60	
$j=4$	100	50	50	50	50

the system is set to be 270 lots. The planning period (PT) is 28 days, and the rework rate (γ) is set to be zero.

4. Machine data for control wafers. In the photolithography area, process engineers disaggregate control wafers into four grades in the process. The depletion of control wafers is related to the amount of product processed. In addition, the relationship between control wafer depletion and the corresponding workstation is known. The number of times used for grading j control wafers for each lot of each product type, TC_{nj}, is shown in Table 1, and the usage per lot (PC_{nj}) is a constant (i.e., 1 piece).
5. Cost types of the control wafers. The costs for using control wafers include new control wafer cost, recycle cost and downgrading cost. The unit cost of control wafers for each cost type and for each grade is shown in Table 2.
6. PUR process. In each loop j, the PUR process consists of three stages of operation, and each stage is represented by a workstation.
7. The maximum recycle ratio (Pr_j) for each grade of control wafer is set to be 0.80.
8. The minimum discard ratio (Pd_j) for each grade of control wafers is set to be 0.10.

4.2 Experimental result and sensitivity analysis

The results of the four strategies are shown in Tables 3, 4, 5 and 6. The optimum costs are calculated for the model and the costs are compared using different downgrading levels, as shown in Table 7.

Table 4. The rates for Strategy II

Loop j	d_j	A_{0j}	P_{jj}	P_{jD}
$j=1$	123	24.6	0.80	0.20
$j=2$	129	25.8	0.80	0.20
$j=3$	165	33.0	0.80	0.20
$j=4$	95	19.0	0.80	0.20

Table 5. The rates for Strategy III

Loop j	d_j	A_{0j}	P_{1j}	P_{2j}	P_{3j}	P_{4j}
$j=1$	123	60.70	0.51			
$j=2$	129	0.00	0.39	0.62		
$j=3$	165	0.00	0.00	0.28	0.78	
$j=4$	95	0.00	0.00	0.00	0.12	0.80
$j=D$			0.10	0.10	0.10	0.20

Table 6. The rates for Strategy IV

Loop j	d_j	A_{0j}	P_{1j}	P_{2j}	P_{3j}	P_{4j}
$j=1$	123	60.70	0.51			
$j=2$	129	0.00	0.37	0.64		
$j=3$	165	0.00	0.00	0.26	0.80	
$j=4$	95	0.00	0.02	0.00	0.10	0.80
$j=D$			0.10	0.10	0.10	0.20

For the first strategy, new wafers are used for each loop, and no recycling or downgrading is allowed. For example, in loop 1, as shown in Table 3, 123 control wafers are demanded, and all are from new control wafers. Once they are used, they will be discarded. Therefore, $P_{jD}=1$. As a result, the total cost for this strategy is the highest.

For the second strategy, each loop requires new wafers. The recycle rate and the discard rate are 0.80 and 0.20, respectively, for each loop. Since each loop can acquire new wafers and no downgrading is allowed, the total cost is the second highest.

For the third strategy, new wafers can only be introduced in the first loop. For other loops, only recycle and downgrading control wafers can be used. In addition, downgrading is permitted for one level. For instance, control wafers of loop 1 can only be downgraded to loop 2, but not loop 3 or 4, etc. As shown in Table 5, 60.70 new control wafers are used in the first loop, and the recycle rate of loop 1 is 0.51. Some control wafers of loop 1

Table 3. The rates for Strategy I

Loop j	d_j	A_{0j}	P_{jD}
$j=1$	123	123	1
$j=2$	129	129	1
$j=3$	165	165	1
$j=4$	95	95	1

Table 7. Costs of control wafers

Strategies	$\sum c_{0j}A_{0i}$	$\sum c_{jj}\lambda_j P_{jj}$	$\sum c_{ij}\lambda_i P_{ij}$	Z
Strategy I	51 200.00	0.00	0.00	51 200.00
Strategy II	10 240.00	26 816.00	0.00	37 056.00
Strategy III	6070.00	22 158.80	6549.54	34 778.34
Strategy IV	6070.00	22 520.96	6143.10	34 734.06

Table 8. Effects of d_j, Pr_j and Pd_j on the CWDP

Changing parameters			$\sum c_{0j} A_{0i}$	$\sum c_{jj} \lambda_i P_{ii}$	$\sum c_{ij} \lambda_i P_{ij}$	Z
The multi-loop model	d_j	111, 116, 149, 86	5480.00	22 330.39	6330.71	34 141.10
		123, 129, 165, 95	6070.00	22 520.96	6143.10	34 734.06
		135, 142, 182, 105	6690.00	23 907.30	4751.12	35 348.12
	Pr_j	0.72	7140.00	19 569.24	8238.70	34 947.94
		0.80	6070.00	22 520.96	6143.10	34 734.06
		0.88	5310.00	25 224.97	4047.00	34 581.97
	Pd_j	0.09	5653.00	22 944.96	6052.53	34 650.49
		0.10	6070.00	22 520.96	6143.10	34 734.06
		0.11	6487.00	22 097.21	6233.30	34 817.51

are downgraded to loop 2, with a downgrading rate of 0.39. Since they cannot be further downgraded, the unsuitable control wafers are discarded with a discard rate of 0.10.

For Strategy IV, downgrading is permitted without restriction in levels. From Table 6, we can see that control wafers of loop 1 can be downgraded to loop 4 with a downgrading rate of 0.02. Since this strategy best uses each piece of control wafer, its total is the lowest, with \$ 34, 734.06 per day. Based on the results, we find that the proposed mutli-loop model performs quite well in setting the recycle ratio, the downgrading ratio, and the new control wafers depletion rate for each control wafer grade. However, notice that the results of Strategy III and IV are almost identical. Therefore, Strategy III is nearly optimal.

As discussed before, the rates obtained under the four strategies can be used as target values for management. In practice, if the actual rates obtained on the floor are higher than the target rates, we can lower the usage rates to meet the target and minimize the cost. For example, if the actual recycle rate for loop 1 is 0.60 (while the target rate is 0.51 under Strategy III and IV), we can downgrade controls wafers of loop 1 more often and still have a low cost. However, if the actual rates are lower than the target rates, we need to further consider whether raw control wafers of a higher quality should be used. Also, the recycle process probably needs to be monitored in order to increase the usage rates and to meet the target. For instance, if the recycle rate is 0.30 in loop 1 (while the target rate is 0.51 under Strategy III and IV), we have to check why control wafers cannot be recycled more often. Could it be simply the policy of not recycling too often, or could it be that the particle content of the control wafers used is too high to meet the recycle requirement? A comprehensive study should be done in order to make the correct actions toward meeting the target rates. If relevant costs change as a result, target rates must be recalculated.

Now, consider a situation in which only one of d_j, Pr_j and Pd_j changes by a fixed proportion while the other parameters remain unchanged. The following sensitivity measures are then calculated for 10% changes in the parameters on either side. Table 8 summarizes these results. Based on the sensitivity analysis, we can infer the following:

1. An increase in demand rate d_j or minimum discard ratio Pd_j, or a decrease in the maximum recycle ratio Pr_j causes increases in the total new control wafers cost.
2. An increase in demand rate d_j or maximum recycle ratio Pr_j or a decrease in minimum discard ratio Pd_j causes increases in the total recycle cost.
3. An increase in the minimum discard ratio Pd_j or a decrease in the demand rate d_j or maximum recycle ratio Pr_j causes increases in the total downgrading cost.
4. The total cost Z increases with an increase in the demand rate d_j or minimum discard ratio Pd_j, or a decrease in the maximum recycle ratio Pr_j. The total cost Z is more sensitive to the parameter d_j than the others.

5 Conclusions

A production management system for CWDP poses new challenges to wafer fabrication and proposing a proper downgrading rule of control wafers is an important task. The use of control wafers is closely related to many critical factors such as the production throughput, product mix, and priority mix. In this paper, a multi-loop model is proposed to determine the supply rate, the recycle ratio, and the downgrading ratio for each control wafer grade. A numerical experiment demonstrates that applying the proposed model can minimize the total cost. In addition, sensitivity analysis is performed to examine the effect of the parameters. According to these results, the proposed model is more sensitive with respect to the demand rate d_j than the others. The analysis provided in this study can be very useful for managers in deciding whether they should have a downgrading policy. For future research, we can focus on stochastic nature of demand that satisfy the minimum cost as well as achieving the manufacturers' planning target. Also, a model for a work-in-process level of control wafers may be established.

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