Design and Implementation of Sensorless Capacitor Voltage Balancing Control for Three-Level Boosting PFC

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***Abstract*—Compared with the conventional boosting PFC converter, the three-level boosting PFC converter has two cascaded switches and two cascaded capacitors across the dc-side voltage. Two capacitor voltages may be different due to their mismatched equivalent series resistance, their mismatched capacitance, and the mismatched conducting time of the corresponding switches. It follows that the controller needs to sense the capacitor voltages to balance both capacitor voltages. In this paper, the sensorless capacitor voltage balancing control (SCVBC) without sensing the capacitor voltages is proposed, and the total number of the feedback signals is saved. The proposed SCVBC is digitally implemented in an FPGA-based system. The provided simulated and experimental results also demonstrate the proposed SCVBC.**

***Index Terms*—Sensorless control, voltage-balancing control.**

I. Introduction

TO REDUCE the power transmission loss and increase the system stability, more and more power-electronics products are forced to include the power factor correction (PFC) function [1]. Generally speaking, the PFC function includes shaping the ac-side current waveform and regulating the dc-side voltage. Due to the characteristics of the continuous current, the boost-derived PFC converters have been widely used to achieve the desired PFC function [2].

For the conventional boost dc/dc converter, the single switch needs to withstand the dc output voltage when the single switch blocks. As shown in Fig. 1, two cascaded switches and two cascaded capacitors are connected together in the three-level boosting dc/dc converter. When one of the switches conducts and the other blocks, the blocking switch needs to withstand only half dc output voltage if both capacitor voltages are balanced. If not balanced, one of the capacitor voltages may be larger than the breakdown voltage of the switch, which would contribute to make damage to the switch.

It is noted that the inductor voltage in the three-level boost dc/dc converter has three levels, which makes the three-level boosting dc/dc converter to have smaller inductor current ripple than the boost converter under the same switching frequency. Therefore, the three-level boost converters are often used in the high-voltage-ratio applications [3], such as the fuel cell applications [4], [5] and the grid-connected applications [6]–[8].

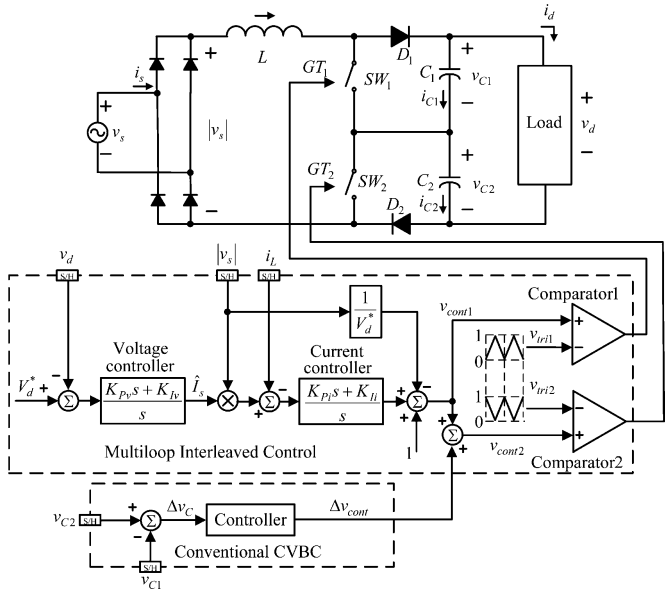

Fig. 1. Three-level boosting PFC converter with multiloop feedforward control and the conventional capacitor voltage balancing control loop.

In addition, the high-withstanding-voltage semiconductor switches often have higher cost and the larger drain-source resistances than the low-withstanding-voltage ones. Thus, the three-level boost converter has the additional advantages of the low switching loss and the high efficiency [9].

The three-level boosting PFC converter was first proposed in [9] by connecting the diode rectifier to the three-level boosting dc/dc converter as shown in Fig. 1 [9]–[14].

In [13], the multiloop interleaved control combining the multiloop control and the interleaved PWM scheme was first proposed to control the three-level boosting PFC converter. As shown in Fig. 1, the multiloop control includes the feedforward loop, the inner current loop, and the outer voltage loop.

The three single-phase three-level boosting PFC converter in Delta connection are used to achieve the three-phase PFC function with the ability of redundancy [14].

However, the balance between two capacitor voltages should be noted. In practice, the mismatched capacitances and the mismatched equivalent series resistance (ESR) would result in

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the voltage imbalance. Therefore, the control of the three-level boosting converter needs to balance both capacitor voltages.

In the literature [7], [8], [11], [12], [15], the voltage balancing control loop for three-level boosting converters can be found. In fact, the other voltage balancing control can be found in the controls of the half-bridge PFC converter [16], [17] and the multilevel inverter [18], [19]. All the methods need to sense capacitor voltages to detect the voltage imbalance and yield the desired voltage balancing function. The multiloop interleaved control with conventional capacitor voltage balancing control (CVBC) is also shown in Fig. 1. One control signal is generated by the multiloop control, and the other control signal is yielded by CVBC with sensing the capacitor voltages. For the three-level boosting dc/dc converter, a voltage balancing control method with sensing only inductor current was first proposed in [20].

In this paper, the concept in [20] is extended to the three-level boosting PFC application and the proposed controller is named the sensorless capacitor voltage balancing control (SCVBC). The voltage imbalance between two capacitor voltages is skillfully detected by sensing the inductor current. The detailed analysis and the design rule of the proportion-type voltage balance controller are also provided. It follows that sensing individual capacitor voltage is not required, and at least one voltage sensor is saved. The provided simulation and experimental results show the effectiveness of the proposed SCVBC.

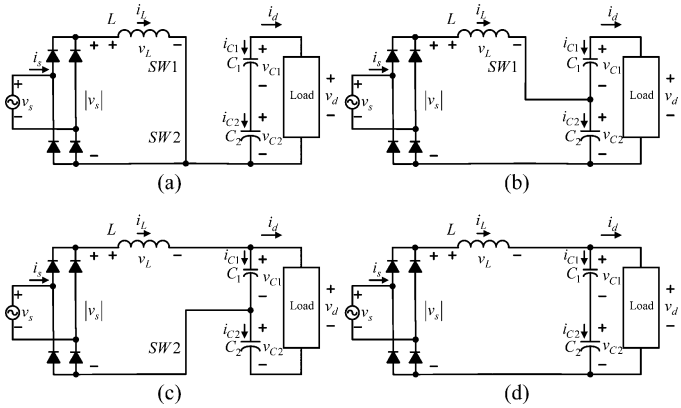

Fig. 2. Possible switching states in the three-level boosting PFC converter: (a) state 1, (b) state 2, (c) state 3, and (d) state 4.

TABLE I
CAPACITOR CURRENTS IN EACH STATE

		state 1	state 2	state 3	state 4
$2 > v_{cont1} + v_{cont2} > 1$	i_{C1}	$-i_d$ (<0)	$-i_d$ (<0)	$i_L - i_d$ (>0)	
	i_{C2}	$-i_d$ (<0)	$i_L - i_d$ (>0)	$-i_d$ (<0)	
$1 > v_{cont1} + v_{cont2} > 0$	i_{C1}		$-i_d$ (<0)	$i_L - i_d$ (>0)	$i_L - i_d$ (>0)
	i_{C2}		$i_L - i_d$ (>0)	$-i_d$ (<0)	$i_L - i_d$ (>0)

II. THREE-LEVEL BOOSTING PFC CONVERTER

From Fig. 1, the input ac voltage $v_s = \hat{V}_s \sin(2\pi f t)$ is assumed to be a sinusoidal function with a peak amplitude $\hat{V}_s$. Through the diode rectifier, the input voltage of the three-level boosting converter can be expressed with the rectified voltage $|v_s|$. By assuming that the switching frequency f_s is much larger than the line frequency f, the control signals $v_{\rm cont1}$ and $v_{\rm cont2}$ can be regarded as two constants within the switching period $T_s = 1/f_s$. In addition, the ideal inductor and the ideal capacitors are assumed. That is, the inductor resistance and the capacitor resistances are assumed to be zero.

In Fig. 1, two triangular signals $v_{\rm tri1}$ and $v_{\rm tri2}$ are interleaved by 180°. The conventional multiloop control generates the control signal $v_{\rm cont1}$, and then, the gate signal GT_1 is generated from the comparison of the control signal $v_{\rm cont1}$ and the triangular signal $v_{\rm tri1}$.

After sensing both capacitor voltages, the voltage imbalance is detected and the conventional CVBC generates the compensation signal $\Delta v_{\rm cont}$. Then, the other control signal $v_{\rm cont2}$ is obtained by adding the compensation signal $\Delta v_{\rm cont}$ to the control signal $v_{\rm cont1}$. The gate signal $\rm GT_2$ is obtained from the comparison of the control signal $v_{\rm cont2}$ and the triangular signals $v_{\rm tri2}$.

Due to the input inductor L and two diodes D_1 and D_2 in the three-level boosting PFC converter, both switches can be conducting at the same time without the concern of the short-circuit damage. As plotted in Fig. 2, there are four switching states in the three-level boosting PFC converter.

As shown in Fig. 2(a), both switches turn ON in the switching state 1. Thus, the inductor voltage v_L in the three-level boosting PFC converter equals the rectified input voltage $v_L = |v_s|$ and both capacitors supply energy to the load $i_{C1} = i_{C2} = (-i_d) < 0$.

In the switching state 2 in Fig. 2(b), the top switch turns ON and the bottom switch turns OFF. The resulting inductor voltage v_L equals the rectified input voltage $|v_s|$ minus the bottom capacitor voltage $v_L = |v_s| - v_{C2}$. Additionally, the capacitor C_1 supplies energy to the load $i_{C1} = (-i_d) < 0$, but the capacitor C_2 stores the energy from the input voltage $i_{C2} = (i_L - i_d) > 0$.

Similarly, the resulting inductor voltage in Fig. 2(c) equals the rectified input voltage minus the top capacitor voltage $v_L = |v_s| - v_{C1}$. In the switching state 3, the top capacitor C_1 is charged $i_{C1} = (i_L - i_d) > 0$, but the bottom capacitor C_2 is discharged $i_{C2} = (-i_d) < 0$.

When both switches turn OFF in Fig. 2(d), the resulting inductor voltage equals the rectified input voltage minus the output voltage $v_L = |v_s| - v_d = |v_s| - v_{C1} - v_{C2}$. The rectified input voltage $|v_s|$ supplies the load current and charges both capacitors simultaneously $i_{C1} = i_{C2} = (i_L - i_d) > 0$.

All the capacitor currents in various switching states are tabulated in Table I.

The behavior of the three-level boosting converter can be divided into two cases as shown in Fig. 3. In the case of $2 > v_{\rm cont1} + v_{\rm cont2} > 1$, two switches may conduct at the same time within the switching period T_s and there are switching state 1, state 2, and state 3.

In the other case of $1 > v_{\rm cont1} + v_{\rm cont2} > 0$, only switching state 2, state 3, and state 4 exist.

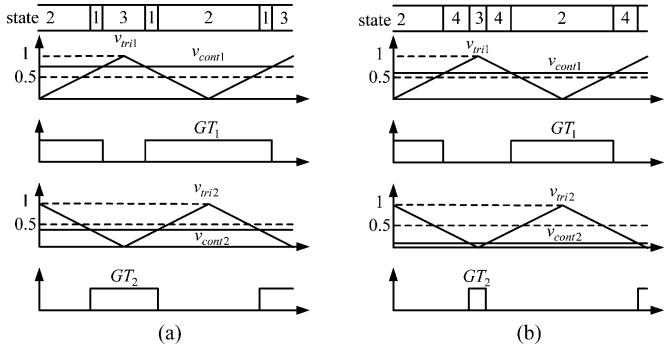

Fig. 3. Behavior of the three-level boosting converter. (a) $2 > v_{\rm cont1} + v_{\rm cont2} > 1$and (b) $1 > v_{\rm cont1} + v_{\rm cont2} > 0$.

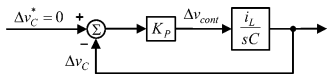

Fig. 4. Equivalent voltage balancing loop with the conventional CVBC.

In the case of $2 > v_{\rm cont1} + v_{\rm cont2} > 1$ in Fig. 3(a), the conducting times of the switching state 2 and the switching state 3 are $(1 - v_{\rm cont2})T_s$ and $(1 - v_{\rm cont1})T_s$, respectively. The remaining time for the switching state 1 is $(v_{\rm cont1} + v_{\rm cont2} - 1)T_s$. Therefore, the average capacitor currents $\langle i_{C1}\rangle_{Ts}$ and $\langle i_{C2}\rangle_{Ts}$ within switching period T_s can be obtained by

$$\langle i_{C1}\rangle_{Ts} = -i_d + (1 - v_{\rm cont1})i_L \tag{1}$$

$$\langle i_{C2}\rangle_{Ts} = -i_d + (1 - v_{\rm cont2})i_L. \tag{2}$$

Similarly, for the other case of $1 > v_{\rm cont1} + v_{\rm cont2} > 0$ in Fig. 3(b), the conducting times of the switching state 2 and state 3 are $v_{\rm cont1}T_s$ and $v_{\rm cont2}T_s$, respectively. The remaining time for the switching state 4 is $(1 - v_{\rm cont1} - v_{\rm cont2})T_s$. After calculations, it can be found that the average capacitor currents $\langle i_{C1}\rangle_{Ts}$ and $\langle i_{C2}\rangle_{Ts}$ have the same equations as (1) and (2).

Thus, in both cases, the difference between two average capacitor currents is obtained from (1) and (2)

$$\langle i_{C1}\rangle_{Ts} - \langle i_{C2}\rangle_{Ts} = (v_{\rm cont2} - v_{\rm cont1})i_L = \Delta v_{\rm cont} i_L. \tag{3}$$

It follows that the voltage imbalance $\Delta v_C = v_{C1} - v_{C2}$ can be expressed as

$$\Delta v_C(s) = \frac{1}{s}\frac{\Delta v_{\rm cont}}{C} i_L \tag{4}$$

where $\Delta v_{\rm cont} = v_{\rm cont2} - v_{\rm cont1}$.

The equivalent voltage balancing loop with the conventional CVBC is plotted in Fig. 4 where the proportional controller (i.e., P controller) with the parameter K_P is used. Thus, the closed-loop transfer function of the voltage imbalance $\Delta v_C(s)$ becomes

$$\frac{\Delta v_C(s)}{\Delta v_C^*(s)} = \frac{\frac{K_p}{C} i_L}{s + \frac{K_p}{C} i_L}. \tag{5}$$

Because that (5) is a first-order response with zero steady-state error, the voltage imbalance would be well regulated to the zero voltage imbalance $\Delta v_C^* = 0$. Therefore, the design of the conventional CVBC with simple P controller is able to balance the capacitor voltages.

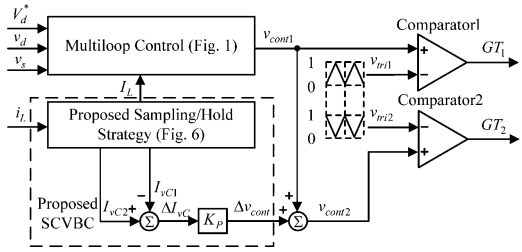

Fig. 5. Multiloop interleaved control with the proposed SCVBC.

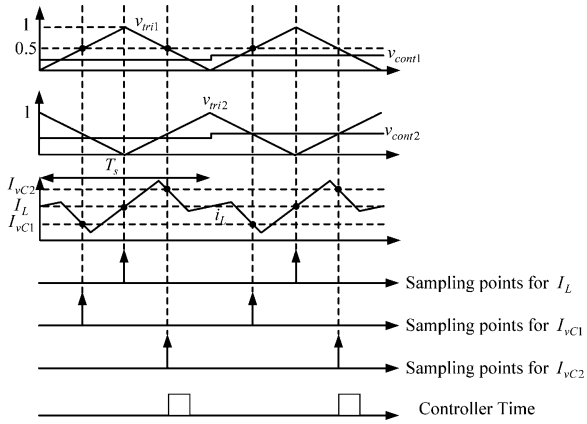

Fig. 6. Proposed sampling and hold strategy.

III. Proposed Sensorless Capacitor Voltage Balancing Control

The multiloop interleaved control and the proposed SCVBC with the proposed sampling/hold strategy are shown in Fig. 5 where only the input voltage v_s, the output voltage v_d, and the inductor current i_L are sensed. It is noted that the proposed sampling/hold strategy samples the inductor current i_L thrice per switching period T_s as shown in Fig. 6, and obtains the average value I_L and the other two values I_{vC1} and I_{vC2}.

The average value current I_L is input to the multiloop control to yield the desired PFC function and obtain the control signal $v_{\rm cont1}$. The difference ΔI_{vC} between two values I_{vC1} and I_{vC2} is calculated and the compensating signal $\Delta v_{\rm cont}$ is obtained by the used P controller

$$\Delta v_{\rm cont} = K_p(I_{vC2} - I_{vC1}). \tag{6}$$

Then, the other control signal $v_{\rm cont2}$ is generated by adding the compensating signal $\Delta v_{\rm cont}$ to the control signal $v_{\rm cont1}$

$$v_{\rm cont2} = v_{\rm cont1} + \Delta v_{\rm cont} = v_{\rm cont1} + K_p(I_{vC2} - I_{vC1}). \tag{7}$$

Fig. 6 shows the proposed sampling/hold strategy with sensing the inductor current i_L. The average value I_L is obtained by sampling the inductor current i_L at the peak of the triangular signal $v_{\rm tri1} = 1$. When the triangular signal $v_{\rm tri1}$ rises to 0.5 from the valley, the inductor current is sampled and the obtained

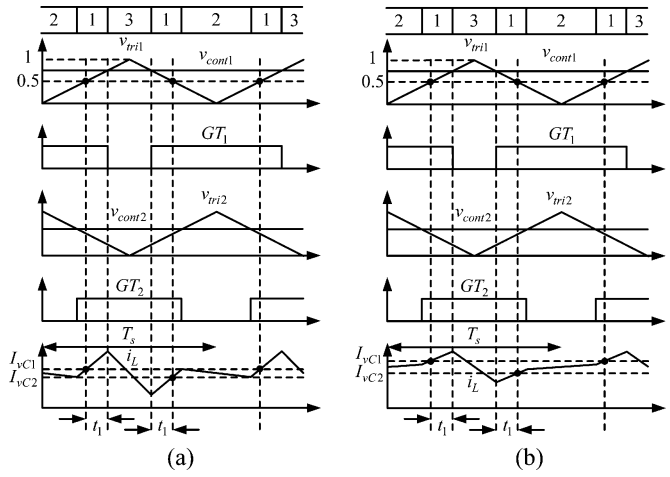

Fig. 7. Illustrated waveforms $(2 > v_{\rm cont1} + v_{\rm cont2} > 1)$. (a) $v_{C1} > v_{C2} > |v_s|$ and (b) $v_{C1} > |v_s| > v_{C2}$.

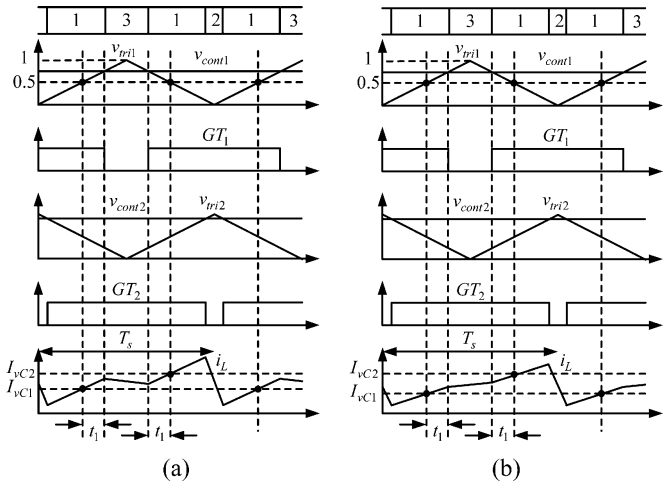

Fig. 8. Illustrated waveforms $(2 > v_{\rm cont1} + v_{\rm cont2} > 1)$. (a) $v_{C2} > v_{C1} > |v_s|$ and (b) $v_{C2} > |v_s| > v_{C1}$.

value is defined as I_{vC1}. The value I_{vC2} is sampled when the triangular signal $v_{\rm tri1}$ falls to 0.5 from the peak.

After finishing all the sampling actions, the multiloop control is performed at the controller time, and updates the two control signals at the valley of the triangular signal v_{tri1}.

In the following paragraphs, the analysis is divided into two cases - $2 > v_{\rm cont1} + v_{\rm cont2} > 1$ and $1 > v_{\rm cont1} + v_{\rm cont2} > 0$

$$2 > v_{\rm cont1} + v_{\rm cont2} > 1.$$

The illustrated waveforms for the voltage imbalance $\Delta v_C > 0$ (i.e., $v_{C1} > v_{C2}$) are plotted in Fig. 7. Since the input ac voltage v_s is time-varying, the voltage imbalance $\Delta v_C > 0$ may be divided into two conditions—either $v_{C1} > v_{C2} > |v_s|$ or $v_{C1} > |v_s| > v_{C2}$. The waveforms in the condition $v_{C1} > v_{C2} > |v_s|$ are plotted in Fig. 7(a), and the inductor current i_L is falling at the switching state 2. But the inductor current i_L is rising at the switching state 2 in the other condition $v_{C1} > |v_s| > v_{C2}$ as plotted in Fig. 7(b).

The illustrated waveforms for the voltage imbalance $v_{C2} > v_{C1} > |v_s|$ and $v_{C2} > |v_s| > v_{C1}$ are plotted in Figs. 8(a) and (b), respectively. It is noted that in Fig. 8(a), the inductor current i_L is falling at the switching state 3, but the current i_L is rising at the switching state 3 in Fig. 8(b).

Due to the waveform symmetry in Fig. 7 and Fig. 8, the time t_1 between the instants of sampling the value I_{vC1} and the turning-off instants of the gate signal $\rm GT_1$ is equal to the time between the turning-on instants of the gate signal $\rm GT_1$ and the instants of sampling the value I_{vC2}. Therefore, the time t_1 can be expressed in terms of the control signal $v_{\rm cont1}$

$$t_1 = \left(\frac{v_{\rm cont1}}{2} - \frac{1}{4}\right) T_s. \tag{8}$$

From Fig. 7 and Fig. 8, the conducting time for the switching state 2 and the switching state 3 are $(1 - v_{\rm cont2})T_s$ and $(1 - v_{\rm cont1})T_s$, respectively. The remaining time for switching state 1 is $(v_{\rm cont1} + v_{\rm cont2} - 1)T_s$. Then, the average inductor voltage $\langle v_L \rangle_{Ts}$ in the three-level boosting converter can be expressed as equation (9) at the bottom of the page.

Because of zero average inductor voltage in the steady-state condition, the rectified input voltage $|v_s|$ must be equal to

$$|v_s| = (1 - v_{\rm cont1})v_{C1} + (1 - v_{\rm cont2})v_{C2}. \tag{10}$$

From Fig. 7 and Fig. 8, the difference ΔI_{vC} between two sampled values I_{vC1} and I_{vC2} can be expressed in terms of the time t_1

$$\Delta I_{vC} = I_{vC2} - I_{vC1} = 2\frac{|v_s|}{L} t_1 + \frac{|v_s| - v_{C1}}{L}(1 - v_{\rm cont1})T_s. \tag{11}$$

Substituting (8) and (10) into (11) obtains

$$\Delta I_{vC} = \frac{T_s}{2L}\left[(v_{C2} - v_{C1})(1 - v_{\rm cont1}) - \Delta v_{\rm cont} v_{C2}\right]. \tag{12}$$

By substituting (6) into (12), the expression ΔI_{vC} in (12) can be rewritten as

$$\Delta I_{vC} = \frac{T_s(1 - v_{\rm cont1})}{2L + T_s K_P v_{C2}}(v_{C2} - v_{C1}) = k_1(v_{C2} - v_{C1}). \tag{13}$$

Because the coefficient k_1 is always positive, the difference ΔI_{vC} is proportional to the voltage imbalance $(v_{C2} - v_{C1})$. It follows that the difference ΔI_{vC} can be used to detect the voltage imbalance $(v_{C2} - v_{C1})$ without directly sensing the capacitor voltages.

$$1 > v_{\rm cont1} + v_{\rm cont2} > 0$$

$$\begin{aligned}\langle v_L \rangle_{Ts} &= \frac{|v_s|(v_{\rm cont1} + v_{\rm cont2} - 1)T_s + (|v_s| - v_{C1})(1 - v_{\rm cont1})T_s + (|v_s| - v_{C2})(1 - v_{\rm cont2})T_s}{T_s} \\ &= |v_s| - v_{C1}(1 - v_{\rm cont1}) - v_{C2}(1 - v_{\rm cont2})\end{aligned} \tag{9}$$

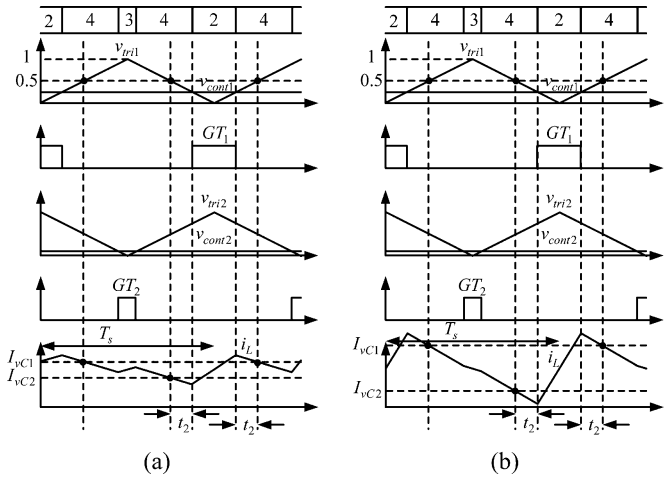

Fig. 9. Illustrated waveforms $(1 > v_{\rm cont1} + v_{\rm cont2} > 0)$. (a) $|v_s| > v_{C1} > v_{C2}$ and (b) $v_{C1} > |v_s| > v_{C2}$.

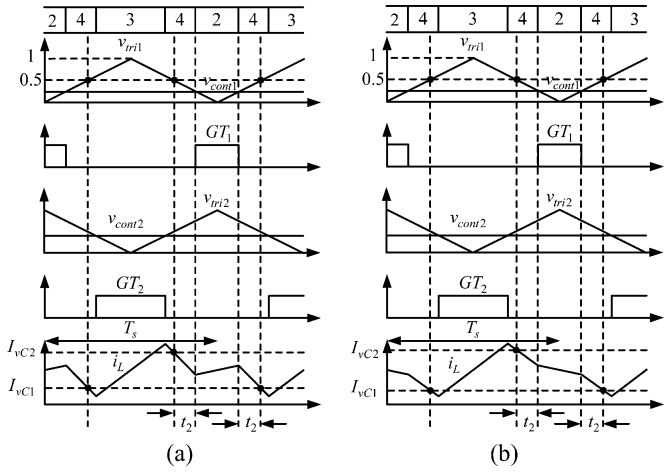

Fig. 10. Illustrated waveforms $(1 > v_{\rm cont1} + v_{\rm cont2} > 0)$. (a) $|v_s| > v_{C2} > v_{C1}$ and (b) $v_{C2} > |v_s| > v_{C1}$.

In this case, the illustrated waveforms for the voltage imbalance $v_{C1} > v_{C2} > |v_s|$ and $v_{C1} > v_{C2} > |v_s|$ are plotted in Fig. 9(a) and (b), respectively. In Fig. 9(a), the inductor current i_L is rising at the switching state 3, but the inductor current i_L is falling at the switching state 3 in Fig. 9(b).

The illustrated waveforms for the voltage imbalance $|v_s| > v_{C2} > v_{C1}$ and $v_{C2} > |v_s| > v_{C1}$ are plotted in Fig. 10(a) and Fig. 10(b), respectively. It is noted that in Fig. 10(a), the inductor current i_L is rising at the switching state 2 due to $|v_s| > v_{C2}$, but the current i_L is falling at the switching state 2 in Fig. 10(b) due to $v_{C2} > |v_s|$.

Due to the symmetry, the time t_2 between the instants of sampling the value I_{vC1} and the turning-off instants of the gate signal GT_1 can be expressed in terms of the control signal $v_{\rm cont1}$

$$t_2 = \left(\frac{1}{4} - \frac{v_{\rm cont1}}{2}\right) T_s. \tag{14}$$

From Fig. 9 and Fig. 10, the conducting times for switching state 2 and switching state 3 are $(v_{\rm cont1}T_s)$ and $(v_{\rm cont2}T_s)$, respectively. The remaining times in a switching period T_s for switching state 4 is $(1 - v_{\rm cont1} - v_{\rm cont2})T_s$. The average inductor voltage $\langle v_L \rangle_{Ts}$ in the three-level converters is the same as (9), equation (15) at the bottom of the page.

From Fig. 9 and Fig. 10, the difference ΔI_{vC} between two sampled values I_{vC1} and I_{vC2} can expressed in terms of the time

$$\Delta I_{vC} = I_{vC2} - I_{vC1} = -\frac{|v_s| - v_{C2}}{L} v_{\rm cont1} T_s - 2\frac{|v_s| - v_d}{L} t_2. \tag{16}$$

Substituting (10) and (14) into (16) obtains

$$\Delta I_{vC} = \frac{T_s}{2L}\left[(v_{C2} - v_{C1})v_{\rm cont1} + \Delta v_{\rm cont} v_{C2}\right]. \tag{17}$$

By substituting (6) into (17), (17) can be rewritten as

$$\Delta I_{vC} = \frac{T_s v_{\rm cont1}}{2L - T_s K_P v_{C2}}(v_{C2} - v_{C1}) = k_2(v_{C2} - v_{C1}). \tag{18}$$

The coefficient k_2 may be either positive one or negative one. In order to force the coefficient k_2 positive, the denominator of (18) should be positive

$$2L - T_s K_P v_{C2} > 0. \tag{19}$$

It implies that the controller parameter K_P should be located at the range

$$0 < K_P < \frac{2L}{T_s v_{C2,\max}} \tag{20}$$

where $v_{C2,\max}$ is the maximum bottom capacitor voltage. Then, the difference ΔI_{vC} would be proportional to the voltage imbalance $(v_{C2} - v_{C1})$.

From (13) and (18) in both cases, the difference ΔI_{vC} in both cases are proportional to the voltage imbalance $(v_{C2} - v_{C1})$ via properly selecting the controller parameter K_P, which implies that the difference ΔI_{vC} obtained from the proposed SCVBC can be used to detect the voltage imbalance $(v_{C2} - v_{C1})$ without directly sensing the capacitor voltages.

IV. Simulation

In this section, some simulation results of the three-level boosting converter are provided and the used parameters are tabulated in Table II. For the multiloop control in Fig. 1, the parameters of the voltage controller are $K_{Pv} = 0.1$ and $K_{Iv} = 5$, and the parameters of the current controller are $K_{Pi} = 0.02$ and $K_{Ii} = 10$. From (20), the range of the parameter K_P must be

$$\begin{aligned}\langle v_L \rangle_{Ts} &= \frac{(|v_s| - v_d)(1 - v_{\rm cont1} - v_{\rm cont2})T_s + (|v_s| - v_{C1})v_{\rm cont2}T_s + (|v_s| - v_{C2})v_{\rm cont1}T_s}{T_s} \\ &= |v_s| - v_{C1}(1 - v_{\rm cont1}) - v_{C2}(1 - v_{\rm cont2})\end{aligned} \tag{15}$$

TABLE II
SIMULATED PARAMETERS OF THREE-LEVEL BOOST CONVERTER

Input voltage	$110V(rms)$, $50Hz$
Output voltage	$V_d^* = 300V$
Inductor	$0.5mH$
Carrier frequency	20kHz
Capacitor	$C_1 = 2240\mu F$, $C_2 = 1410\mu F$ equivalent capacitance $\approx 865\mu F$
Voltage balance parameter	$K_P = 0.05$

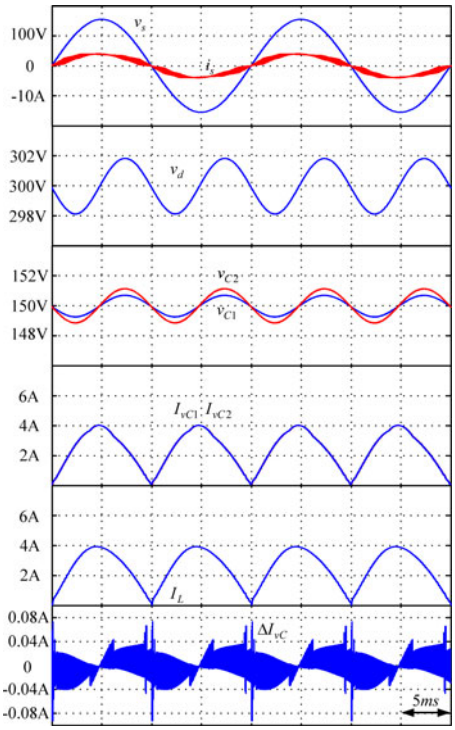

Fig. 11. Simulation results for the three-level boost converter at 300 W.

between 0 and 0.1. Then, $K_P = 0.05$ is selected with consideration of the inductance variation.

Two mismatched capacitances with $C_1 = 2240$ μF and $C_2 = 1410$ μF are used in the simulation. The capacitance-mismatch condition does not appear in the practical case, but the mismatched conditions are helpful for the demonstration of the proposed SCVBC.

A. Steady-State Response

The simulation results for the three-level boosting PFC converter at 300W and 600 W are plotted in Fig. 11 and Fig. 12, respectively. The yielded input currents i_s are sinusoidal in phase with the input voltage v_s. Both capacitor voltages have the average values equal to the half average value of the dc voltage v_d even though the capacitances are mismatched.

The obtained value ΔI_{vC} approximates to zero in the steady state. The results show that the proposed SCVBC is able to achieve PFC function in the three-level boost converter without directly sensing capacitor voltages.

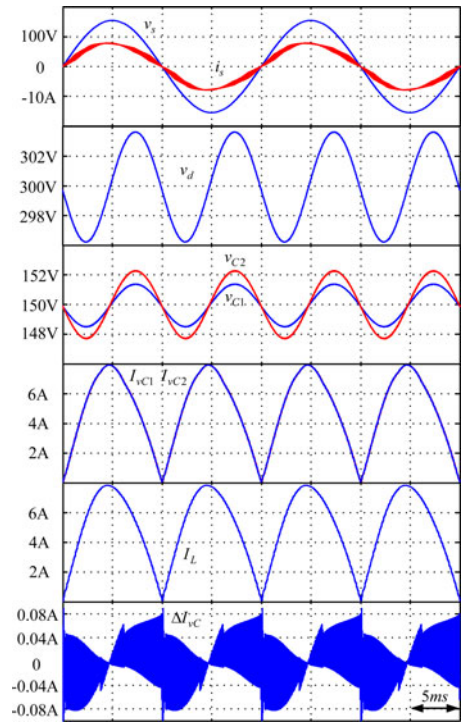

Fig. 12. Simulation results for the three-level boost converter at 600 W.

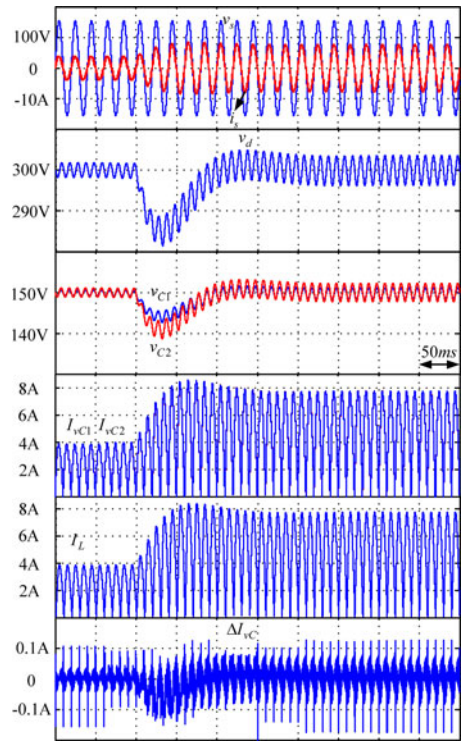

Fig. 13. Simulation waveforms during load change from 300 to 600 W.

B. Transient Response

In order to observe the transient response, the simulation results during load regulation are plotted in Fig. 13. The output power changes from 300 to 600 W due to the change of the load resistance from 300 to 150 Ω. During the operation, the

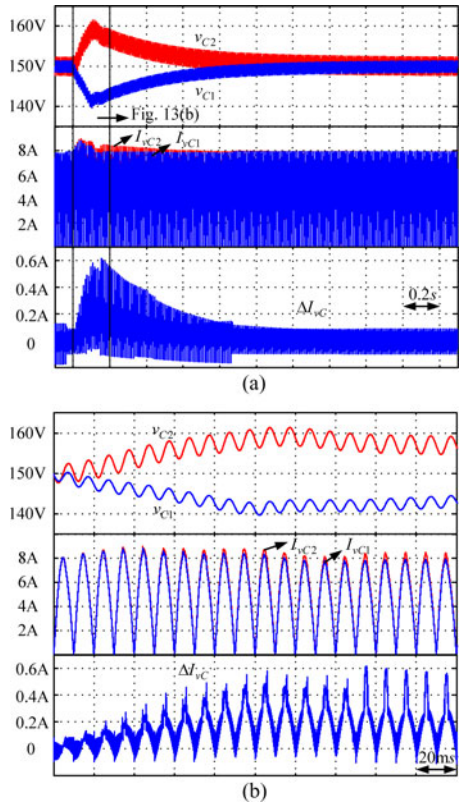

Fig. 14. Simulation results when a resistor 400Ω is connected to the capacitor C_1 and then, removed from the capacitor C_1.

sinusoidal input current i_s is always in phase with the input voltage v_s and the output voltage v_d is well regulated to the command 300 V.

In addition, the bottom capacitor voltage v_{C2} possesses larger voltage dip than the top capacitor voltage v_{C1}, because that the capacitance C_2 is smaller than the other capacitance C_1. The significant dip in the difference ΔI_{vC} can also be found during the transient operation.

Both average capacitor voltages are finally equal to half voltage command 150 V, which also shows that the proposed SCVBC is able to detect the voltage imbalance and balance the capacitor voltages.

The other simulation results of the transient operation are provided in Fig. 14(a) where a $400\,\Omega$ resistor is suddenly connected the capacitor C_1 and then, removed from the capacitor C_1. The zoomed waveforms are plotted in Fig. 14(b).

The capacitor voltage v_{C1} drops to 140 V in $0.1\,\mathrm{s}$ due to the connected resistor, and at the same time, the capacitor voltage v_{C2} raises to 160 V due to the voltage control loop in the multiloop control.

It is noted that during the transient operation, the difference ΔI_{vC} becomes positive when the capacitor voltage v_{C2} is larger than the other capacitor voltage v_{C1}. After the resistor is removed, both capacitor voltages are finally balanced.

Obviously, the provided simulation results show that the proposed SCVBC works well without directly sensing the capacitor voltages.

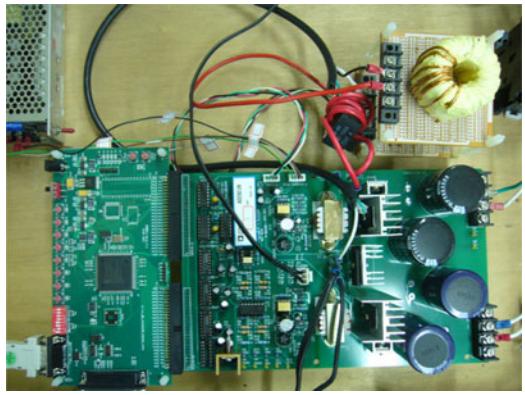

Fig. 15. Implemented three-level boosting PFC converter with the FPGA board.

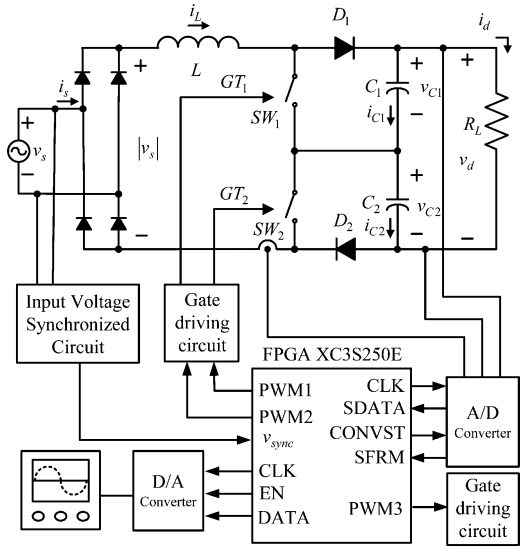

Fig. 16. Block diagram of the implemented three-level boosting PFC converter.

V. Experimental Results

The proposed SCVBC had been implemented in an FPGA-based system as shown in Fig. 15. The nominal parameters are the same as those in Table II. Fig. 16 is the block diagram of the implemented three-level boosting PFC converter. Due to no A/D and no D/A function in the commercial FPGA XC3S250 chip, three external A/D converters are used to sense the output voltage, the input voltage, and the inductor current. Some D/A converters are also used to show the control variables in the scope.

Fig. 17 and Fig. 18 show the steady-state experimental waveforms at the power level 300 ($R_L = 300\,\Omega$) and 600 W ($R_L = 150\,\Omega$), respectively. Both output voltage v_d are well regulated to 300 V, and the input currents i_s are sinusoidal in phase with the input voltage v_s. Although two capacitor voltages have different voltage ripples due to their different capacitance, they have the same average voltage 150 V.

The input current harmonics of the waveforms in Fig. 17 and Fig. 18 are listed in Table III where the limitations for the Class D in IEC-61000-3-2 standard are also provided for comparison.

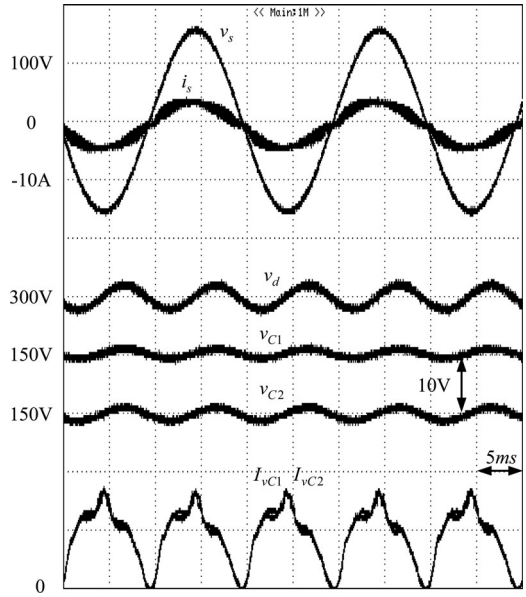

Fig. 17. Experimental results at 300 W.

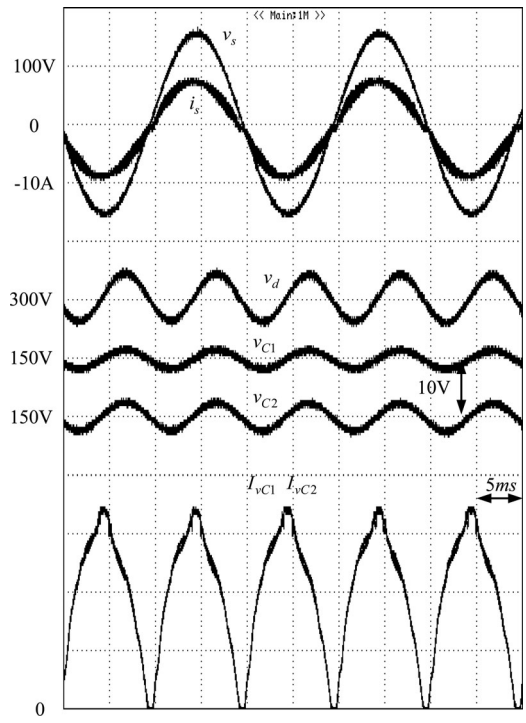

Fig. 18. Experimental results at 600 W.

In the experiment, the yielded input current harmonics are below the IEC-61000-3-2 standard.

In order to observe the transient responses, the experimental waveforms during the load change from 300 to 600 W are plotted in Fig. 19. The input currents i_s keeps sinusoidal in phase with the input voltage v_s during the load regulation. All three voltages v_d, v_{C1}, and v_{C2} are well regulated during the transient period and the capacitor v_{C2} has the larger voltage dip than the other capacitor voltage v_{C1}.

TABLE III
INPUT CURRENT HARMONICS AT VARIOUS POWER LEVELS

Harmonics	Class D 300W(A)	Fig. 17 (A)	Class D 600W(A)	Fig. 18 (A)
Fundamental	X	2.7975	X	5.6130
3rd	1.02	0.1604	2.04	0.1430
5th	0.57	0.0258	1.14	0.0098
7th	0.3	0.0092	0.6	0.0140
9th	0.15	0.0330	0.3	0.0196
11th	0.105	0.0384	0.21	0.0774
13th	0.089	0.0188	0.178	0.0124
15th	0.077	0.0234	0.154	0.0082
17th	0.068	0.0364	0.136	0.0461
19th	0.061	0.0360	0.122	0.0413
21st	0.055	0.0358	0.11	0.0358
PF		0.9952		0.9984

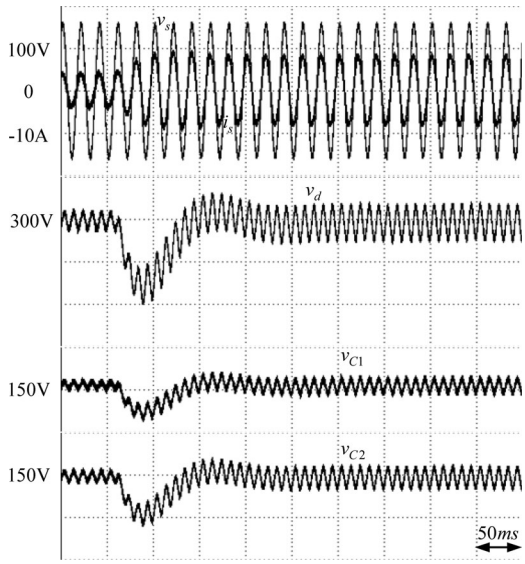

Fig. 19. Experimental waveforms during the load change from 300 to 600 W.

It can be found that the experimental results in Fig. 19 are similar to the simulation results in Fig. 13. Therefore, the proposed SCVBC is able to balance voltages during the load regulation.

After connecting a resistor $400\,\Omega$ to the capacitor C_1, the experimental results are shown in Fig. 20(a) and the zoomed waveforms are plotted in Fig. 20(b). The resistor is removed from the capacitor after 0.1 s.

Due to the connected resistor across the capacitor C_1, the capacitor voltage v_{C1} drops quickly, and at the same time, the other capacitor voltage v_{C2} rises in order to regulate the dc-side voltage v_d. After the resistor is removed, significant positive voltage imbalance $(v_{C2} - v_{C1}) > 0$ exists and the sensed difference becomes positive $\Delta I_{vC} > 0$, too. It shows that the proposed difference signal ΔI_{vC} is able to detect the voltage imbalance by sensing the inductor current. Then, the two capacitor voltages are finally balanced.

There are many examples that the load current is not constant, but pulsating, such as phase-shifted dc/dc converter, electronic ballasts. To evaluate the performance of the pulsating load current, an additional semiconductor switch is connected in series with the load resistor $R_L = 150\,\Omega$. The additional switch switches with the same 20 kHz as the PFC switching frequency, and its duty ratio changes linearly from 100% to 10% to vary the

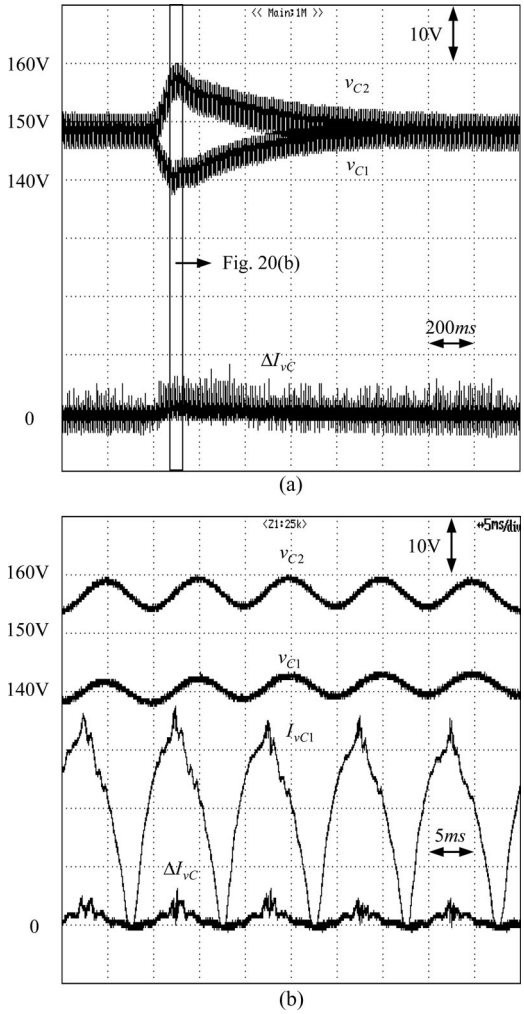

Fig. 20. (a) Experimental results when capacitor voltages are forced to change and (b) the zoomed waveform of Fig. 20(a).

equivalent load resistor R'_L from 150 to 1500 Ω. The obtained experimental results are provided in Fig. 21.

Before PFC and SCVBC are applied, the capacitor voltages are not balanced due to the mismatched capacitances. The capacitor voltages turn to rise and finally become balanced after the PFC and the SCVBC are applied. Then, the equivalent load resistor R'_L changes linearly from 150 to 1500 Ω. The experimental waveforms with equivalent resistors 150, 300, and 1500 Ω are plotted in Fig. 21(b), (c) and (d), respectively. Although the load current is pulsating, the PFC performances are still accepted.

The proposed SCVBC is developed based on the assumptions of ideal inductor and ideal capacitors. The provided experimental results show that the proposed SCVBC works well in the practical condition of nonzero inductor resistance and capacitor resistance.

The provided results also show that the proposed SCVBC cooperated with the multiloop interleaved control possesses the ability to achieve both the PFC function and the voltage balancing function without sensing any capacitor voltage even large difference between two capacitances exists.

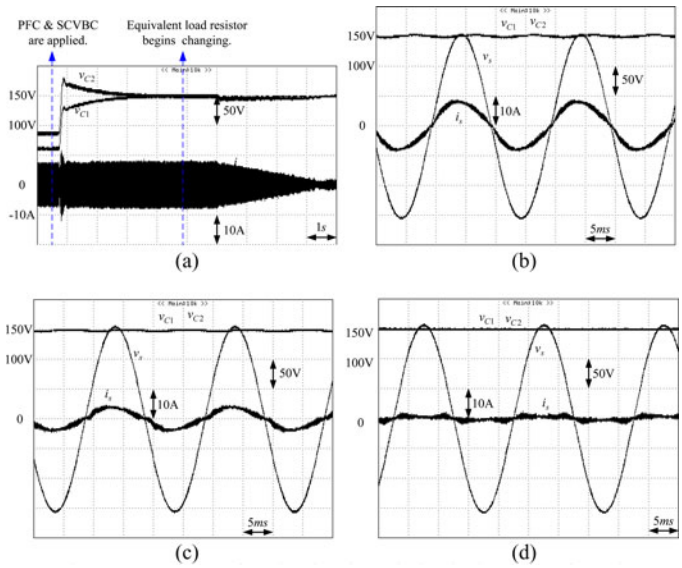

Fig. 21. (a) Experimental results when the equivalent load resistor is changed, (b) the zoomed waveforms with equivalent resistor 150 Ω (duty ratio 100%), (c) the zoomed waveforms with equivalent resistor 300 Ω (duty ratio 50%). (d) Zoomed waveforms with equivalent resistor 1500 Ω (duty ratio 10%).

VI. Conclusion

In this paper, the SCVBC method for the three-level boosting PFC converter has been proposed. The proposed method shows that the voltage imbalance can be detected from sensing the inductor current by the proposed sampling/hold strategy. That is, it eliminates the need for extra sensors, reduces control complexity, and reduces the cost and size. The reduction of cost and size are the important contributions for PFC converters. The control method is implemented in an FPGA-based system, and all the provided results demonstrate the proposed method.

References

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[2] J. C. Crebier, B. Revol, and J. P. Ferrieux, "Boost-chopper-derived PFC rectifiers: Interest and reality," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 36–45, Feb. 2005.

[3] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up DC–DC converter with coupled-inductor and voltage-doubler circuits," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4196–4206, Sep. 2011.

[4] A. Shahin, M. Hinaje, J. P. Martin, S. Pierfederici, S. Rael, and B. Davat, "High voltage ratio DC–DC converter for fuel-cell applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 3944–3955, Dec. 2010.

[5] M. H. Todorovic, L. Palma, and P. N. Enjeti, "Design of a wide input range DC–DC converter with a robust power control scheme suitable for fuel cell power conversion," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1247–1255, Mar. 2008.

[6] W. Li and X. He, "Review of nonisolated high-step-Up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[7] J. M. Kwon, B. H. Kwon, and K. H. Nam, "Three-phase photovoltaic system with three-level boosting MPPT control," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2319–2327, Sep. 2008.

[8] V. Yaramasu and B. Wu, "Three-level boost converter based medium voltage megawatt PMSG wind energy conversion systems," in *Proc. Energy Convers. Cong. Expo.*, 2011, pp. 561–567.

[9] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *IEEE App. Power Electron. Conf.*, 1995, pp. 434–439.
[10] J. R. Pinheiro, D. L. R. Vidor, and H. A. Grundling, "Dual output three-level boost power factor correction converter with unbalanced loads," in *Proc. IEEE Power Electron. Spec. Conf.*, 1996, pp. 733–739.
[11] B. R. Lin and H. H. Lu, "A novel PWM scheme for single-phase three-level power-factor-correction circuit," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 245–252, Apr. 2000.
[12] H. Wu and X. He, "Single phase three-level power factor correction circuit with passive lossless snubber," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 946–953, Nov. 2002.
[13] J. Y. Liao and H. C. Chen, "Multiloop interleaved control for two-switch two-capacitor three-level SMR without capacitor voltage balancing loop," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 3766–3772.
[14] R. Greul, S. D. Round, and J. W. Kolar, "The Delta-Rectifier: Analysis, Control and Operation," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1637–1648, Nov. 2006.
[15] E. Ribeiro, A. J. M. Cardoso, and C. Boccaletti, "Fault-tolerant strategy for a photovoltaic DC–DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 3008–3018, Jun. 2013.
[16] R. Ghosh and G. Narayanan, "A simple analog controller for single-phase half-bridge rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 186–198, Jan. 2007.
[17] B. R. Lin, T. L. Huang, and C. H. Huang, "Bi-directional single-phase half-bridge rectifier for power quality compensation," *IEE, Electric Power Appl.*, vol. 150, no. 4, pp. 397–406, July 2003.
[18] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.
[19] C. Gao, X. Jiang, Y. Li, Z. Chen, and J. Liu, "A DC-link voltage self-balancing method for a diode-clamped modular multilevel converter with minimum number of voltage sensors," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2125–2139, May 2013.
[20] H. C. Chen and Wen-Jan Lin, "MPPT and voltage balancing control with sensing only inductor current for PV-fed three-level boost-type converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 29–35, Jan. 2014.

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