Multiloop Interleaved Control for Three-Level Switch-Mode Rectifier in AC/DC Applications

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***Abstract*—In this paper, multiloop interleaved control (MIC) is proposed, and it is combined with conventional multiloop control and the interleaved pulsewidth modulation scheme. The average behavior of the interleaved three-level switch-mode rectifier (SMR) behaves similar to the conventional boost-type SMR even though two capacitor voltages are imbalanced. It implies that conventional multiloop control can be applied to the interleaved three-level SMRs to achieve the desired power factor correction function. The proposed MIC is digitally implemented and verified in a field-programmable-gate-array-based system. The provided results show that MIC stably works and the capacitor voltages are eventually balanced during the system operations.**

***Index Terms*—Interleaved control, three-level boost switch-mode rectifier (SMR).**

I. Introduction

With the increase in power electronics products, the power factor correction (PFC) function becomes important [1]. Generally speaking, the PFC function includes shaping the current waveform and regulating the output voltage. Due to the continuous input current, the boost-type converter has been widely integrated to the switch-mode rectifier (SMR) shown in Fig. 1(a) to achieve the desired PFC function [2]. The gate signal *GT* is obtained from the comparison of controller output signal $v_{\rm cont}$ and sawtooth signal $v_{\rm tri}$.

As shown in Fig. 1(b), the conventional multiloop control includes an inner current loop and an outer voltage loop, and it is often used to generate the gate signal for the conventional boost-type SMR. One inductor current signal is fed back to the inner current loop to shape the current waveform. The output voltage is sensed for the outer voltage loop to regulate the output voltage. Sensing input voltage is also required for the generation of the desired current reference [3], [4] and the feedforward terms [5], [6]. In [7] and [8], some compensation loops are added to the multiloop control to improve the PFC performance for motor drive applications. For the boost converter, the single switch needs to withstand the overall output voltage when the switch blocks.

The three-level boost converter is shown in Fig. 2 where two capacitors are connected across the switches, respectively.

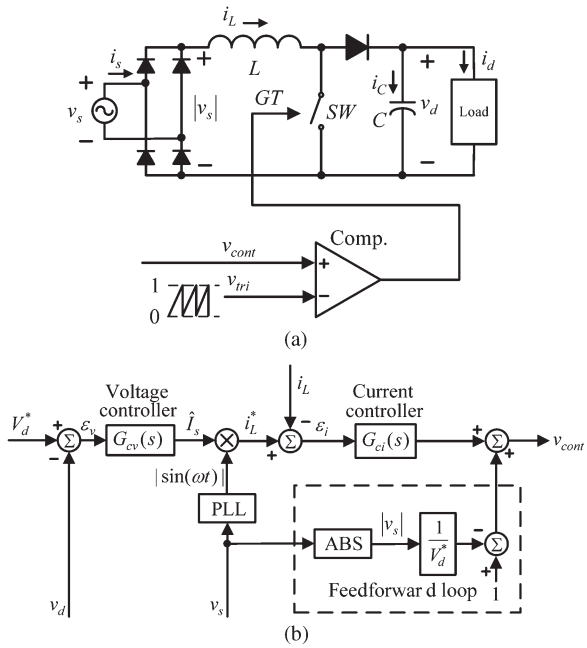

Fig. 1. (a) Conventional boost-type SMR. (b) Multiloop control with feedforward loop [5], [6].

Thus, each switch needs to withstand only a half output voltage. In addition, the inductor voltage in the three-level boost converter has three levels, but the inductor voltage in the conventional boost converter has only two levels.

Therefore, the three-level boost converter is able to yield smaller inductor current ripple than the conventional boost converter. It follows that three-level converters are often used in the applications, such as the high-voltage–ratio dc/dc conversion [9]–[12] and the wide input voltage range [13], particularly in the fuel cell applications [11], [13] and the grid-connected applications [10], [14], [15].

Additionally, the high-withstanding-voltage semiconductor switches often have larger drain–source resistances than the low-withstanding-voltage ones. Thus, the three-level converter has the advantages of low voltage stress, small inductor current ripple, and low switching loss [1], [11], [16].

In Fig. 2, the three-level SMR was obtained by connecting the diode rectifier with the three-level converter [16]–[20]. In [17], the three single-phase three-level SMRs are in Delta connection to achieve the three-phase PFC function with the ability of redundancy.

The control methods for the three-level SMR (ac/dc application) can be found in [18]–[20] where gate signals *GT1* and *GT2* are generated from the lookup table with inputs H_1, H_2, and H_3.

Manuscript received December 9, 2012; revised February 17, 2012, April 3, 2013, and June 14, 2013; accepted July 24, 2013. Date of publication August 16, 2013; date of current version January 31, 2014. This work was supported by the Ministry of Economic Affairs of Taiwan under Contract 99-EC-17-A-05-S1-154.

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Digital Object Identifier 10.1109/TIE.2013.2278961

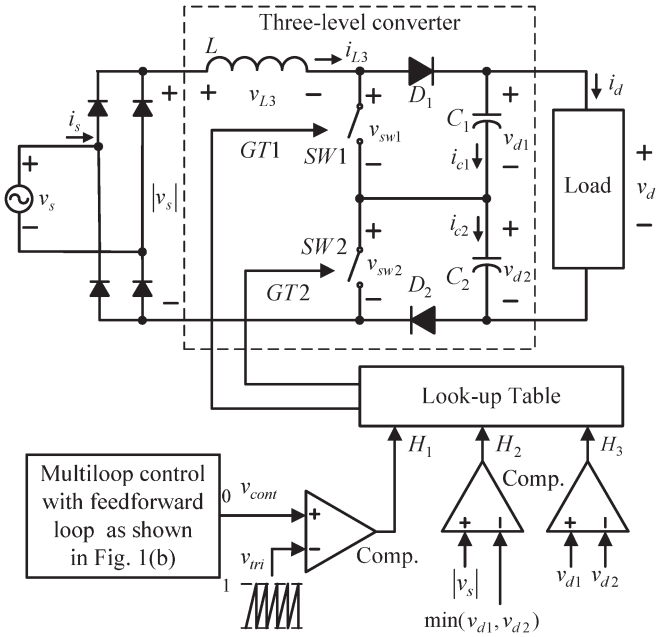

Fig. 2. Three-level SMR and its conventional control [17]–[19].

Comparative signal H_1 is generated from the comparison of the conventional multiloop output $v_{\rm cont}$ and sawtooth signal $v_{\rm tri}$, and signal H_1 is the same as gate signal *GT* in Fig. 1. The table input H_2 is the comparison output to show whether the absolute input voltage $|v_s|$ is lower or higher than the minimum one of capacitor voltages v_{d1} and v_{d2}. The input H_3 is used to indicate which capacitor voltage is higher than the other.

It can be found that sensing capacitor voltage is required for the generation of inputs H_2 and H_3. Therefore, for the control of the three-level SMR, it is necessary to sense individual capacitor voltage and to add voltage balancing loop in [18]–[20]. Similar voltage balancing loops can be also found in the dc/dc applications [11], [12], [14], [15], [21].

In this paper, the average behavior of a three-level SMR under the interleaved pulsewidth modulation (PWM) scheme [22]–[24] (i.e., interleaved three-level SMR) is derived. The interesting result shows that the interleaved three-level SMR behaves similar to a conventional boost-type SMR even when the two capacitor voltages are imbalanced. It means that the multiloop control and the interleaved PWM scheme can be integrated to achieve the desired PFC function without an additional voltage balancing loop. Thus, the proposed multiloop interleaved control (MIC) is simpler than the control method in Fig. 2.

From the provided simulation and experimental results, the proposed MIC is able to achieve PFC functions, and in particular, the three-level SMR in ac/dc application is able to take several seconds to balance the capacitor voltages without the voltage balancing control loop. However, because the time taken to balance the voltages is long, the voltage balancing loop is sometimes required.

II. Conventional Boost-Type SMR

In first, the average inductor voltage and the current ripple of the conventional boost-type SMR in Fig. 1 is studied for comparison. The input voltage $v_s = \hat{V}_s \sin(2\pi ft)$ is assumed to be a sinusoidal function with peak amplitude $\hat{V}_s$. Through the diode rectifier, the input voltage of a boost converter can be expressed by an absolute function $|v_s|$.

By assuming that switching frequency f_s is much larger than line frequency f, the control signal $v_{\rm cont}$ within each switching period $T_s = 1/f_s$ can be regarded as a constant. Then, in Fig. 1, the operating duty ratio of the switch is equal to $v_{\rm cont}$ due to the unity sawtooth signal $v_{\rm tri}$. It means that the conducting time and the blocking time of the switch can be expressed as $v_{\rm cont}T_s$ and $(1 - v_{\rm cont})T_s$, respectively.

A. Average Inductor Voltage

When the switch conducts in Fig. 1, inductor voltage v_L equals the rectified input voltage $|v_s|$. Once the switch blocks, inductor voltage v_L equals the difference between the rectified input voltage $|v_s|$ and output voltage v_d, i.e., $v_L = |v_s| - v_d$. Then, the average inductor voltage $\langle v_L \rangle_{Ts}$ within each switching period T_s can be expressed by

$$\langle v_L \rangle_{Ts} = \frac{\begin{bmatrix} |v_s| v_{\rm cont} T_s \\ +(|v_s| - v_d)(1 - v_{\rm cont})T_s \end{bmatrix}}{T_s} = |v_s| - (1 - v_{\rm cont})v_d. \tag{1}$$

The input voltage of the boost converter is equal to the rectified input voltage $|v_s| = \hat{V}_s |\sin(2\pi ft)|$. By assuming that output voltage v_d is well regulated to voltage command V_d^*, duty ratio $v_{\rm cont}$ can be expressed as

$$v_{\rm cont} = 1 - \frac{\hat{V}_s \, |\sin(2\pi ft)|}{V_d^*}. \tag{2}$$

B. Inductor Current Ripple

When the switch conducts, the inductor voltage is equal to the rectified input voltage $v_L = |v_s|$. Thus, the rising rate of the inductor current is $|v_s|/L$. Similarly, the falling rate of the current is $(|v_s| - v_d)/L$ when the switch blocks. Therefore, within each switching period T_s, inductor current ripple Δi_L can be expressed by either the current rising rate or the current falling rate. Thus

$$\Delta i_L = \frac{|v_s|}{L} v_{\rm cont} T_s = \frac{|v_s|}{L f_s} v_{\rm cont} \tag{3}$$

$$\Delta i_L = \frac{|v_s| - v_d}{L}(1 - v_{\rm cont})\, T_s = \frac{|v_s| - v_d}{L f_s}(1 - v_{\rm cont}). \tag{4}$$

By combining (3) and (4) and eliminating the term $|v_s|$, the expression of current ripple Δi_L can be obtained by

$$\begin{aligned} \Delta i_L &= \frac{v_d}{L f_s}(1 - v_{\rm cont}) v_{\rm cont} \\ &= -\frac{v_d}{L f_s}\left(v_{\rm cont} - \frac{1}{2}\right)^2 + \frac{v_d}{4 L f_s} \le \frac{v_d}{4 L f_s}. \end{aligned} \tag{5}$$

It is clear that the maximum current ripple $\Delta i_{L,\max} = v_d/(4Lf_s)$ occurs at the duty ratio $v_{\rm cont} = 1/2$, and the minimum current ripple is zero, i.e., $\Delta i_{L,\min} = 0$, when the control signal equals either $v_{\rm cont} = 1$ or $v_{\rm cont} = 0$.

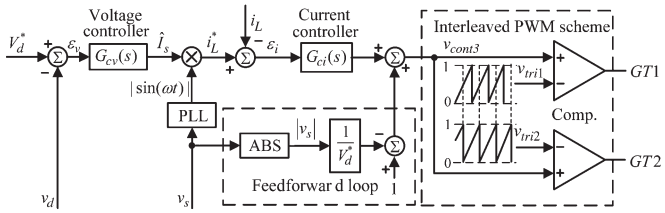

Fig. 3. Proposed MIC for three-level SMR.

C. Output Voltage

When the switch conducts, the diode current is zero, i.e., $i_D(t) = 0$, and when the switch blocks, diode current $i_D(t)$ is equal to the inductor current, i.e., $i_D(t) = i_L(t)$. Then, the average diode current $\langle i_D \rangle_{Ts}$ within switching period T_s can be expressed in terms of duty ratio $v_{\rm cont}$ and the average inductor current $\langle i_L \rangle_{Ts}$. Thus

$$\langle i_D \rangle_{T_s} = (1 - v_{\rm cont}) \langle i_L \rangle_{T_s}. \tag{6}$$

Assume that the average inductor current $\langle i_L \rangle_{Ts}$ is well controlled to follow the rectified sinusoidal waveform $\langle i_L \rangle_{Ts} = \hat{I}_s |\sin(2\pi ft)|$ in phase with input voltage $v_s(t)$. Then, by combining (2) and (6), the average diode current $\langle i_D \rangle_{Ts}$ can be rewritten as

$$\langle i_D \rangle_{Ts} = \frac{\hat{V}_s \hat{I}_s \sin(2\pi ft)^2}{V_d^*} = \frac{\hat{V}_s \hat{I}_s}{2V_d^*} - \frac{\hat{V}_s \hat{I}_s}{2V_d^*} \cos(4\pi ft). \tag{7}$$

It is clear that the second term in (7) is an ac component with double line frequency, and it must flow through capacitor C. Thus, the average capacitor current $\langle i_C \rangle_{T_s}$ is equal to

$$\langle i_C \rangle_{Ts} = -\frac{\hat{V}_s \hat{I}_s}{2V_d^*} \cos(4\pi ft). \tag{8}$$

The average capacitor current $\langle i_C \rangle_{T_s}$ flowing through capacitor C yields the following average voltage ripple $\langle v_{\rm rip} \rangle_{Ts}$:

$$\langle v_{\rm rip} \rangle_{Ts} \approx \frac{1}{C} \int \langle i_C \rangle_{Ts} \, dt = -\frac{\hat{V}_s \hat{I}_s}{8\pi f C V_d^*} \sin(4\pi ft). \tag{9}$$

Then, the average output voltage can be roughly expressed as

$$\langle v_d \rangle_{Ts} \approx V_d^* + \langle v_{\rm rip} \rangle_{Ts} = V_d^* - \frac{\hat{V}_s \hat{I}_s}{8\pi f C V_d^*} \sin(4\pi ft). \tag{10}$$

III. MIC

The proposed MIC shown in Fig. 3 combines the conventional multiloop control, the feedforward loop, and the interleaved PWM scheme. Both the voltage controller and the current controller are proportional–integral-type controllers. Two gate signals G_{T1} and G_{T2} are generated from the comparisons of control signal $v_{\rm cont3}$ and two unit sawtooth signals $v_{\rm tri1}$ and $v_{\rm tri2}$, respectively. It is noted that the two sawtooth signals have unit amplitude and identical period T_s; however, there is a 180° phase difference between them. Both duty ratios of switches *SW*1 and *SW*2 are equal to the MIC control signal $v_{\rm cont3}$.

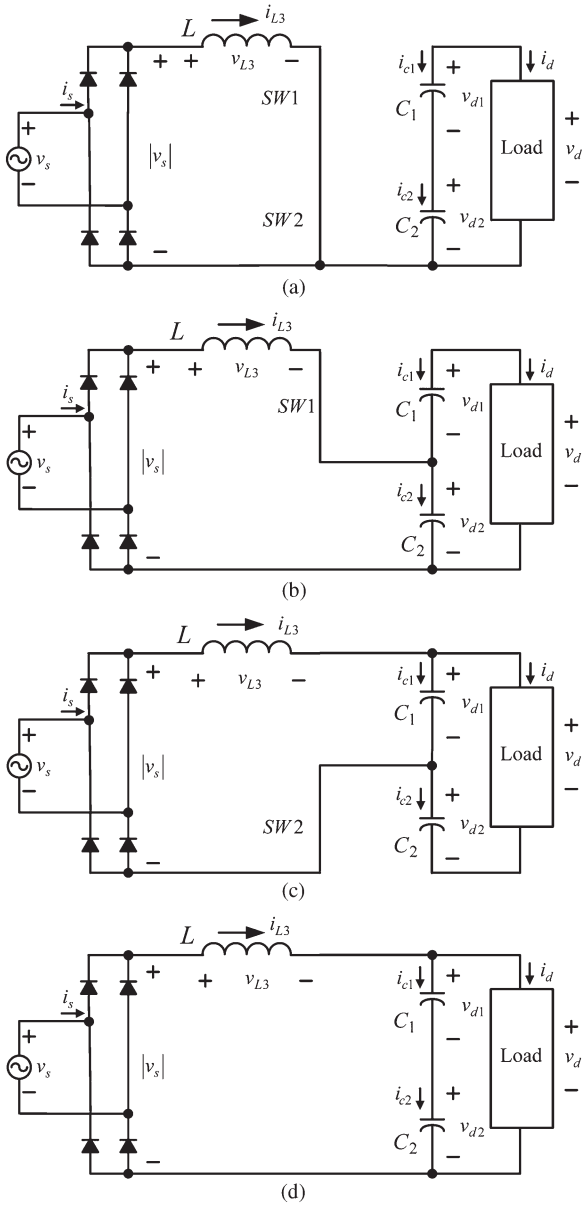

Fig. 4. Possible switching states in the interleaved three-level SMR. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

Due to input inductor L and diodes D_1 and D_2 in the three-level SMR, both switches are turned on at the same time. Therefore, there are four possible switching states in the operation of the interleaved three-level SMR, and they are plotted in Fig. 4.

As shown in Fig. 4(a), both switches turn on at switching state 1. Thus, inductor voltage v_{L3} in the three-level SMR equals the rectified input voltage $v_{L3} = |v_s|$, and both capacitors supply energy to the load $i_{C1} = i_{C2} = -i_d$. At switching state 2 plotted in Fig. 4(b), the upper switch turns on, and the lower switch turns off. The resulting inductor voltage $v_{L3} = |v_s| - v_{d2}$ equals the difference between the rectified input voltage $|v_s|$ and capacitor voltage v_{d2}. Additionally, capacitor C_1 supplies energy to the load $i_{C1} = -i_d$; however, capacitor C_2 stores the energy from input source $i_{C2} = i_{L3} - i_d$.

Similarly, the resulting inductor voltage in Fig. 4(c) is equal to the rectified input voltage minus the upper capacitor voltage $v_{L3} = |v_s| - v_{d1}$. At switching state 3, the upper capacitor

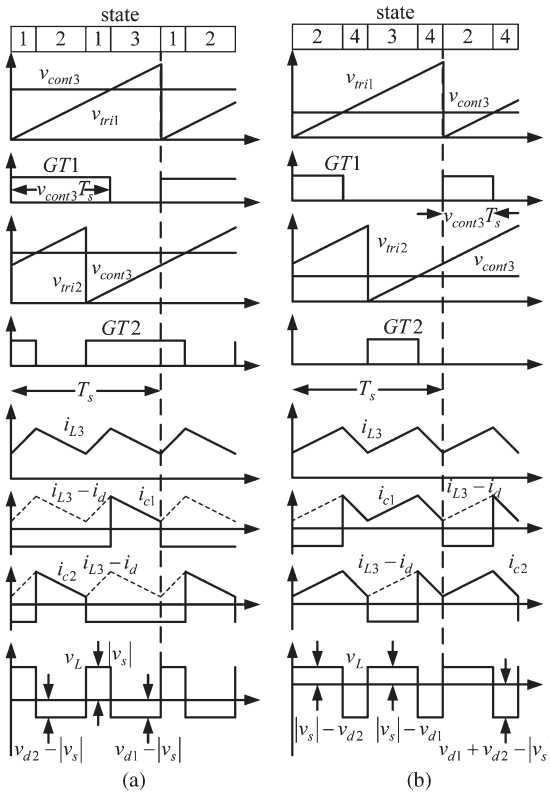

Fig. 5. Illustrated waveforms for (a) $v_{\rm cont} > 0.5$ and (b) $v_{\rm cont} < 0.5$.

C_1 is charging $i_{C1} = i_{L3} - i_d$, but the lower capacitor C_2 is discharging $i_{C2} = -i_d$.

When both switches turn off in Fig. 4(d), the resulting inductor voltage equals the rectified input voltage minus the output voltage $v_{L3} = |v_s| - v_d = |v_s| - v_{d1} - v_{d2}$. The rectified input voltage $|v_s|$ supplies the load and charges both capacitors $i_{C1} = i_{C2} = i_{L3} - i_d$.

The analysis of the three-level converter can be divided into two conditions. One condition is $v_{\rm cont3} > 0.5$, and the other condition is $v_{\rm cont3} < 0.5$. Both illustrated waveforms are plotted in Fig. 5.

A. Average Inductor Voltage

$v_{\rm cont3} > 0.5$*:* When control signal $v_{\rm cont3}$ is larger than 0.5, both duty ratios of the switches are larger than 0.5, and their conducting times are $v_{\rm cont3}T_s$. However, there is a time difference $T_s/2$ between their turning-on instants. Therefore, the times taken by switching state 2 and switching state 3 are $(1 - v_{\rm cont3})T_s$. The remaining time for switching state 1 is $(2v_{\rm cont3} - 1)T_s$ because each switching period is T_s.

By applying the average method, the average inductor voltage $\langle v_{L3}\rangle_{Ts}$ in this condition can be expressed as

$$\begin{aligned}\langle v_{L3}\rangle_{Ts} &= \frac{\begin{array}{l}|v_s|(2v_{\rm cont3}-1)T_s \\ +(|v_s|-v_{d_1})(1-v_{\rm cont3})T_s \\ +(|v_s|-v_{d2})(1-v_{\rm cont3})T_s\end{array}}{T_s} \\ &= |v_s| - (1-v_{\rm cont3})(v_{d1}+v_{d2}) = |v_s| - (1-v_{\rm cont3})v_d \end{aligned} \tag{11}$$

where output voltage v_d is the sum of the two capacitor voltages $v_d = v_{d1} + v_{d2}$.

$v_{\rm cont} < 0.5$*:* As shown in Fig. 5(b), both duty ratios of the switches are smaller than 0.5, and both times taken by switching state 2 and switching state 3 are $v_{\rm cont3}T_s$. Thus, the time for state 4 is $(1 - 2v_{\rm cont3})T_s$. It follows that the average inductor voltage $\langle v_{L3}\rangle_{Ts}$ in this condition is

$$\begin{aligned}\langle v_{L3}\rangle_{Ts} &= \frac{\begin{array}{l}(|v_s|-v_{d_1})\,v_{\rm cont3}T_s \\ +(|v_s|-v_{d2})\,v_{\rm cont3}T_s \\ +(|v_s|-v_d)\,(1-2v_{\rm cont3})T_s\end{array}}{T_s} \\ &= |v_s| - (1-v_{\rm cont3})v_d. \end{aligned} \tag{12}$$

From (11) and (12), it can be found that whether control signal $v_{\rm cont3}$ is larger or smaller than 0.5, the average inductor voltage $\langle v_{L3}\rangle_{Ts}$ is always equal to $\langle v_{L3}\rangle_{Ts} = |v_s| - (1 - v_{\rm cont3})v_d$ even though two capacitor voltages are imbalanced $v_{d1} \neq v_{d2}$. Additionally, the result $\langle v_{L3}\rangle_{Ts} = |v_s| - (1 - v_{\rm cont3})v_d$ is the same as the average inductor voltage (1), which shows that the three-level SMR behaves similar to a conventional boost-type SMR even though two capacitor voltages are imbalanced. Therefore, the conventional multiloop control in Fig. 1(b) can be integrated into the proposed MIC to achieve the same PFC function for the three-level SMR. Due to the same average inductor voltage $\langle v_{L3}\rangle_{Ts}$, the control signal $v_{\rm cont}$ by the multiloop control in (2) can be extended to the MIC control signal $v_{\rm cont3}$, i.e.,

$$v_{\rm cont3} = v_{\rm cont} = 1 - \frac{\hat{V}_s\,|\sin(2\pi ft)|}{V_d^*}. \tag{13}$$

B. Output Voltage and Capacitor Voltages

When switch *SW*1 in Fig. 2 conducts, the diode current is zero, i.e., $i_{D1}(t) = 0$, and when switch *SW*1 blocks, the diode current is equal to the inductor current, i.e., $i_{D1}(t) = i_{L3}(t)$. Then, the average diode current $\langle i_{D1}\rangle_{Ts}$ within switching period T_s can be expressed in terms of duty ratio $v_{\rm cont3}$ and the average inductor current $\langle i_{L3}\rangle_{Ts}$. Thus

$$\langle i_{D1}\rangle_{Ts} = (1 - v_{\rm cont3})\,\langle i_{L3}\rangle_{Ts}\,. \tag{14}$$

Similarly, diode current i_{D2} equals zero and inductor current i_{L3} when switch *SW*2 conducts and blocks, respectively. Then, the average diode current $\langle i_{D2}\rangle_{Ts}$ can be expressed as

$$\langle i_{D2}\rangle_{Ts} = (1 - v_{\rm cont3})\,\langle i_{L3}\rangle_{Ts} = \langle i_{D1}\rangle_{Ts}\,. \tag{15}$$

It is clear that two diode currents have the same average value $\langle i_{D2}\rangle_{Ts} = \langle i_{D1}\rangle_{Ts}$. Assume that the average inductor current $\langle i_{L3}\rangle_{Ts}$ is well controlled to follow the rectified sinusoidal waveform $\langle i_{L3}\rangle_{Ts} = \hat{I}_s|\sin(2\pi ft)|$ in phase with input voltage $v_s(t)$. Then, by combining (13)(15), the average diode currents $\langle i_{D1}\rangle_{Ts}$ and $\langle i_{D2}\rangle_{Ts}$ can be rewritten as

$$\begin{aligned}\langle i_{D1}\rangle_{Ts} = \langle i_{D2}\rangle_{Ts} &= \frac{\hat{V}_s\hat{I}_s\sin(2\pi ft)^2}{V_d^*} \\ &= \frac{\hat{V}_s\hat{I}_s}{2V_d^*} - \frac{\hat{V}_s\hat{I}_s}{2V_d^*}\cos(4\pi ft). \end{aligned} \tag{16}$$

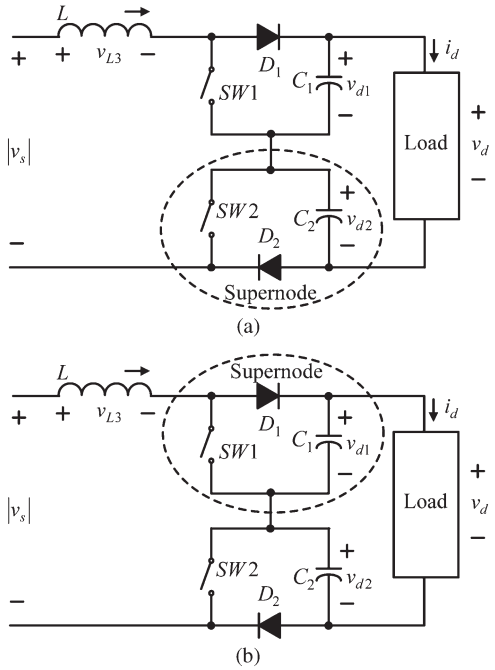

Fig. 6. Replotted circuit. (a) With lower boost unit regarded as a supernode. (b) With upper boost unit regarded as a supernode.

It is clear that the ac component in (16) must flow through capacitors C_1 and C_2, respectively. The average capacitor currents $\langle i_{C1}\rangle_{Ts}$ and $\langle i_{C2}\rangle_{Ts}$ are equal to

$$\langle i_{C1}\rangle_{Ts} = \langle i_{C2}\rangle_{Ts} = -\frac{\hat{V}_s\hat{I}_s}{2V_d^*}\cos(4\pi ft). \tag{17}$$

Therefore, the average voltage ripples across capacitors C_1 and C_2 can be expressed as

$$\langle v_{\rm rip1}\rangle_{Ts} \approx \frac{1}{C_1}\int \langle i_{C1}\rangle_{Ts}\,dt = -\frac{\hat{V}_s\hat{I}_s}{8\pi fC_1V_d^*}\sin(4\pi ft) \tag{18}$$

$$\langle v_{\rm rip2}\rangle_{Ts} \approx \frac{1}{C_2}\int \langle i_{C2}\rangle_{Ts}\,dt = -\frac{\hat{V}_s\hat{I}_s}{8\pi fC_2V_d^*}\sin(4\pi ft). \tag{19}$$

As shown in Fig. 6(a), the circuit in the dashed area can be considered a supernode. Then, the remaining circuit can be referred to as a boost converter with switch *SW1*. Similarly, the circuit in Fig. 6(b) can be seen as a boost converter with switch *SW2* by considering the supernode in the dashed area.

Since two boost converters have the circuit parameters and the same duty ratios and output voltage v_d is well regulated to voltage command V_d^*, from the average voltage ripples in (18) and (19), the average capacitor voltages can be represented as

$$\langle v_{d1}\rangle_{Ts} \approx \frac{V_d^*}{2} + \langle v_{\rm rip1}\rangle_{Ts} = \frac{V_d^*}{2} - \frac{\hat{V}_s\hat{I}_s}{8\pi fC_1V_d^*}\sin(4\pi ft) \tag{20}$$

$$\langle v_{d2}\rangle_{Ts} \approx \frac{V_d^*}{2} + \langle v_{\rm rip2}\rangle_{Ts} = \frac{V_d^*}{2} - \frac{\hat{V}_s\hat{I}_s}{8\pi fC_2V_d^*}\sin(4\pi ft). \tag{21}$$

It is noted that the dc components of the average capacitor voltages in (20) and (21) are independent of the capacitance; however, the average voltage ripples are highly related to the capacitance values. Consequently, the average output voltage can be expressed as

$$\langle v_d\rangle_{Ts} \approx V_d^* - \frac{\hat{V}_s\hat{I}_s(C_1+C_2)}{8\pi fC_1C_2V_d^*}\sin(4\pi ft). \tag{22}$$

C. Inductor Current Ripple

To simplify the analysis of the inductor current ripple, the identical capacitance values $C_1 = C_2$ and the balanced voltages are assumed. Similar to the steps for the above analysis of the average inductor voltage, the analysis is also divided into two conditions, i.e., $v_{\rm cont3} > 0.5$ and $v_{\rm cont3} < 0.5$. From the repeated waveforms, as shown in Fig. 5, current ripple Δi_{L3} can be equivalently calculated within each half switching period $0.5T_s$.

$v_{\rm cont3} > 0.5$*:* In Fig. 5(a), the time taken by switching state 1 is $(v_{\rm cont3} - 0.5)T_s$, and both switches conduct as shown in Fig. 4(a). The inductor voltage is $v_{L3} = |v_s|$, and thus, the rising rate of the inductor current is $|v_s|/L$.

Similarly, the falling rate of the inductor current is $(0.5v_d - |v_s|)/L$ in switching state 2 when switch *SW2* blocks. In Fig. 5(a), the time taken by switching state 2 is $(1 - v_{\rm cont3})T_s$. Therefore, within each half switching period $0.5T_s$, the inductor current ripple Δi_{L3} can be expressed by either the current rising rate $|v_s|/L$ or the current falling rate $(0.5v_d - |v_s|)/L$. Thus

$$\Delta i_{L3} = \frac{|v_s|}{L}(v_{\rm cont3} - 0.5)T_s = \frac{|v_s|}{Lf_s}(v_{\rm cont3} - 0.5) \tag{23}$$

$$\Delta i_{L3} = \frac{0.5v_d - |v_s|}{L}(1 - v_{\rm cont3})T_s = \frac{0.5v_d - |v_s|}{Lf_s}(1 - v_{\rm cont3}). \tag{24}$$

Combining (23) and (24) yields the expression of the current ripple Δi_{L3} in the three-level SMR, i.e.,

$$\begin{aligned}\Delta i_{L3} &= \frac{v_d}{Lf_s}(1 - v_{\rm cont3})(v_{\rm cont3} - 0.5)\\ &= -\frac{v_d}{Lf_s}\left(v_{\rm cont3} - \frac{3}{4}\right)^2 + \frac{v_d}{16Lf_s} \le \frac{v_d}{16Lf_s}.\end{aligned} \tag{25}$$

$v_{\rm cont} < 0.5$*:* In switching state 2, the inductor voltage is equal to $(|v_s| - 0.5v_d)$, and the current rising rate is $(|v_s| - 0.5v_d)/L$. In Fig. 5(b), the time taken by switching state 2 is $v_{\rm cont3}T_s$, and the current falling rate is $(v_d - |v_s|)/L$ at switching state 4 when both switches block. Thus, the remaining time for switching state 4 is $(0.5 - v_{\rm cont3})T_s$.

Therefore, within each half switching period $0.5T_s$, the inductor current ripple Δi_{L3} can be expressed by either the current rising rate $(|v_s| - 0.5v_d)/L$ or the current falling rate $(v_d - |v_s|)/L$. Thus

$$\Delta i_{L3} = \frac{|v_s| - 0.5v_d}{L}v_{\rm cont3}\,T_s = \frac{|v_s| - 0.5v_d}{Lf_s}v_{\rm cont3} \tag{26}$$

$$\Delta i_{L3} = \frac{v_d - |v_s|}{L}(0.5 - v_{\rm cont3})T_s = \frac{v_d - |v_s|}{Lf_s}(0.5 - v_{\rm cont3}). \tag{27}$$

TABLE I
SIMULATED PARAMETERS OF THE THREE-LEVEL SMR

Input voltage	$110V(rms)$, $50Hz$
Output voltage	$V_d^* = 300V$
Inductor	$0.5mH$
Carrier frequency	20kHz
Capacitor	$C_1 = C_2 = 1880\mu F$ equivalent capacitance $\approx 940\mu F$ (for capacitance-matched condition)
	$C_1 = 2240\mu F$, $C_2 = 1410\mu F$ equivalent capacitance $\approx 865\mu F$ (for capacitance-mismatched condition)
Voltage controller	$k_p = 0.1$, $k_i = 20$
Current controller	$k_p = 0.02$, $k_i = 10$

Eliminating the term $|v_s|$ in (26) and (27) yields the expression of current ripple Δi_{L3}, i.e.,

$$\Delta i_{L3} = \frac{v_d}{Lf_s} v_{\text{cont3}}(0.5 - v_{\text{cont3}}) = -\frac{v_d}{Lf_s}\left(v_{\text{cont3}} - \frac{1}{4}\right)^2 + \frac{v_d}{16Lf_s} \le \frac{v_d}{16Lf_s}. \quad (28)$$

From (25) and (28), the maximum current ripple $\Delta i_{L3,\max} = v_d/(16Lf_s)$ in the three-level SMR occurs at either $v_{\text{cont3}} = 1/4$ or $3/4$. It is clear that the maximum current ripple $\Delta i_{L3,\max} = v_d/(16Lf_s)$ is smaller than the maximum current ripple $\Delta i_{L,\max} = v_d/(4Lf_s)$ for the conventional boost-type SMR. It shows that the three-level SMR has smaller current ripple than the conventional boost-type SMR.

Additionally, the minimum current ripple for the three-level SMR is zero, i.e., $\Delta i_{L3,\min} = 0$, when control signal v_{cont3} equals either $1, 1/2$, or 0.

IV. SIMULATION RESULTS

In this section, some simulation results are provided, and the simulated parameters used in the three-level SMR are shown in Table I.

The capacitance-matched condition means that both capacitors have nominal capacitance 1880 μF. At the capacitance-mismatch case, the nominal capacitance of the upper capacitor is $C_1 = 2240$ μF, and the other is $C_2 = 1410$ μF. It is noted that the capacitance-mismatch case is not practical; however, it is helpful for the demonstration of the MIC performance.

The results under the capacitance-matched condition and the capacitance-mismatched condition are plotted in Fig. 7(a) and (b), respectively. The yielded input current i_s is sinusoidal in phase with input voltage v_s, and the dc components of the capacitor voltages are equal to half of voltage command $V_d^*/2 = 150$ V even in the capacitance-mismatched condition, as plotted in Fig. 7(b).

From (11) and (12), the equivalent inductor voltage $\langle v_{L3}\rangle_{Ts}$ in the three-level SMR is a function of output voltage v_d but not of the individual capacitor voltages v_{d1} and v_{d2}. With the same controller parameters, the current waveform i_s in Fig. 7(a) is similar to the current waveform i_s in the capacitance-mismatched condition in Fig. 7(b).

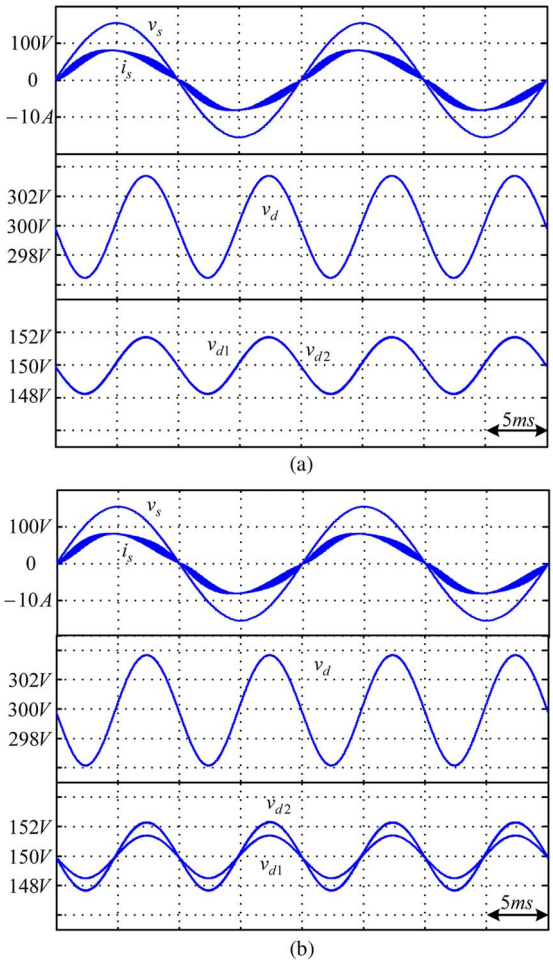

Fig. 7. Simulated results for the three-level SMR at 600 W. (a) Under capacitance-matched condition. (b) Under capacitance-mismatched condition.

The ripple across voltage v_d in Fig. 7(a) is smaller than that in Fig. 7(b) due to its larger equivalent capacitance in the capacitance-mismatched condition. In Fig. 7(a), both capacitor voltages possess the same voltage ripple. In Fig. 7(b), the voltage ripple across capacitor C_1 is smaller than that across capacitor C_2 due to the mismatched capacitance values.

However, the results show that the proposed MIC is able to achieve the PFC function in the three-level SMR without the capacitor voltage balancing loop.

In order to observe the MIC performance of the transient operation, the simulated results during the load regulation are plotted in Fig. 8. The output power changes from 300 to 600 W due to the change of the load resistor from 300 to 150 Ω. In Fig. 8(a), the sinusoidal input current i_s is always in phase with input voltage v_s, and output voltage v_d is well regulated to the command 300 V during the transient period. Both the two capacitor voltages in Fig. 8(a) have the same response in this capacitance-matched condition.

The results in the capacitance-mismatched condition are plotted in Fig. 8(b). The input current waveform and the output voltage are still well controlled. In addition, capacitor voltage v_{d2} possesses larger voltage dip than capacitor voltage v_{d1} because capacitance C_2 is smaller than capacitance C_1. However, both capacitor voltages are well regulated to half command

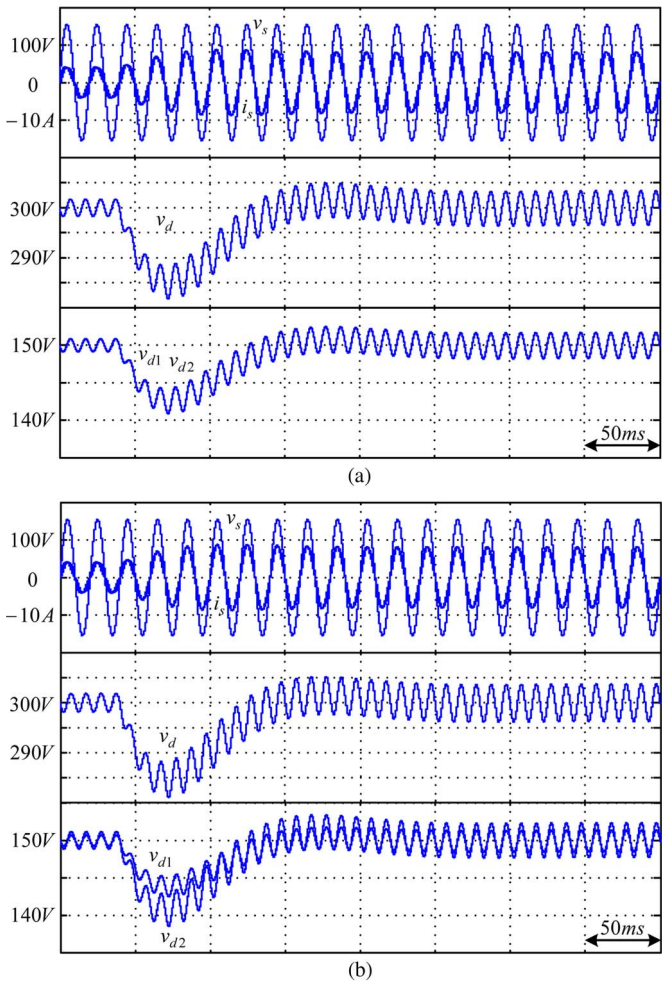

Fig. 8. Simulated waveforms during load change from 300 to 600 W. (a) Under capacitance-matched condition. (b) Under capacitance-mismatched condition.

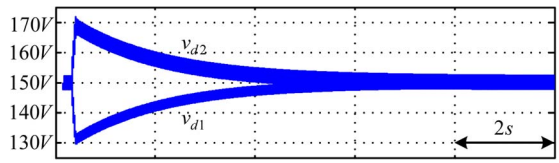

Fig. 9. Simulated waveforms when a resistor is suddenly connected across capacitor C_1 and then removed from capacitor C_1.

150 V without the voltage balancing loop. It is also noted that the current waveform i_s in Fig. 8(b) is similar to the current waveform i_s in Fig. 8(a) even during the temporary voltage imbalance in Fig. 8(b).

To understand voltage balance between two capacitors, a 400-Ω resistor is suddenly connected across capacitor C_1, and then, the resistor is removed from capacitor C_1. The simulated waveforms are plotted in Fig. 9.

The voltage ripple in capacitor voltage v_{d1} is smaller than that in voltage v_{d2}, which shows that the simulation is performed under the capacitance-mismatched condition. Capacitor voltage v_{d1} quickly drops to near 130 V due to the suddenly connected resistor, and capacitor voltage v_{d2} increases to near 170 V due to the voltage control loop in MIC. After removing the connected resistor, two capacitor voltages are gradually

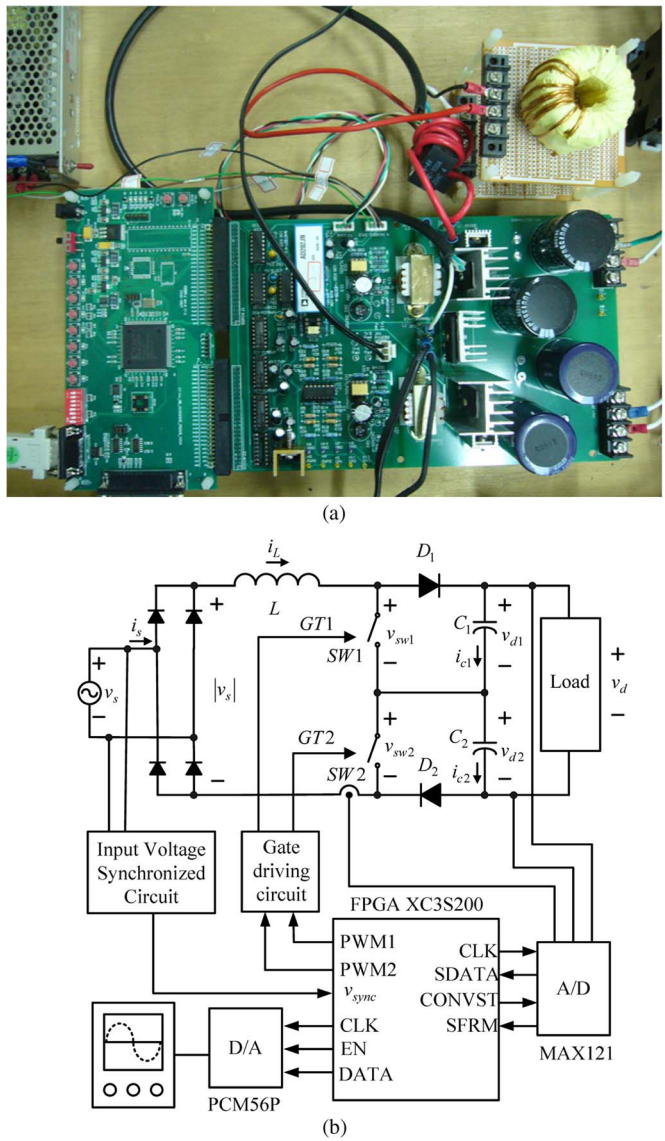

Fig. 10. (a) FPGA and the circuit board. (b) System block diagram.

balanced. It is clear that the results in Figs. 8 and 9 show that for the proposed MIC, the capacitor voltages are finally balanced without the balancing control loop and that voltage imbalance has no effect on the current waveforms.

V. Experimental Results

The proposed MIC had been implemented in a field-programmable gate array (FPGA)-based system, as shown in Fig. 10(a) and (b) shows the system block diagram of the experimental implementation. Due to the no-A/D and no-D/A functions in commercial FPGA XC3S200 chip, an external A/D converter is used to sense the output voltage, and a zero-crossing detecting circuit is used to detect the zero-crossing of the input voltage. Some D/A converters are used to show the control variables of the implemented MIC in the scope. The nominal parameters are the same as those in Table I.

In practice, the mismatch of two capacitor equivalent series resistors and two duty ratio exists. Therefore, some voltage imbalance can be observed even in the capacitance-matched

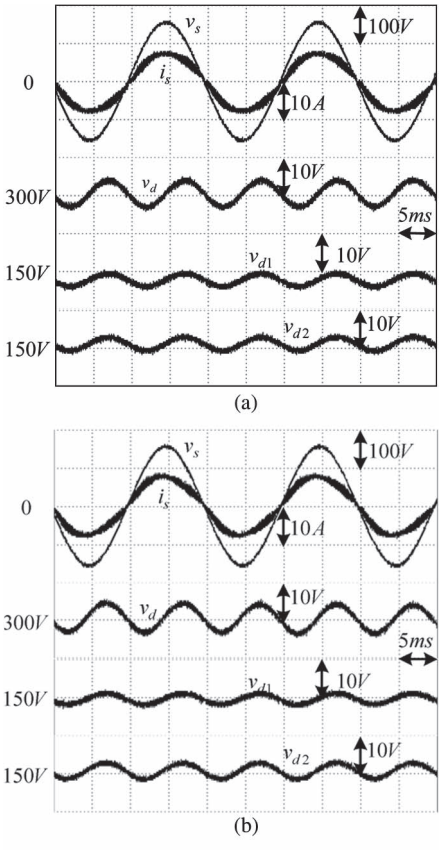

Fig. 11. Experimental results for the three-level SMR at 600 W. (a) Under capacitance-matched condition. (b) Under capacitance-mismatched condition.

TABLE II
HARMONICS OF THE INPUT CURRENT

Harmonics	Class A	Class D	Fig. 11(a)	Fig. 11(b)
Fundamental	X	X	5.6025A	5.6791A
3	4.60A	4.08A	0.2456A	0.2720A
5	2.28A	2.28A	0.0508A	0.0909A
7	1.54A	1.20A	0.0419A	0.0910A
9	0.80A	0.60A	0.0307A	0.0806A
11	0.66A	0.42A	0.0299A	0.0614A
13	0.42A	0.36A	0.0283A	0.0503A
15	0.30A	0.31A	0.0311A	0.0488A
17	0.26A	0.27A	0.0389A	0.0606A
19	0.24A	0.24A	0.0502A	0.0660A
21	0.18A	0.22A	0.0509A	0.0713A
PF			0.994	0.988

condition. Fig. 11(a) and (b) shows the experimental steady-state waveforms at a 600-W power level for the capacitance-matched condition and the capacitance-mismatched condition, respectively.

Both output voltage v_d is well regulated to 300 V and input current i_s is sinusoidal in phase with input voltage v_s. Small deviation near 2–3 V from half voltage command 150 V in two capacitor voltages can be also found even in the capacitance-matched condition, as shown in Fig. 11(a).

In addition, the same capacitor voltage ripples can be found in Fig. 11(a), and different capacitor voltage ripples can be found in Fig. 11(b). It means that the derivations of voltage ripples in (20) and (21) are verified. Table II lists the comparison of harmonics of the input current and the IEC-61000-3-2 standard.

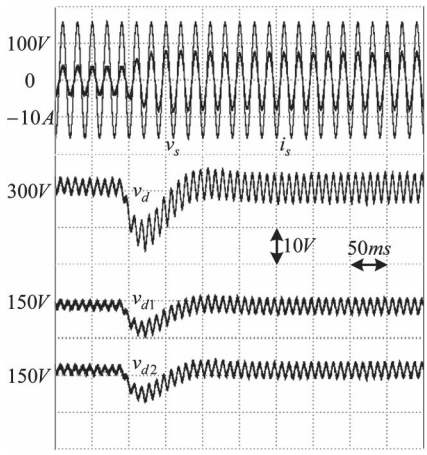

Fig. 12. Experimental waveforms under the capacitance-matched condition.

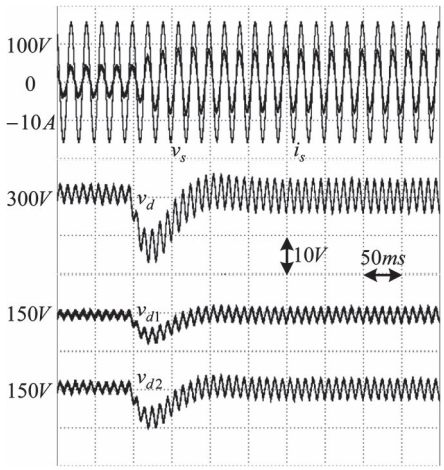

Fig. 13. Experimental waveforms under the capacitance-mismatched condition.

The current harmonics yielded by the proposed MIC is below the standard even in the capacitance-mismatched condition in Fig. 11(b).

The transient responses under the capacitance-matched condition are plotted in Fig. 12. Output voltage v_d is well regulated to 300 V, and input current i_s keeps sinusoidal in phase with input voltage v_s during the load regulation. It can be found that the experimental results in Fig. 12 are similar to the simulation results in Fig. 8(a). The voltage difference between two capacitor voltages is near 4 V and can be accepted in practice.

The transient responses under the capacitance-mismatched condition are plotted in Fig. 13. All three voltages v_d, v_{d1}, and v_{d2} are well regulated during the transient period. Because capacitance C_1 is larger than capacitance C_2, capacitor voltage v_{d2} has larger voltage dip than capacitor voltage v_{d1}. However, the voltages are finally balanced without the voltage balancing loop.

Note that the first two plots, i.e., i_s and v_d, in Fig. 13 are close to those in Fig. 12. It shows that the proposed MIC is able to achieve the PFC function without the voltage balancing loop even though voltage imbalance temporarily exists.

To understand the ability to balance the capacitor voltages, a 400-Ω resistor is suddenly connected across capacitor C_1.

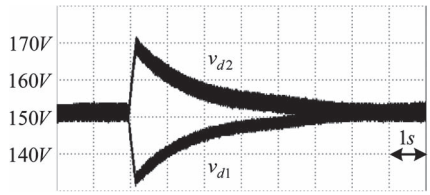

Fig. 14. Experimental waveforms when a resistor is suddenly connected across capacitor C_1 and then removed.

TABLE III
MEASURED INPUT POWER, POWER LOSS, EFFICIENCY, AND POWER FACTOR FOR THE CONVENTIONAL BOOST SMR AND THREE-LEVEL SMR

Three-level SMR	Input power (W)	304.3	406.9	522.0	617.5
	Output power (W)	288.5	385.1	493.4	582.3
	Efficiency (%)	94.8	94.6	94.5	94.3
	Power loss(W)	15.8	21.8	28.7	35.2
	Power factor	0.975	0.984	0.990	0.994
Boost SMR	Input power (W)	316.6	402.4	513.7	602.3
	Output power (W)	294.0	375.6	479.8	561.6
	Efficiency (%)	92.9	93.3	93.4	93.2
	Power loss(W)	22.6	26.8	34.0	40.7
	Power factor	0.771	0.828	0.861	0.891

Then, the connected resistor is removed. The experimental waveforms are plotted in Fig. 14.

The voltage ripple in capacitor voltage v_{d1} is smaller than that in voltage v_{d2}, which shows that the waveforms are measured under the capacitance-mismatched condition. Capacitor voltage v_{d1} quickly drops to near 130 V due to the connected resistor, and capacitor voltage v_{d2} increases to near 170 V due to the voltage control loop. After removing the connected resistor, two capacitor voltages are gradually balanced. Therefore, the three-level SMR with the proposed MIC possesses the ability to balance the capacitor voltages; however, it takes several seconds to balance the voltages.

For the three-level SMR, the measured power loss, efficiency, and power factor at various power levels are tabulated in Table III. For comparison, the measured values for the conventional boost-type SMR with the same inductor and the same switching frequency are also tabulated.

From Table III, the three-level SMR yields less power loss than the conventional boost-type SMR, and the former possesses higher efficiency than the latter. It clearly shows that the three-level SMR possesses higher efficiency than the conventional boost-type SMR.

In addition, the current ripple in the three-level SMR is smaller than that in the conventional SMR, and the power factor of the three-level SMR is higher than that of the conventional SMR.

The results at 210 V (600 W) and 265 V (400 W) are plotted in Fig. 15(a) and (b), respectively. The results show that the proposed MIC is able to work at high line voltages.

From the provided simulation and experimental results, the proposed MIC is able to achieve the PFC function without adding the voltage balancing control loop. The results show that the three-level SMR in ac/dc applications takes several seconds to automatically balance the capacitor voltages.

Because the time taken to balance the voltages is several seconds in this case, adding the voltage balancing loop is sometimes required.

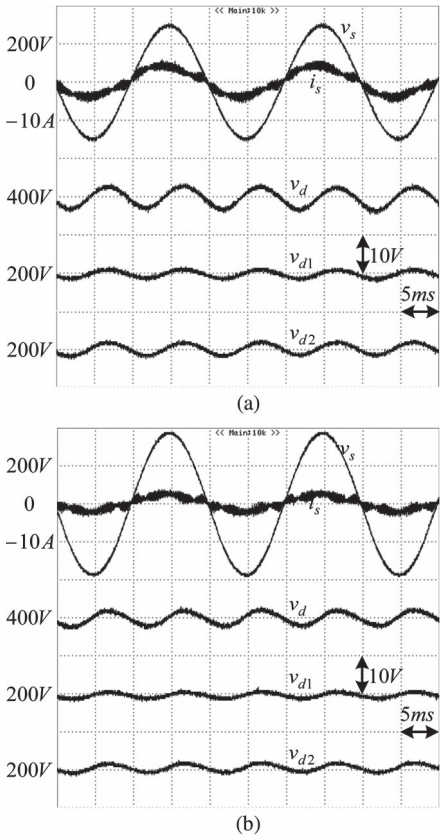

Fig. 15. Experimental results for the three-level SMR. (a) At 210 V and 600 W. (b) At 265 V and 400 W.

Furthermore, some other simulations and experiments for the three-level boost converter in dc/dc applications had been done; however, the results show that the converter is not able to balance the capacitor voltages automatically without the voltage balancing control loop. Hence, the proposed simple MIC cannot be extended to the three-level boost converter in dc/dc applications because the voltage balancing loop is still required.

VI. CONCLUSION

In this paper, the results show that the interleaved three-level SMR with the interleaved PWM scheme behaves similar to a conventional boost-type SMR. Its performance of the current shaping function does not degrade even when the two capacitor voltages are imbalanced. The MIC for the three-level SMR in ac/dc applications has been first proposed.

The proposed MIC is implemented in an FPGA-based system. The measured results show that the proposed MIC is able to achieve the desired PFC function, and the capacitor voltages are automatically balanced without adding the voltage balancing loop.

The commercial PFC ICs have the multiloop function but do not integrate the voltage balancing loop. However, based on this paper, the commercial PFC ICs can be used in the three-level SMRs if the temporary voltage imbalance is acceptable during the system operation.

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