Boundary Conduction Mode Controlled Power Factor Corrector With Line Voltage Recovery and Total Harmonic Distortion Improvement Techniques

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***Abstract*—The proposed line voltage recovery (LVR) and the total harmonic distortion improvement (THDI) technique improve power factor (PF) and total harmonic distortion (THD) over a wide line voltage range in boundary conduction mode controlled power factor corrector (PFC). The LVR detects the input line root-mean-square voltage to generate the digital equivalent code to the THDI for optimizing the THD by tuning the on-time value at different line voltages. In addition, the LVR and the THDI provide a feedforward path to reduce the ripple of the feedback voltage for further improving the THD. Therefore, the PFC controller can keep high PF and low THD over a wide line voltage. Experimental results demonstrate that the peak PF value is 0.998 and the minimum THD is 1.7% by the test circuit fabricated in a TSMC 800-V ultrahigh-voltage process with the universal line voltage range of 90–264 V.**

***Index Terms*—Line voltage recovery (LVR), power factor (PF), total harmonic distortion (THD).**

I. Introduction

GREEN POWER becomes more important in the world due to the lack of energy. In green power designs, high-quality ac power conversion aims to enhance power utilization efficiency of the ac power supply, minimize power loss, and improve regulation. For increasing the power utilization efficiency of the ac power supply, the demanded power factor correction (PFC) converter can shape the input current of offline power supplies to be in phase with the line voltage. In addition, the total harmonic distortion (THD) of the line current, which also determines the quality of power source, is expressed in Fig. 1 and the following equation:

$$\mathrm{THD} = \left(\frac{\cos^2 \theta}{\mathrm{PF}^2} - 1 \right)^{1/2} \tag{1}$$

where power factor PF is the ratio of the real power to the apparent power, and θ is the phase angle between the line current and voltage.

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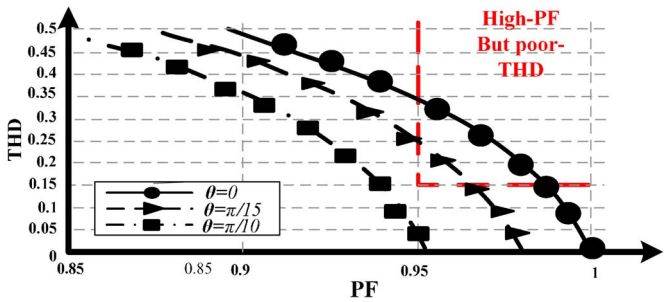

Fig. 1. Diagram of THD versus PF.

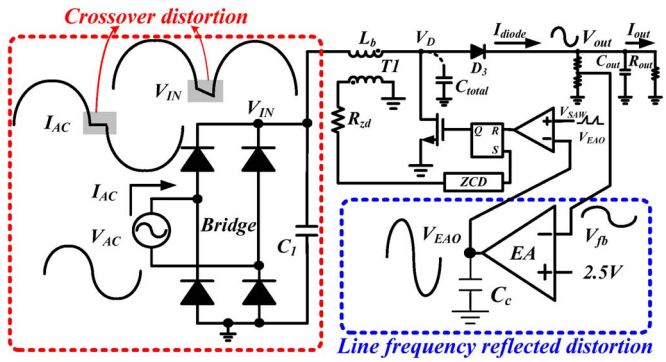

Fig. 2. Two major THD-deteriorated contributors in the conventional PFC with BCM control.

Interestingly, the relationship between PF and THD reveals that THD is still poor even if PF is high. That is to say, for high-quality power supply, both the PF and the THD are important. The harmonic currents will increase power losses on the transmission line and cause electrical equipment damages. Therefore, the THD needs to be decreased for high-quality power supply even if the PF is high. There are safety standards that determine the maximum THD of electrical products in many countries, such as EN61000-3-2. In other words, improving THD becomes an essential requirement for electrical products.

Basically, two major THD-deteriorated contributors are shown in Fig. 2 in a conventional PFC boost converter with boundary conduction mode (BCM) control [1]–[3]. One is the crossover distortion caused by the forward voltage of the diodes in the bridge and parasitic capacitances C_{total}, which includes the parasitic capacitance of D_3 and power nMOSFET. The other is the line frequency reflected distortion. The frequency

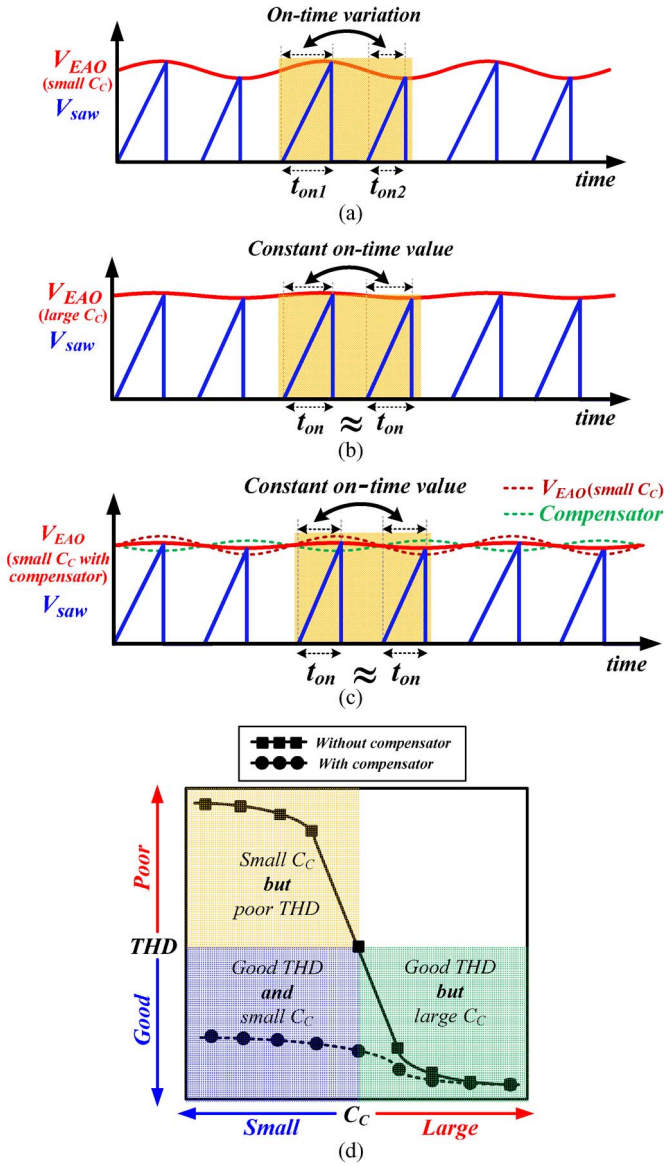

Fig. 3. (a) On-time variation is caused by the line frequency reflected distortion. (b) Variation of on-time value can be reduced by large C_C. (c) Variation of on-time value can be reduced by the compensator even with small C_C. (d) Relationship between C_C and THD.

of the PFC output ripple is twice of the ac line. The reflected output ripple is fed into the feedback loop so that the output of the error amplifier contains the voltage ripple with twice the line frequency. The ripple brings the variation of on-time within an ac cycle, as depicted in Fig. 3(a). The on-time variation goes against constant on-time control, which is the general demand for the PFC boost converter with BCM control to lower the THD for satisfying standard requirements [4]. Hence, THD is deteriorated short of expected specifications due to line frequency reflected distortion. In general, a large compensated capacitor C_C is used to keep the bandwidth within 20 Hz to reduce the gain of the error amplifier at twice the line frequency such that the PFC boost converter can operate with constant on-time control, as shown in Fig. 3(b) [5]. However, the solution occupies a large footprint area. In this paper, the ripple compensator is proposed to suppress the output ripple of the error amplifier. Therefore, constant on-time can be ensured even if a small C_C is adopted, as illustrated in Fig. 3(c). The relationship between C_C and THD is depicted in Fig. 3(d). In conventional PFC, the smaller the selected C_C is, the poorer the THD performance will be. With the contribution of the ripple compensator, the small footprint area and the low THD can be simultaneously achieved.

On the other hand, a conventional BCM controller usually uses a shaping skill to minimize crossover distortion [6]. However, the multiplier, which multiplies the output of the error amplifier by feedforward input voltage for duty cycle generation, dissipates much power. Therefore, to alleviate both THD deteriorated issues, which contain crossover distortion and line frequency reflected distortion, line voltage recovery (LVR) circuit and total harmonic distortion improvement (THDI) techniques are proposed in this paper. THDI modulates on-time value based on the digital correction codes generated by LVR circuit to improve crossover distortion. Simultaneously, LVR and THDI form a feedforward path to reduce line frequency reflected distortion. Consequently, the two major THD-deteriorated contributors can be simultaneously and effectively alleviated to get high PF and low THD over a wide input line voltage range of 90–264 V.

This paper is organized as follows. The proposed architecture and the circuit implementation are illustrated in Sections II and III, respectively. Simulation and experimental results are shown in Section IV. Finally, a conclusion is made in Section V.

II. Proposed Architecture With the LVR and the THDI

As shown in Fig. 4(a), the inductor L_b can store enough energy during inductor charging phase normally. During inductor discharging phase, as shown in Fig. 4(b), total capacitance at node V_D, C_{total}, which includes the parasitic capacitance of D_3 and power nMOSFET, can be successfully charged up to the required voltage. The required voltage is the output voltage V_{out} plus the turn-on voltage of diode D_3. Once diode D_3 is turned on, the energy stored in the inductor is delivered to the output, as shown in Fig. 4(c). Unfortunately, when the line voltage V_{AC} is near the zero-crossings, the inductor can still store the energy during inductor charging phase. Nevertheless, the stored energy is not enough to charge C_{total} up to the required voltage during inductor discharging phase. As a result, diode D_3 will not be turned on. The energy is confined and dissipated in the tank circuit, which is composed of C_{total}, C_1, and L_b, and causes a resonance phenomenon, as shown in Fig. 4(d). The phenomenon is kept for an interval until the absolute value of the line voltage is larger than the voltage of V_{IN}, which is the rectified line voltage.

During this interval, V_{IN} decreases at a slower rate determined by the losses of the power nMOSFET and the tank circuit. However, the line voltage decreases at a faster rate. Thus, the diode of the bridge rectifier cannot be turned on, and the flat portion in the line current I_{AC} happens, as illustrated in Fig. 5. This distortion is called "crossover distortion," which increases the number of the total harmonics in I_{AC} greatly. In other words, the THD becomes serious.

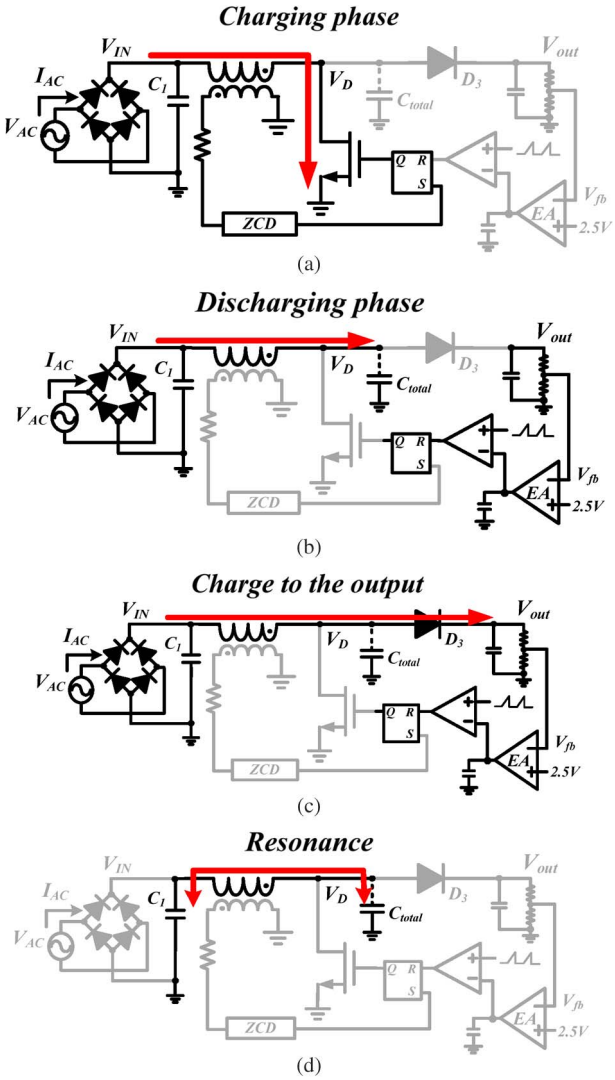

Fig. 4. (a) Charging phase of the PFC boost converter. (b) Discharging phase of the PFC boost converter. (c) Energy charges to the output when the line voltage is high enough. (d) Energy is confined in the resonant tank when the line voltage is near zero-crossings.

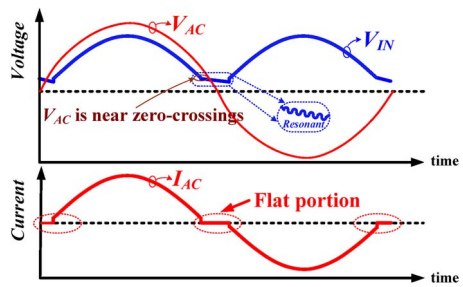

Fig. 5. Line voltage and current waveforms of crossover distortion phenomenon.

If the inequality shown in (2) is simply conformed, it means that the energy stored in the charging phase is not high enough to conduct diode D_3 in the discharging phase

$$\frac{1}{2}L_b \cdot \left[\sqrt{2}I_{\mathrm{AC,rms}}\sin(\pi-\phi_d)\right]^2 \le \frac{1}{2}C_{\mathrm{total}} \cdot (V_{\mathrm{out}}+V_{\mathrm{diode}})^2 \tag{2}$$

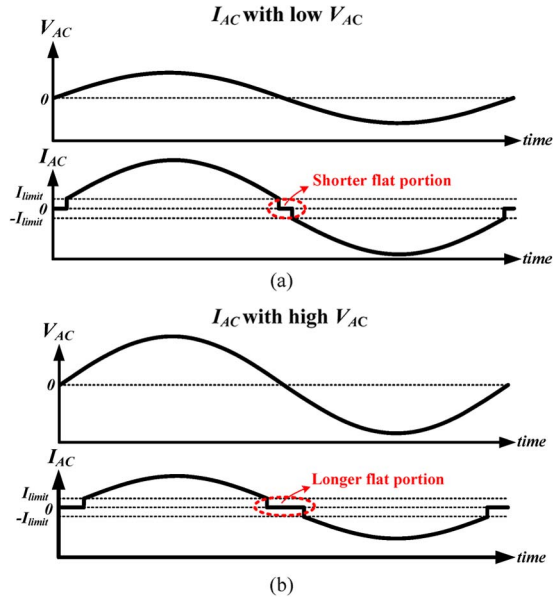

Fig. 6. Waveforms of the line current with (a) low line RMS voltage and (b) high line RMS voltage.

where ϕ_d is the crossover distortion angle, which indicates that I_{AC} starts away from the ideal sinusoidal wave; V_{diode} is the forward voltage of D_3; and $I_{\mathrm{AC,rms}}$ is the RMS value of the line current.

Here, $I_{\mathrm{AC,rms}}$ can be expressed as (3) based on the relationship between power and current. $V_{\mathrm{AC,rms}}$ and $P_{\mathrm{AC,rms}}$ are the RMS values of the line voltage and input power, respectively, i.e.,

$$I_{\mathrm{AC,rms}} = \frac{P_{\mathrm{AC,rms}}}{V_{\mathrm{AC,rms}}}. \tag{3}$$

The limiting current I_{limit}, which is defined as the required current that can charge C_{total} up to the required voltage, is derived as (4). If the line current is lower than I_{limit}, the crossover distortion, which results in the flat portion in the line current, will happen, i.e.,

$$I_{\mathrm{limit}} = \sqrt{\frac{C_{\mathrm{total}}}{L_b}} \cdot (V_{\mathrm{out}}+V_{\mathrm{diode}}). \tag{4}$$

Using the information of the line voltage to modulate the on-time value of the power nMOSFET can alleviate crossover distortion [7]. At a high level of the line voltage, the on-time value is slightly shortened. Contrarily, the on-time value is extended at the region of low line voltage near the zero-crossings. Therefore, the inductor current near the zero-crossings is increased to break through I_{limit}. The THD performance can be improved by compressing the flat portions.

However, good THD performance for universal input line voltage is unable to be achieved if the modulated on-time value is not adapted to the variation of the input line RMS voltage. With fixed output power, higher input line RMS voltage results in lower line current and larger flat portion, as depicted in Fig. 6(a). On the contrary, lower input line RMS voltage results in higher line current and smaller flat portion, as depicted in

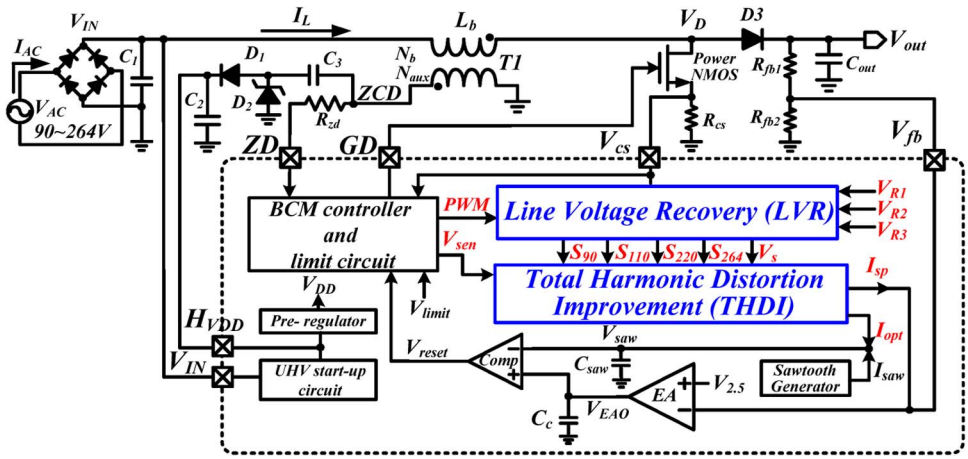

Fig. 7. Proposed BCM architecture with LVR and THDI.

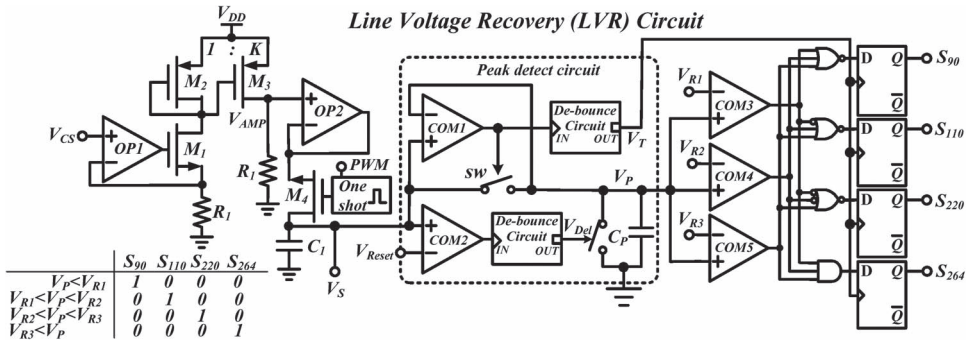

Fig. 8. Circuit implementation of the proposed LVR circuit.

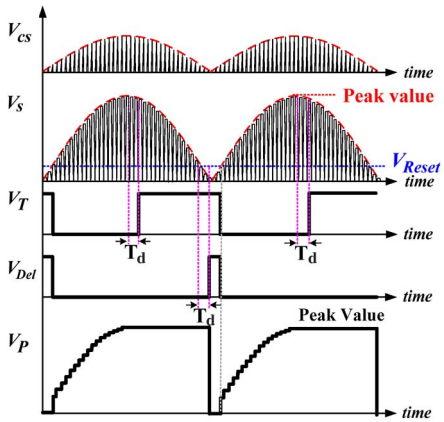

Fig. 9. Detailed operation waveform of the proposed LVR.

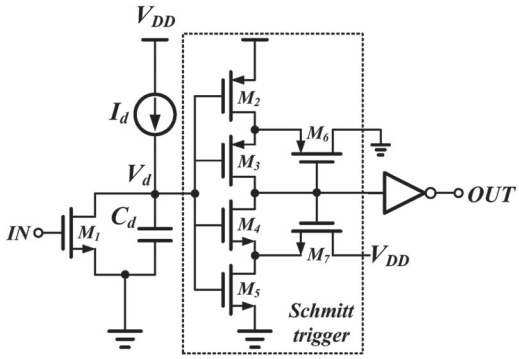

Fig. 10. Circuit implementation of the debounce circuit.

Fig. 6(b). The period of the flat portion, i.e., T_f, which results from the crossover distortion, is shown as

$$T_f = \frac{\phi_d}{2\pi \cdot f_{\text{line}}} \approx \frac{\sqrt{2}}{4} \cdot \frac{I_{\text{limit}} \cdot V_{\text{AC,rms}}}{f_{\text{line}} \cdot P_{\text{AC,rms}}} \tag{5}$$

where

$$\phi_d \approx \frac{\sqrt{2}}{2} \cdot I_{\text{limit}} \cdot \frac{V_{\text{AC,rms}}}{P_{\text{AC,rms}}}$$

where f_{line} is the line frequency. When the line RMS voltage is high, the crossover distortion becomes serious. Thus, the crossover distortion needs to be adaptively improved according to different line RMS voltages such that the THD can be maintained within a quite low level.

In addition, even if the modulated value of the on-time makes the flat portion becomes shorter gradually, the waveform of the line current is unlike the ideal sinusoid waveform and, thus, may distort the line current [8]. Thus, the level of the modulated on-time value has to be carefully designed at different line voltages to get good THD performance.

Fig. 7 shows the architecture of the proposed PFC boost converter, which is operating in BCM control in low-power applications. LVR can detect the input line RMS voltage to generate the digital correction codes, namely, S_{90}, S_{110}, S_{220}, and S_{264}, to THDI for optimizing the THD by tuning the

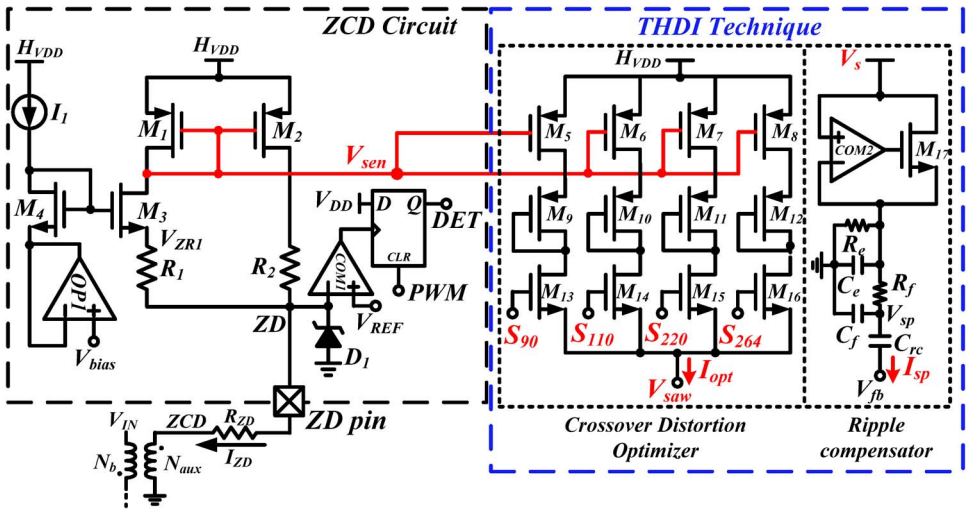

Fig. 11. Schematic of the ZCD and the THDI technique.

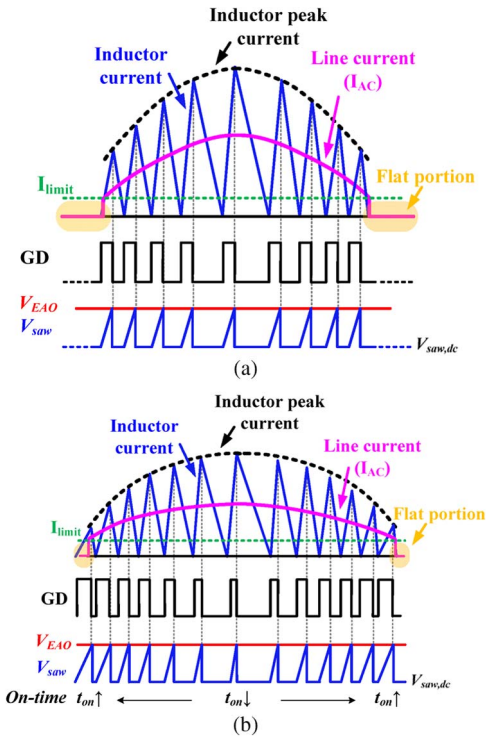

Fig. 12. (a) Control mechanism of a conventional PFC controller. (b) Control mechanism of the proposed PFC controller with the THDI technique.

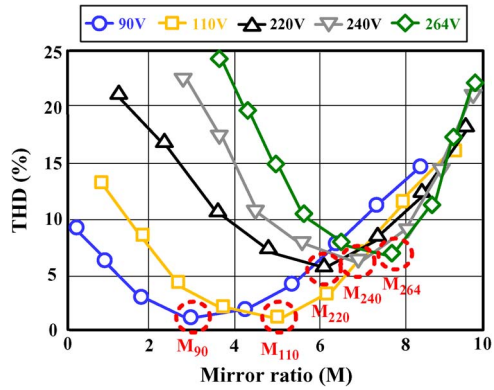

Fig. 13. Relationship between the THD and the mirror ratio at different line RMS voltages.

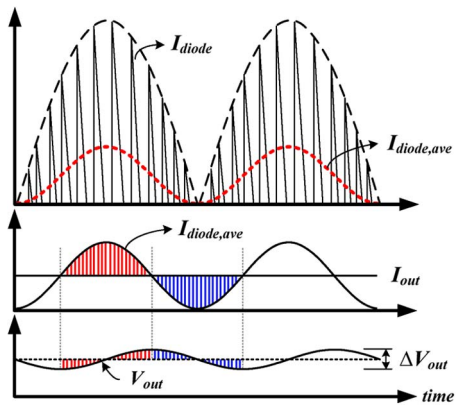

Fig. 14. Relationship between the diode current and the output voltage.

on-time value at different line RMS voltages. In addition, LVR and THDI provide a feedforward path to reduce the ripple of the feedback voltage for decreasing THD. Therefore, high PF and low THD can be concurrently achieved over a wide range of the line voltage by the proposed method.

III. Circuit Implementation

A. Proposed LVR Circuit

According to different line voltages, the THD should be improved by different on-time values. In general, the peak value of the rectified line voltage $V_{\rm IN}$ can indicate the RMS line voltage. In [9], one resistive divider is used to detect the input line RMS voltage. Although the method can detect the input line RMS voltage successfully, it needs extra pins and discrete devices such that the efficiency is deteriorated and the cost increases. The proposed LVR circuit in Fig. 8 can use the inductor current sensing signal $V_{\rm CS}$, which is used for over inductor current protection originally, to reconstruct the sinusoidal-wave tendency of the line voltage and judge the input line RMS voltage. Since the LVR does not need extra pins and discrete resisters, the power consumption and cost can be reduced.

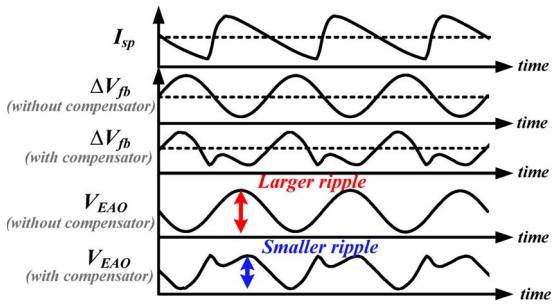

Fig. 15. Ripple of the feedback voltage and the output ripple of the error amplifier with and without the proposed ripple compensator.

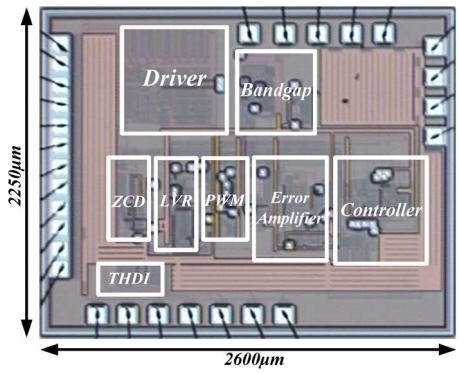

Fig. 16. Chip micrograph of the proposed PFC controller LVR and the THDI.

During the on-time period, the power nMOSFET is switched on, and then, the inductor current flows through the sensing resistor $R_{\rm CS}$ to obtain $V_{\rm CS}$. Without the on-time modulation of THDI, $V_{\rm CS}$ can be expressed as

$$V_{\rm CS} = \frac{V_{\rm IN}}{L_b} \times R_{\rm CS} \times t_{\rm on,fix} = \frac{2 \cdot V_{\rm IN} \cdot R_{\rm CS} \cdot P_O}{V_{\rm rms}^2 \cdot \eta} \quad (6)$$

where $V_{\rm IN}$ is the rectified line voltage, L_b is the inductor value, P_O is the output power, $V_{\rm rms}$ is the input line RMS voltage, η is the conversion efficiency, and $t_{\rm on,fix}$ is the on-time value of the power nMOSFET before modulation.

Since the on-time value varies with the input line RMS voltage $V_{\rm rms}$ and the output power P_O, the sinusoidal-wave tendency of the line voltage is unable to be obtained by $V_{\rm CS}$ directly. Furthermore, the range of $V_{\rm CS}$ is too large to use the differentiator [10] to reconstruct the line voltage. Instead of the on-time value, a fixed sampling time $t_{\rm sample}$ is adopted to generate V_S in the proposed LVR. Therefore, the dependence on the input line RMS voltage $V_{\rm rms}$ and the output power P_O can be removed. V_S can reconstruct the sinusoidal-wave tendency of the line voltage successfully, as shown in

$$V_S = K \times \frac{V_{\rm IN}}{L_b} \times R_{\rm CS} \times t_{\rm sample} \propto V_{\rm IN} \propto |V_{\rm AC}| \quad (7)$$

where K is the ratio of signal amplification.

In Fig. 8, the transistors M_2 and M_3 form a current mirror to amplify $V_{\rm CS}$ by K times and generate $V_{\rm AMP}$. V_S can be obtained by sampling $V_{\rm AMP}$ with a fixed sampling time $t_{\rm sample}$, which is generated by triggering the one shot circuit with a pulsewidth modulation signal, through the sampling switch M_4. Thus, the sinusoidal-wave tendency of the line voltage is correctly reconstructed. Moreover, the peak detector circuit detects the peak value of V_S to judge the input line RMS voltage. The comparator COM1 decides the status of the switch sw. When sw turns on, C_P samples the information of V_S. Once V_S is smaller than V_P, sw turns off, and V_P holds the value previously sampled. Consequently, V_P keeps the peak value of V_S within a half ac cycle until the reset signal $V_{\rm Del}$ rises, as shown in Fig. 9.

TABLE I
DESIGN SPECIFICATIONS OF THE PROPOSED PFC WITH LVR AND THDI TECHNIQUES

Technology	TSMC 0.5μm 800V UHV
Input line voltage range (V_{AC})	90~264V (rms value) / 60 Hz
Output voltage (V_{out})	400V
Primary inductor (L_b)	460μH
Primary winding turns (N_b)	60T
Auxiliary winding turns (N_{aux})	8T
Output capacitor (C_{out})	68μF/450V
Output power (P_{out})	90 W
Switching frequency (f_{sw})	35 kHz ~ 250 kHz
Bandwidth (BW)	20 Hz
Feedback resistors (R_{fb1}/R_{fb2})	795 kΩ/5 kΩ
Sensing resistor (R_{cs})	0.15 Ω
Total harmonic distortion (THD)	1.7% (Minimum)
Power factor (PF)	0.998 (Maximum)
Efficiency	94.8% (Maximum)

V_T indicates whether the peak value is detected or not. While V_S is smaller than V_P over the debounce time T_d, which is produced by the debounce circuit, V_T signifies the calculation of the line RMS voltage. Comparing V_P and the reference voltages V_{R1}–V_{R3} sorted by increasing order, the level of the input line RMS voltage can be successfully detected. By synchronization of V_T, the 4-bit digital equivalent code, which is composed of S_{90}, S_{110}, S_{220}, and S_{264}, can be generated to indicate the input line RMS voltage. The truth table is shown at the bottom left in Fig. 8. For example, if the 4-bit digital equivalent code shows "0100," the input line RMS voltage is 110 V.

Since V_S returns to zero during every switching cycle, the debounce time T_d has to be carefully designed to avoid generating incorrect signals. The debounce circuit, as depicted in Fig. 10, is used to avoid abnormal operation and noise interference. When the input signal changes from high to low, the current I_d will charge the capacitor C_d. The debounce time is determined by I_d and C_d. The hysteresis window is formed by the Schmitt trigger, the transistors M_2–M_7. If the node voltage V_d can be higher than the upper bound of the hysteretic window and this condition can be longer than the debounce time, the output signal will be changed. Careful definition of the debounce time and the hysteresis window can ensure a robust system.

B. Proposed THDI Technique

The proposed THDI technique, as shown in Fig. 11, is composed of the crossover distortion optimizer and the ripple compensator. The proposed crossover distortion optimizer conquers

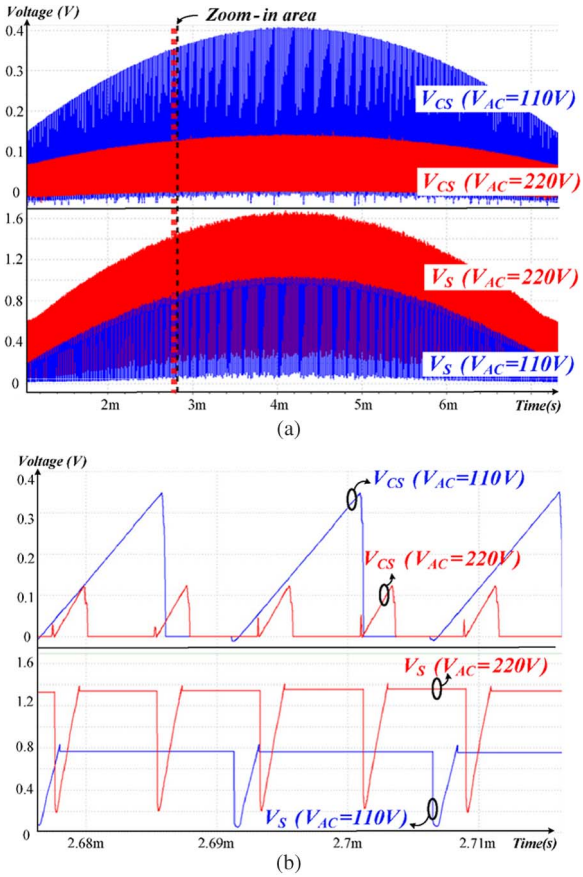

Fig. 17. (a) Simulation waveforms of the LVR circuit. (b) Zoom-in waveforms.

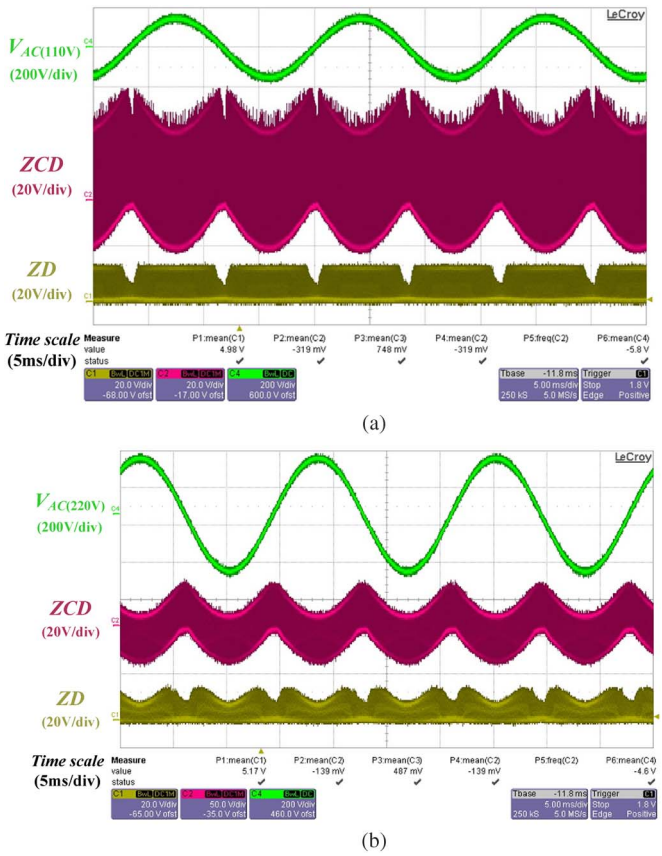

Fig. 18. Measured waveforms of the ZCD circuit at the input line RMS voltages of (a) 110 V and (b) 220 V.

two major drawbacks for THD improvement in [2] and [3]. First, the requirement of extra resistors for on-time modulation deteriorates the efficiency of the PFC boost converter. Second, the THD performance cannot be ensured with different line RMS voltages.

The proposed crossover distortion optimizer alleviates the crossover distortion at different line RMS voltages without extra pin and discrete devices. Instead, the zero-current detection (ZCD) circuit, which is essential for the BCM control, is utilized. When the power nMOSFET is turned on, the voltage of ZCD node $V_{\rm ZCD}$ is shown as

$$V_{\rm ZCD} = -\frac{V_{\rm IN} \cdot N_{\rm aux}}{N_b} \tag{8}$$

where N_b and $N_{\rm aux}$ are the primary and auxiliary winding turns, respectively.

The transistors M_1–M_3 and the resistors R_1 and R_2 of the ZCD circuit form a negative feedback to clamp the voltage of the ZD pin to be $V_{\rm ZD,clamp}$, which is higher than 0 V when the power nMOSFET is turned on. Therefore, the current $I_{\rm ZD}$ can be expressed as

$$I_{\rm ZD} = \frac{V_{\rm ZD,clamp} - V_{\rm ZD}}{R_{\rm ZD}} = \frac{V_{\rm ZD,clamp} + \frac{V_{\rm IN} \cdot N_{\rm aux}}{N_b}}{R_{\rm ZD}}. \tag{9}$$

Fortunately, $I_{\rm ZD}$ includes the line voltage information. That is, a high line voltage produces larger $I_{\rm ZD}$. Contrarily, a low line voltage produces smaller $I_{\rm ZD}$. The THDI technique mirrors $I_{\rm ZD}$ to modulate the on-time value of the power nMOSFET under four different input line RMS voltages. As the LVR detects the level of the input line RMS voltage, only one switch among M_3–M_{16} will be turned on, and the selected current $I_{\rm opt}$ will charge the $V_{\rm saw}$ to adjust the on-time value. Therefore, the slope of $V_{\rm saw}$ is proportional to the line voltage, owing to the dependence of $I_{\rm opt}$ on the line voltage.

As shown in Fig. 12(a), serious crossover distortion with large flat portion happens in conventional PFC with constant on-time control. Since the power delivered to output in one ac line cycle is fixed with constant load condition, the output power can be manipulated within an ac line cycle. In other words, if the on-time at high $V_{\rm in}$ decreases, the on-time near zero-crossings must be increased to provide enough power. Therefore, the current near zero-crossings can break through $I_{\rm limit}$ and shorten the flat portion of the line current, as shown in Fig. 12(b).

The adjusted $V_{\rm saw}$ is controlled by two components. The first component is $I_{\rm saw}$ in Fig. 7, which is used to generate the $V_{\rm saw}$ with the charging slope of $S_{\rm saw}$ in conventional PFC originally. $I_{\rm opt}$, which alters the charging slope by $S_{\rm opt}$ for on-time modulation, forms the second component. Since $V_{\rm saw}$ is limited in the range of $V_{\rm saw,dc}$ and $V_{\rm EAO}$, as shown in

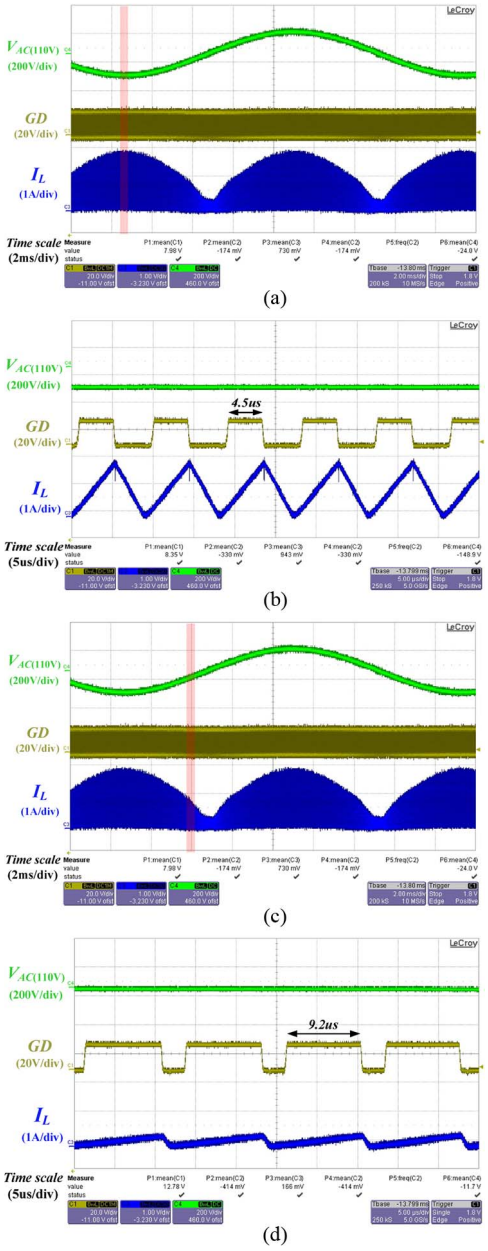

Fig. 19. (a) Measured waveforms of the gate signal and the inductor current at the high level of the line voltage. (b) Zoom in on the red region of (a). (c) Measured waveforms of the gate signal and the inductor current at the low level of the line voltage. (d) Zoom in on the red region of (c).

Fig. 12(b), the on-time value of the power nMOSFET after modulation is derived in

$$t_{\text{on,proposed}} = \frac{V_{\text{EAO}} - V_{\text{saw,dc}}}{S_{\text{saw}} + S_{\text{opt}}} = (V_{\text{EAO}} - V_{\text{saw,dc}}) \times \left(S_{\text{saw}} + \frac{\left(V_{\text{ZD,clamp}} + \frac{V_{\text{IN}} \cdot N_{\text{aux}}}{N_b} \right) \times M_i}{R_{\text{ZD}} \times C_{\text{saw}}} \right)^{-1} \quad (10)$$

where V_{EAO} is the output voltage of the error amplifier. $V_{\text{saw,dc}}$ is the designed lower bound of the sawtooth signal. S_{saw} and S_{opt} are the charging slopes of I_{saw} and I_{opt}, respectively, to charge C_{saw}. M_i is the optimal mirror ratio for THD minimization.

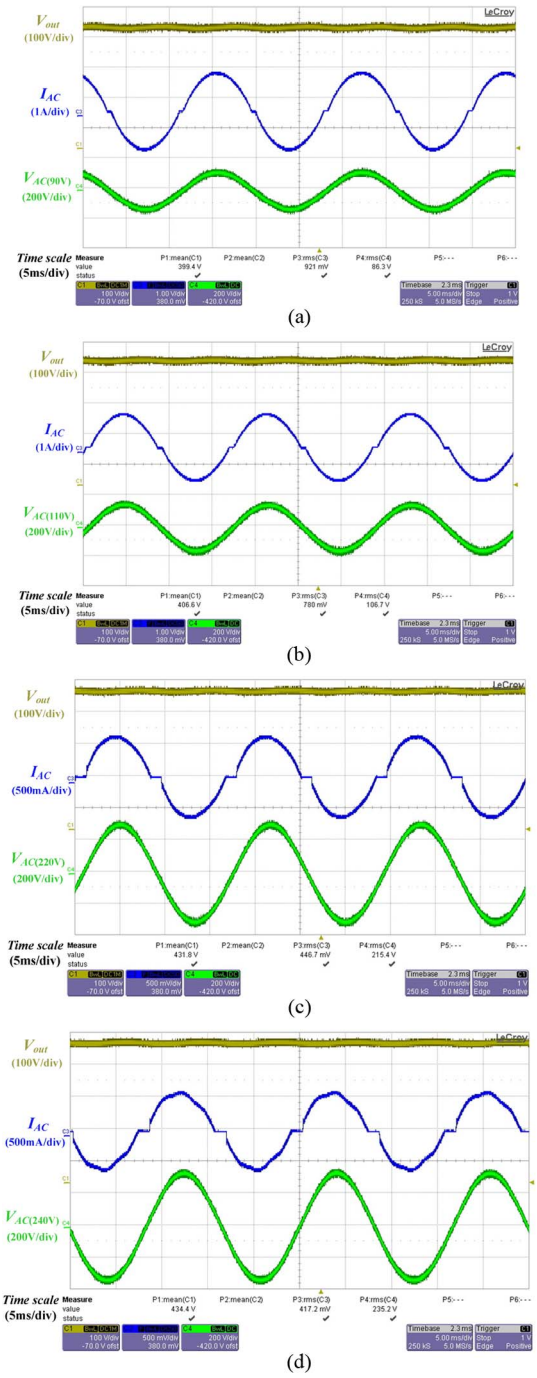

Fig. 20. Measured waveforms of the output voltage and the line current at the input line RMS voltages of (a) 90 V, (b) 110 V, (c) 220 V, and (d) 240 V.

It is worth to be mentioned that there exists a distinct optimal mirror ratio, i.e., M_i, at different line RMS voltages. That is, the ratio of M_5, M_6, M_7, and M_8 to M_1 are M_{90}, M_{110}, M_{220}, and M_{264}, respectively. To obtain the optimal mirror ratio, the relationship between the THD and the mirror ratio at different line RMS voltages is illustrated in Fig. 13. Therefore, the M_{90}, M_{110}, M_{220}, and M_{264} ratio is designed for the optimal on-time modulation value to obtain the minimum THD at different line voltages.

The output ripple with twice the ac line frequency is fed into the feedback loop, as shown in Fig. 14. The frequency of averaged diode current $I_{\text{diode,ave}}$, which is twice the ac line

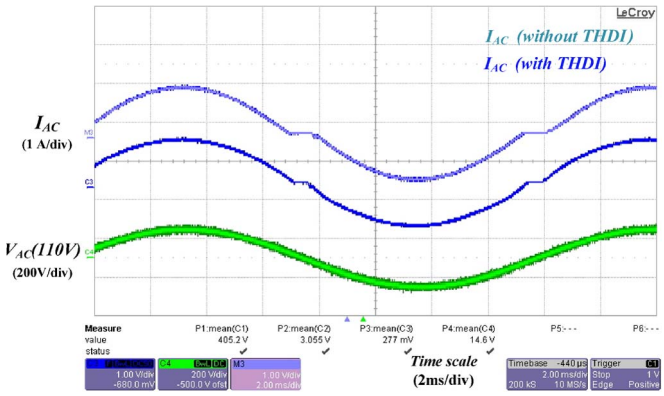

Fig. 21. Measured line voltage and line current waveforms at $V_{\rm AC}$ of 110 V with and without the proposed THDI.

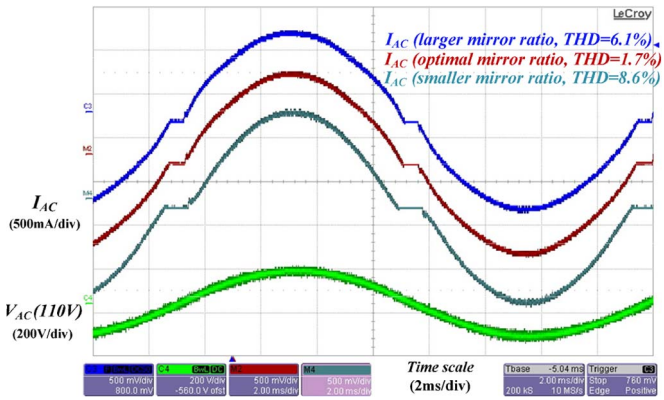

Fig. 22. Measured line voltage and line current waveforms with different mirror ratios.

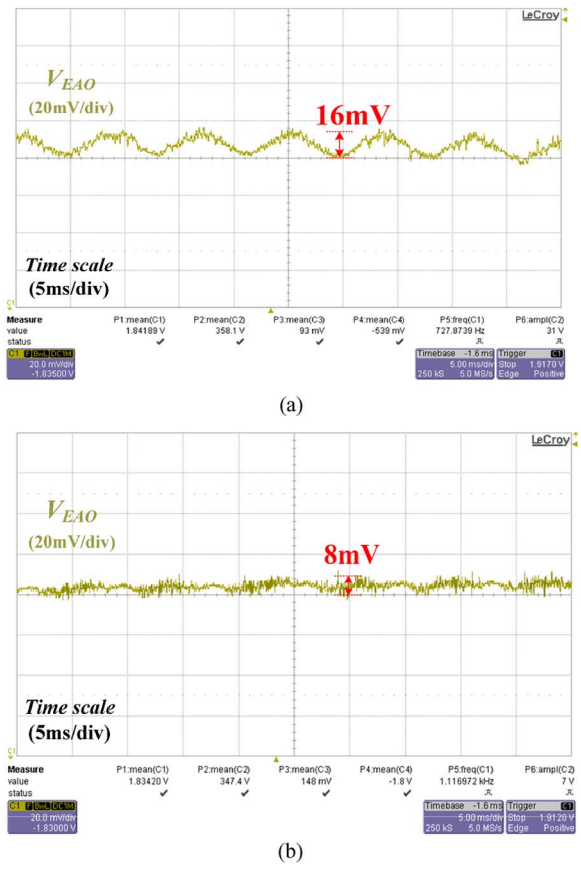

Fig. 23. Measured error amplifier output ripple (a) without the ripple compensator in the THDI and (b) with the ripple compensator in the THDI.

frequency, is derived in (11), shown at the bottom of the page, where $I_{\rm diode}$ is the diode current of the power stage, and $I_{\rm out}$ is a constant loading current. When $I_{\rm diode,ave}$ is larger than $I_{\rm out}$, $C_{\rm out}$ is charged. When $I_{\rm diode,ave}$ is smaller than $I_{\rm out}$, $C_{\rm out}$ is discharged. Thus, the voltage ripple frequency of $V_{\rm out}$ is also twice the ac line frequency, and the ripple at $V_{\rm out}$ is derived as (12). As long as the ripple, which is fed into the feedback loop, can be reduced, the line frequency reflected distortion can be improved as

$$\Delta V_{\rm out} = \frac{\int_{\frac{1}{8f_{\rm line}}}^{\frac{3}{8f_{\rm line}}} (I_{\rm diode,ave} - I_{\rm out})dt}{C_{\rm out}} = \frac{I_{\rm out}}{2\pi \cdot f_{\rm line} \cdot C_{\rm out}}. \quad (12)$$

The ripple compensator is used to further alleviate the line frequency reflected distortion. The idea of the ripple compensator is to inject a sinusoidal-like and out-of-phase current I_{sp} with respect to the current ripple flowing through the feedback resistor $R_{\rm fb1}$, i.e., $\Delta I_{\rm Rfb1}$. As a result, the output ripple of the error amplifier, i.e., $V_{\rm EAO}$, can be reduced such that the on-time variation is decreased to improve the THD, as shown in Fig. 15.

Since a sinusoidal-like current is needed, the voltage V_S from the LVR has to be processed by the envelope detector, which is composed of COM2, M_{17}, R_e, and C_e. By $C_{\rm rc}$, the out-of-phase current I_{sp} is generated and injected into $V_{\rm fb}$. Since $V_{\rm fb}$ decides the regulated voltage at the output, any dc value of I_{sp} deteriorates the regulation performance. Fortunately, $C_{\rm rc}$ blocks the dc components of I_{sp}. Therefore, the output voltage is not affected by the ripple compensator.

To conquer the line frequency reflected distortion, the design of $C_{\rm rc}$ is crucial. Since the goal of the ripple compensator is to eliminate the ripple of $V_{\rm FB}$, $V_{\rm FB}$ can be viewed as ac ground.

$$I_{\rm diode,ave} = \frac{\left[\sqrt{2} \cdot V_{\rm AC,rms} \cdot \sin(2\pi f_{\rm line} t)\right] \times \left[\sqrt{2} \cdot I_{\rm AC,rms} \cdot \sin(2\pi f_{\rm line} t)\right] \times \eta}{V_{\rm out}} = \frac{V_{\rm AC,rms} \times I_{\rm AC,rms}}{V_{\rm out}} \times (1 - \cos(4\pi f_{\rm line} t)) \times \eta = I_{\rm out} \cdot (1 - \cos(4\pi f_{\rm line} t)) \quad (11)$$

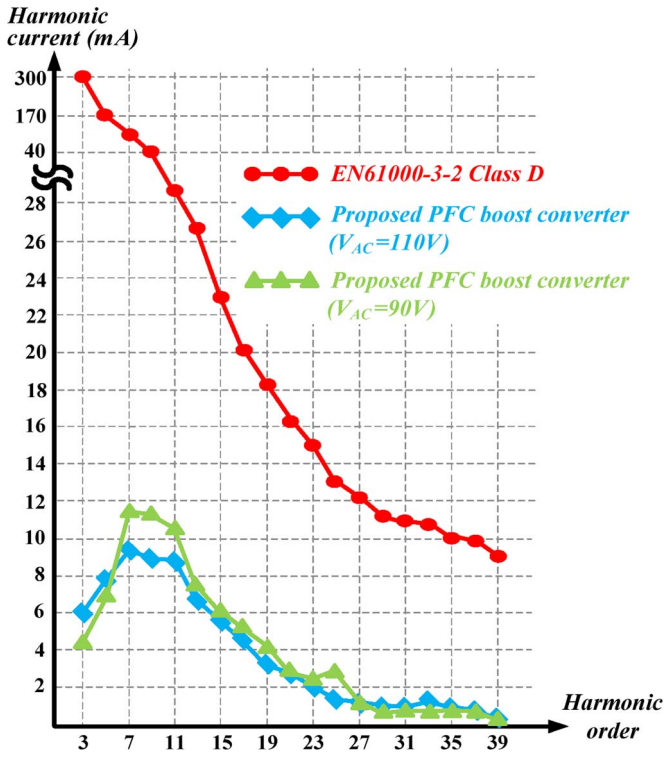

Fig. 24. Measured harmonic current and EN61000-3-2 class D regulation at the output power of 90 W.

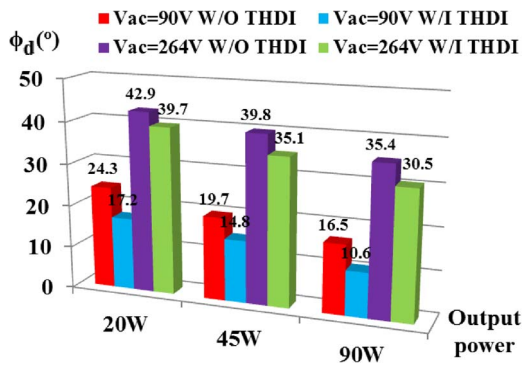

Fig. 25. Measured crossover distortion angle at different output power and line voltage conditions with and without the proposed THDI.

Thus, the current that flows from $V_{\rm out}$ to $V_{\rm FB}$, $\Delta I_{\rm Rfb1}$, and compensation current I_{sp} are cancelled at $V_{\rm FB}$, as shown in

$$\Delta I_{\rm Rfb1} + I_{sp} = 0. \tag{13}$$

Since $\Delta I_{\rm Rfb1}$ and I_{sp} are out of phase, (14) can be derived from (13) as

$$\frac{\Delta V_{\rm out}}{R_{\rm fb1}} - \frac{\Delta V_{sp}}{1/sC_{\rm rc,opt}} = 0 \tag{14}$$

where $\Delta V_{\rm out}$ is the ripple of the output voltage. ΔV_{sp} is the peak-to-valley amplitude of V_{sp}. Consequently, the optimal value of $C_{\rm rc}$ can be derived in

$$C_{\rm rc,opt} = \frac{\Delta V_{\rm out}}{2\pi f_{\rm line} \cdot \Delta V_{sp} \cdot R_{\rm fb1}} \tag{15}$$

where $f_{\rm line}$ is the line frequency.

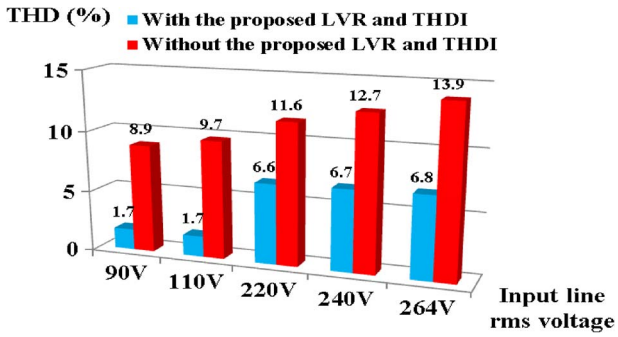

Fig. 26. Comparison diagram of the THD at the output power of 90 W with different input line RMS voltages.

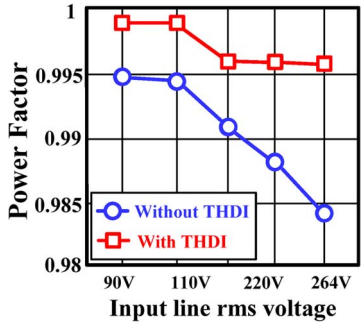

Fig. 27. Comparison diagram of the PF at the output power of 90 W with different input line RMS voltages.

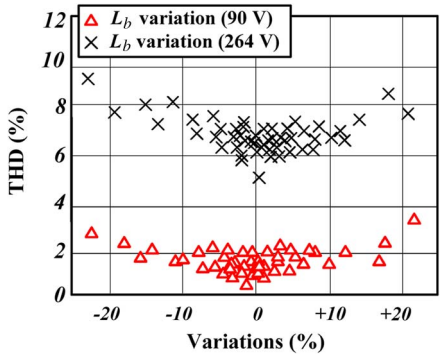

Fig. 28. Monte Carlo analysis of THD with inductance L_b variation at $V_{\rm rms}$ = 90 V and $V_{\rm rms}$ = 264 V.

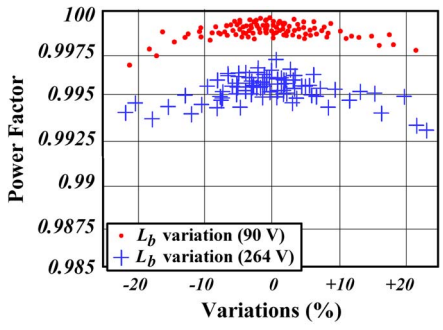

Fig. 29. Monte Carlo analysis of PF with inductance L_b variation at $V_{\rm rms}$ = 90 V and $V_{\rm rms}$ = 264 V.

IV. Simulation and Experimental Results

The proposed PFC controller with the LVR and the THDI was fabricated in a TSMC 0.5-μm 800-V ultrahigh-voltage (UHV) process. The chip micrograph is shown Fig. 16, and the

TABLE II
COMPARISONS BETWEEN PROPOSED METHOD AND PRIOR ARTS

	This work	[7]	[11]	[12]	[13]
Input line voltage	90~264V	90~264V	85~265V	115V	85~265V
Output voltage	400V	400V	392.5V	N/A	395V
Output power	90W	90W	300W	50W	80W
Circuit integrated	Fully integrated	Fully integrated	System level	System level	Fully integrated
Control methodology	Analog	Analog	Digital	Digital	Analog
Efficiency (maximum)	94.8%	95%	99.17%	94.7%	97%
THD (minimum)	1.7%	8%	3.59%	5%	3.6%
Power factor	0.998	0.99	0.985	0.996	0.998

specifications are listed in Table I. Fig. 17 shows the current sensing signal $V_{\rm CS}$ and the reconstructed line voltage V_S with different RMS line voltages. It is proved that the sinusoidal-wave tendency of the line voltage can be reconstructed by LVR without any extra pins. The waveforms of the ZCD circuit are shown in Fig. 18. Although the voltage of node ZCD varies in a wide range, the highest voltage of the ZD pin, which is connected to the integrated circuit, is clamped to about 20 V, determined by the breakdown voltage of the ZD in the ZCD circuit. In addition, the lowest voltage of the ZD pin is clamped to a quite low voltage higher than 0 V by the negative feedback in the ZCD circuit.

Fig. 19 shows the measured on-time, which is modulated by the THDI at the high and low levels of the line voltage. When the line voltage is at a high level, the on-time is about 4.5 μs. When the line voltage is at a low level near zero-crossings, the on-time is longer about 9.2 μs. Therefore, the crossover distortion can be effectively improved by on-time modulation according to the line voltage.

At the output power of 90 W, the measured waveforms of the output voltage and the line current at different line RMS voltages are shown in Fig. 20. The output voltage is regulated at 400 V. To provide power to equipment for general purpose, the 400 V is applied to the next dc–dc converter stage such as quasi-resonant and primary side regulator to step down the dc voltage. The line current is a sinusoidal wave, which is in phase with the line voltage by the proposed LVR and THDI techniques. Thus, the PF at different line voltages is higher than 0.99.

Fig. 21 shows the measured line voltage and line current waveforms with and without the proposed THDI. Fig. 22 shows the measured line voltage and current waveforms with different mirror ratios in the THDI at the output power of 90 W. Compared with the optimal mirror ratio, a larger or a smaller mirror ratio results in poor THD performance. In Fig. 23, the proposed ripple compensator effectively suppresses the output ripple of the error amplifier by 50%, which is decreased from 16 to 8 mV. In other words, the capacitance of C_C can be reduced by 50% by the feedforward path formed in the ripple compensator. Converting to the decrement of the chip area, the capacitor C_C occupies 0.98 and 0.49 mm^2 without and with the ripple compensator, respectively. However, the ripple compensator occupies only 0.06 mm^2. Consequently, the chip area of 0.43 mm^2 can be saved to lower the cost of the PFC.

The measured harmonic currents with the output power of 90 W at the input line RMS voltages of 90 and 110 V are shown in Fig. 24. It can be seen that the EN61000-3-2 class D regulation is met with enough design margin. Fig. 25 shows the measured crossover distortion angle at different output power and line voltage conditions. Without THDI, a crossover distortion angle of 42.9° happens at the output power of 20 W and $V_{\rm ac}$ of 264 V. The crossover distortion angles at all conditions are suppressed by modulating the on-time in THDI. Fig. 26 shows that the measured THD can be reduced to 1.7% at the line RMS voltage of 90–110 V and kept within 7% at the line RMS voltage of 90–264 V with the help of the proposed LVR and THDI. Fig. 27 shows that the measured PF is higher than 0.995 at different line RMS voltages with the output power of 90 W. Considering the devices mismatch of the proposed PFC controller, the THD and PF performance is mainly affected by the inductance variation. In Figs. 28 and 29, the Monte Carlo analyses of THD and PF with inductance L_b variation at $V_{\rm rms} = 90$ V and $V_{\rm rms} = 264$ V are shown, respectively. Even though the THD and PF performance is slightly affected by the inductance variation, Monte Carlo analyses show that the tolerance of the inductance variation can be as high as 20% with the proposed THDI. The comparisons between the proposed method and prior arts are listed in Table II.

V. CONCLUSION

The proposed LVR can detect the input line RMS voltage to generate the digital equivalent code to the THDI for optimizing the THD by tuning the on-time value at different line voltages. In addition, the LVR and the THDI provide a feedforward path to reduce the ripple of the feedback voltage for decreasing the THD. Experimental results show that the THD can be reduced to 1.7% at the line voltage of 90–110 V and that the PF is higher than 0.995 at different line voltages. Furthermore, the THD can be kept within 7% at universal line voltages. The test circuit was fabricated in a TSMC 800-V UHV process.

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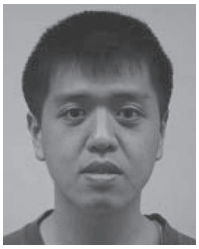

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