Low-Voltage Steep Turn-On pMOSFET Using Ferroelectric High-κ Gate Dielectric

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***Abstract*— Power consumption is the most difficult challenge for CMOS integrated circuits. Here, we demonstrate experimentally a novel steep turn-on pMOSFET for low-voltage operation for the first time, which exhibits 5–60 mV/decade SS, wide voltage range for SS < 60 mV/decade, sturdy <60 mV/decade SS at 85 °C, faster transistor turn-on at above threshold voltage, and lower off-state leakage by greater than three orders of magnitude. Such improved leakage current is crucial to decrease the OFF-state leakage current in sub-1X nm CMOS. This was achieved using ferroelectric high-κ ZrHfO gate dielectric pMOSFET.**

***Index Terms*— Ferroelectric, ZrHfO, transistor, sub-threshold swing.**

I. Introduction

POWER consumption is the most important criterion for integrated circuit (IC) using multi-Gb electronic devices [1]. To reach the low power target, both DC leakage power and AC switching power ($C_S V_D^2 f/2$) need to be decreased [2], [3]; here C_S, V_D, and f are the switching capacitance, drain voltage of a MOSFET, and operation frequency, respectively. Therefore, the MOSFET must be operated at a small V_D to lower the AC switching power. Nevertheless, the ultimate V_D reduction is limited by the fundamental transistor physics of slow turn-on sub-threshold slope (SS) of 60 mV/decade at room temperature [4]–[7]. The DC leakage power in a MOSFET originates from the off-state leakage current [3], [8], which becomes worse as the device downscales to sub-10 nm via quantum-mechanical tunneling. Thus, a novel steep turn-on MOSFET device with low off-state leakage needs to be invented.

In this letter, we present a novel steep turn-on MOSFET. Average SS < 60 mV/decade at 85 °C and improved off-state leakage by three orders of magnitude were measured, which are necessary for ultra-low power operation. This novel ultra-low power green transistor was achieved by applying a ferroelectric effect [9]–[12] to a high-κ gate dielectric, which has the extra merit of full fabrication compatibility with sub-32 nm IC process that uses high-κ MOSFETs [13]–[16].

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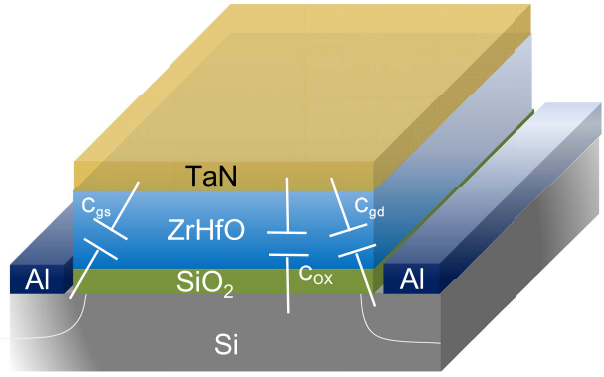

Fig. 1. Schematic structure of low SS ZrHfO pMOSFET device.

II. Experiments

The simple, self-aligned, gate-first TaN/ZrHfO/SiO_2 p-MOSFETs were fabricated on standard n-type Si substrates. First, a thin interfacial SiO_2 was grown on n-type Si substrate, followed by the ~30-nm high-κ ZrHfO deposition. A post-deposition annealing at 400 °C in oxygen ambient was applied to improve the gate dielectric quality. A 150-nm TaN metal was then deposited and patterned to form the gate electrode. Self-aligned B^+ ions were then implanted into the source–drain region and activated through rapid thermal annealing (RTA) at 950 °C. After etching the ZrHfO/SiO_2 on the source-drain contact region, the Al metal was deposited, patterned, and sintered to form the p-MOSFETs with a gate dimension of 10-μm × 100-μm.

III. Results and Discussion

Fig. 1 shows the schematic plot of gate-first TaN/ZrHfO/SiO_2 p-MOSFETs used in this letter. The ZrHfO dielectric was examined by energy-dispersive X-ray spectroscopy (EDX) that gives a Zr/Hf cation ratio of ~35/65. The Curie temperature of mixed ZrO_2-HfO_2 dielectric is at least up to 400K [11].

Fig. 2(a) shows the measured capacitance-voltage ($C - V$) characteristics of the high-κ ZrHfO p-MOSFET, in which a ferroelectric hysteresis loop was discovered at a higher voltage sweep. The extracted κ value from measured capacitance density of crystallized ZrHfO dielectric is ~30, which is favorable for both equivalent-oxide-thickness (EOT) scaling and low drive voltage operation.

Nevertheless, the large hysteresis loop causes flat-band voltage changes that in turn alter the transistor's threshold

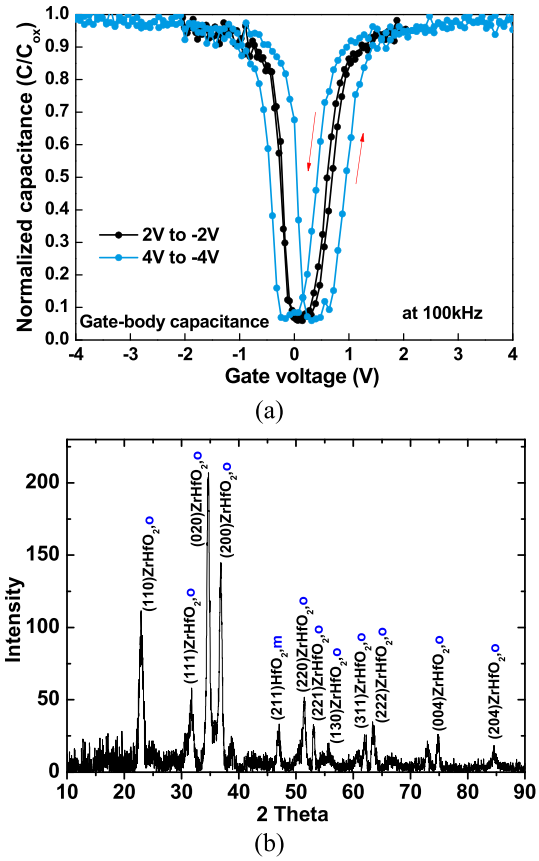

Fig. 2. (a) Measured $C-V$ characteristics and (b) GI-XRD diffractograms of high-κ ZrHfO p-MOSFET.

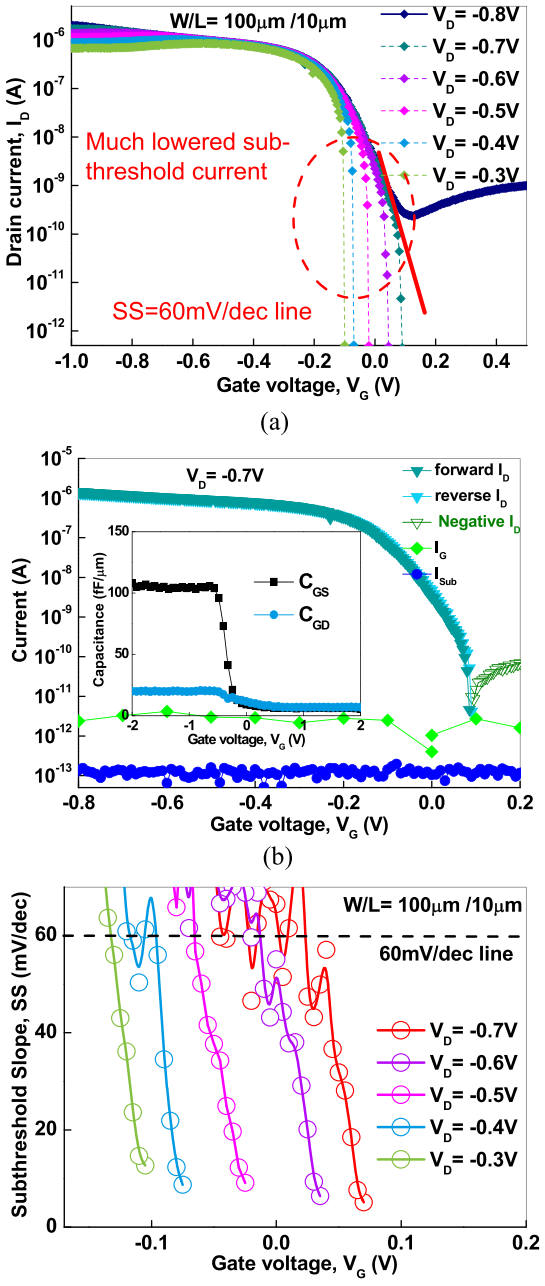

Fig. 3. (a) I_D-V_G characteristics (b) I_D-V_G, I_G-V_G and $I_{SUB}-V_G$ characteristics and (c) corresponding SS as a function of V_G of ferroelectric ZrHfO p-MOSFETs. The insert figure shows the C_{GS} and C_{GD} characteristics versus V_G. The I_S is nearly the same with I_D because of the small I_G, low I_{Sub}, and Kirchhoff's Current Law. Besides, a negative I_D was also measured at $V_G > 0.1$ V.

voltage (V_T) and hinder the low V_D operation. Fortunately, the ferroelectric hysteresis loop decreases monotonically as the sweep voltage decreases to a small 0.07 V at -2 to $+2$ V sweep. The ferroelectricity is related to the measured crystalline structure of ZrHfO gate dielectric [11] by using the grazing incidence x-ray diffraction diffractogram (GI-XRD), shown in Fig. 2(b). The ZrHfO gate dielectric has a small nano-crystalline size, which allows incorporation into a highly scaled MOSFET at sub-10 nm. It is crucial to notice that the previous ferroelectric MOSFET was used for one-transistor memory application with thicker non-Hf-based high-κ gate dielectrics [9], [10] that are quite different from the current application.

The transistor characteristics were further evaluated. The measured I_D-V_G characteristics of a ferroelectric high-κ ZrHfO p-MOSFET are shown in Fig. 3(a). Steep turn-on $SS < 60$ mV/decade is measured at V_D up to -0.7 V. Here, neither apparent hysteresis loop nor V_T changes can be found at such low voltage operation. Such steep turn-on behavior is difficult to reach in tunnel FET, because of the heavier holes effective mass than that of electrons.

Furthermore, the off-state leakage current is reduced by >3 orders of magnitude because of the steeper SS, from $\sim 10^{-9}$ A at $V_D = -0.8$ V with $SS > 60$ mV/decade to $<10^{-12}$ A at $V_D = -0.7$ V with $SS < 60$ mV/decade. Such greatly improved off-state leakage is crucial for MOSFET scaling into a sub-10 nm regime, where the leakage current is the major DC power limitation for a high-density IC. Therefore, the measured steep SS MOSFET not only diminishes the AC switching power but also simultaneously decreases the DC leakage power, although the detailed mechanism for DC leakage current reduction is still under investigation.

In Fig. 3(b), very low gate and substrate leakage currents (I_G and I_{SUB}) were measured due to the relatively thick high-κ dielectric. A small ferroelectric I_D-V_G hysteresis of 5 mV was measured under forward and reverse sweep

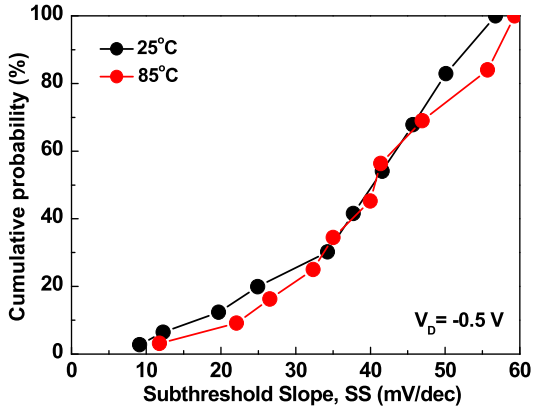

Fig. 4. Temperature dependence on *SS* distribution of the ferroelectric ZrHfO p-MOSFETs.

with nearly the same *SS*. The source-gate and drain-gate capacitances (C_{GS} and C_{GD}) in the inset figure are similar to conventional MOSFET that allows unilateral gain with small feedback. Although we achieved superior *SS* to previous publication [17], no negative capacitance [17] was measured in this letter. Thus, the $SS < 60$ mV/decade *SS* property is attributed to the ferroelectric polarization effect of ZrHfO dielectric. Fig. 3(c) plots the *SS* as a function of V_G. A steep *SS* of 5 to 60 mV/decade is measured at V_D from -0.7 to -0.3 V. It is important to notice that such low *SS* is valuable for lower AC power operation due to its V_D^2 dependence. The improved *SS* with decreasing $|V_G - V_T|$ is also beneficial for lower power operation.

Another critical aspect of this steep turn-on MOSFET is its high temperature characteristics, because ICs typically operate at an elevated temperature. Fig. 4 displays the sub-60-mV/decade *SS* distribution at both 25 °C and 85 °C, with $V_D = -0.5$ V. The cumulative probability was defined as the probability that the value of a random variable happens within a specific range. This was used to predict the occurrence probability of $SS < 60$ mV/decade at different temperatures. The excellent sub-60 mV/dec property at 85 °C is measured, although the *SS* data are slightly inferior to those at 25 °C. The *SS* data at 85 °C are the best reported [6]–[7], which are critical for low-power IC operation at the elevated temperatures.

IV. Conclusion

In summary, a steep sub-60-mV/decade turn-on property at 85 °C and an extremely low off-state leakage current were achieved simultaneously. These excellent device performances were achieved using a ferroelectric high-κ ZrHfO gate dielectric in a p-MOSFET that has full compatibility with existing high-κ MOSFET process used in the current ICs. For the first time, the p-MOSFET possesses steep turn-on characteristics that are much more difficult than an n-MOSFET.

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