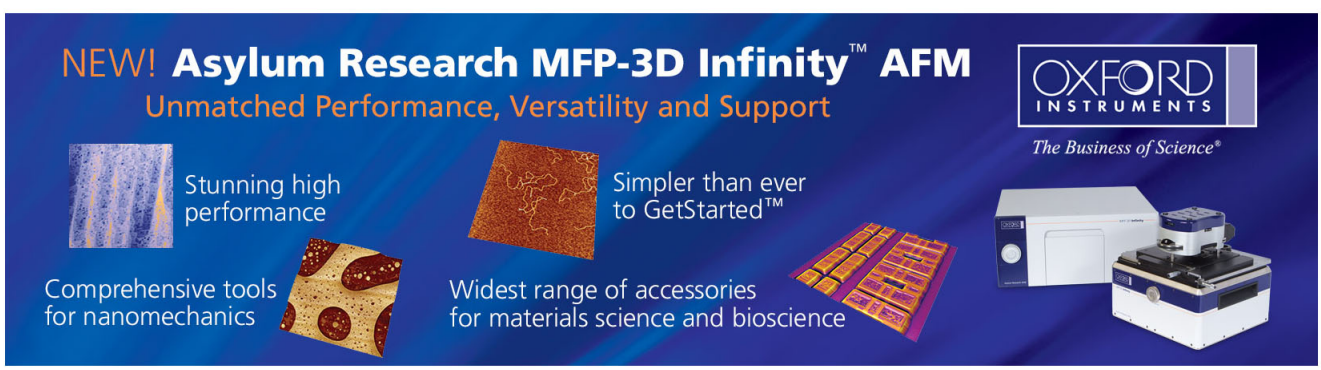
AIP | Applied Physics Letters

Fermi-level shifts in graphene transistors with dual-cut channels scraped by atomic force microscope tips

Meng-Yu Lin, Yen-Hao Chen, Chen-Fung Su, Shu-Wei Chang, Si-Chen Lee, and Shih-Yen Lin

Citation: Applied Physics Letters **104**, 023511 (2014); doi: 10.1063/1.4862275
View online: http://dx.doi.org/10.1063/1.4862275
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/104/2?ver=pdfcov
Published by the AIP Publishing



Fermi-level shifts in graphene transistors with dual-cut channels scraped by atomic force microscope tips

Meng-Yu Lin,[1,2] Yen-Hao Chen,[3] Chen-Fung Su,[4] Shu-Wei Chang,[2,3] Si-Chen Lee,[1] and Shih-Yen Lin[1,2,3,a)]
[1]*Institute of Electronics, National Taiwan University, Taipei 10617, Taiwan*
[2]*Research Center for Applied Sciences, Academia Sinica, Taipei 11529, Taiwan*
[3]*Department of Photonics, National Chiao Tung University, Hsinchu 30010, Taiwan*
[4]*College of Photonics, National Chiao Tung University, Tainan 71150, Taiwan*

(Received 20 November 2013; accepted 30 December 2013; published online 16 January 2014)

We investigate the electronic properties of p-type graphene transistors on silicon dioxide with dual-cut channels that were scraped using atomic force microscope tips. In these devices, the current is forced to squeeze into the path between the two cuts rather than flow directly through the graphene sheet. We observe that the gate voltages with minimum current shift toward zero bias as the sizes of the dual-cut regions increase. These phenomena suggest that the Fermi levels in the dual-cut regions are shifted toward the Dirac points after the mechanical scraping process. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4862275]

Following the massive efforts that have been devoted to the investigation of the unique two-dimensional crystal graphene, practical applications of this material have been gradually directed towards transparent electrodes and high-speed electronics.[1–3] The foundation for these proposed applications is the high carrier mobility that has been theoretically predicted in this material.[4] To demonstrate these functionalities in practice, the first issue is the availability of large-area and uniform graphene films to be used for device fabrication. The most common fabrication approaches used are silicon (Si) sublimation from silicon-carbide (SiC) substrates and graphene growth by either chemical vapor deposition (CVD) or molecular beam epitaxy (MBE).[5–7] Touch-panel display screens and gallium-nitride light-emitting diodes that used large-area graphene films prepared by CVD for their transparent electrodes have been demonstrated.[2,8] For high-speed electronics, terahertz (THz) logic circuits have been implemented that use graphene films prepared on SiC substrates for the transistor channels.[3] At this stage, it seems that the practical use of graphene has become feasible. However, in high-speed electronics applications, while the THz circuits themselves have been realized, the difficulty of integrating these circuits with current Si device fabrication lines and the high cost of SiC substrates would be two major disadvantages of this approach. Replacement of the CVD-prepared graphene films with films that were grown on the SiC substrates may offer a solution to this problem.

In previous publications, a structure that was commonly adopted to demonstrate the ambipolar characteristics of graphene and measure its carrier mobility is that of thin-film transistors on silicon dioxide (SiO_2).[6,9–14] However, in contrast to the high mobility observed in free-standing graphene sheets, low values are usually observed in transistors that were fabricated with CVD-grown graphene films.[9] Experiments have also shown that the type and concentration of the carriers in the graphene channels depend critically on the nature of the graphene/SiO_2 interfaces and the adsorbed atoms.[10,12,13] The graphene film morphology is also significantly affected by the underlying SiO_2 structure, and the conformity between the two materials is generally imperfect.[15] Theoretical calculations have indicated that the Fermi level may vary widely for the different bonding configurations of the graphene-SiO_2 interfaces.[16]

In this work, by scraping the p-type CVD-prepared graphene transistors on SiO_2 with atomic force microscope (AFM) tips, we fabricate dual-cut channels and investigate their electronic properties. The two isolating AFM cuts mean that the current is forced to flow through the dual-cut region that is sandwiched between them. We see that the minimum-current gate voltage, at which the Fermi level crosses the Dirac points, shifts from positive to near-zero bias as the size of the dual-cut region increases. These phenomena indicate that the dual-cut region may become intrinsic or less strongly p-type following the AFM cuts, so that a lower gate bias is required to shift the Fermi level to the Dirac points. We speculate that the scraping process has effects on the bonding configurations of the graphene-SiO_2 interfaces in the dual-cut regions.

The graphene film used in this paper was prepared by CVD. The graphene film fabrication procedure is as follows. (a) A 25 μm copper foil is placed in a quartz tube furnace for 30 min of annealing under a hydrogen (H_2) atmosphere at 1030 °C. The chamber pressure is maintained at 320 mTorr. (b) A gas mixture composed of methane and H_2 at flow rates of 7 sccm and 15 sccm, respectively, is added to the chamber for 10 min for graphene growth. During the growth process, the pressure is maintained at 650 mTorr. (c) The sample is moved out of the tube and standard graphene transfer procedures are used to reattach the graphene films to 600 nm SiO_2/Si substrates.[6] To investigate the device characteristics, bottom-gate thin film transistors are fabricated from the graphene. An optical microscopy image of a typical device is shown in Fig. 1. These devices are fabricated using standard photolithography techniques. Their channels are 10 μm wide,

a)Electronic mail: shihyen@gate.sinica.edu.tw

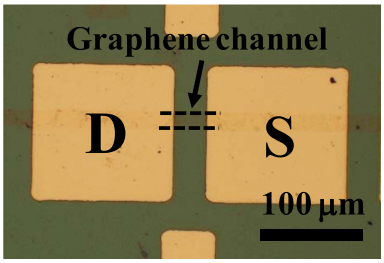
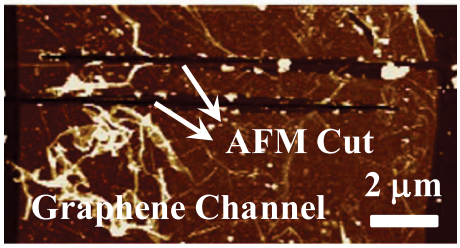


FIG. 1. Optical microscopy image of the bottom-gate graphene transistor.

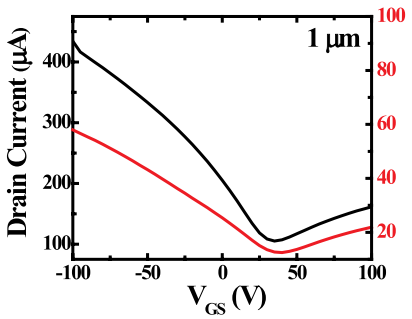
and 50/300 nm titanium/gold layers are deposited as electrodes (i.e., the drain/source terminal and the bottom gate).

To change the conduction paths of the graphene transistors, two cuts from the interior to the opposite edges of the graphene sheet are fabricated in parallel, with different spacings used near the channel midpoint. Openings of 1 μm are left for each cut. An image of the dual cuts with 1 μm separation is shown in Fig. 2(a) as an example. The cuts are formed by scraping the graphene channels with a diamond-coated tip installed on a Dimension Icon AFM system. Scraping the graphene surface with AFM tips has proved to be effective in providing electrical isolation between the graphene sheets on the two sides of the trench[17] and is therefore a simple approach for current redirection and confinement. In this way, the current is forced to flow through the graphene channel between the two cuts (the dual-cut region). Also, because of the presence of the two parallel AFM cuts, which effectively function as a capacitor, a major proportion of the drain-source voltage V_{DS} would fall on the dual-cut region, even though the gate bias V_{GS} also changes the graphene resistivity outside the cut area. This situation is analogous to that of a p-n diode operating below its turn-on voltage, where most of the external bias is applied to the junction (depletion) region rather than to the p- or n-type semiconductors. From this viewpoint, the measurements to be described mostly reflect the differences in electronic properties between the dual-cut region and an ordinary graphene sheet on SiO_2.

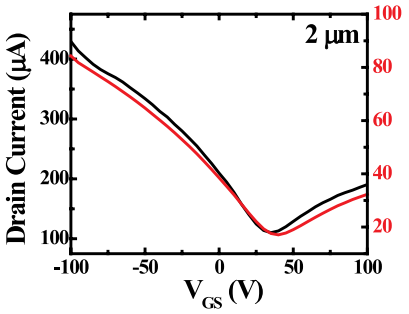
The I_D-V_{GS} curves of three devices with 1, 2, and 3 μm cut separations at $V_{DS} = 1$ V are shown in Figs. 2(b)–2(d), respectively. In Fig. 2(b), despite a ten-fold current reduction that was observed for the device after the AFM cuts, the gate voltage V_{GS} at the minimum drain current only changes slightly. This voltage corresponds to the energy difference between the Dirac point E_{Dirac} and the Fermi level E_F of the graphene, and the minor change in this case therefore implies that there is little difference in the values of E_{Dirac}–E_F in the dual-cut region before and after the AFM cuts. In contrast, the minimum-current gate voltage begins to shift towards the zero bias with increasing cut separation, as shown in Fig. 2(d). These results suggest that the effective energy difference $E_{Dirac} - E_F$ in the dual-cut region decreases if the cut separation increases. Although the hole concentration that is responsible for the conduction in the dual-cut region decreases under such circumstances, increasing the cut separation from 1 to 3 μm enlarges the conduction cross-section and reduces the current-crowding effect (redirection of the current flows at the two channel openings become less



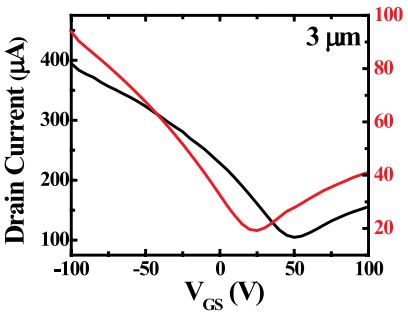
(a)



(b)



(c)



(d)

FIG. 2. (a) AFM image of the dual-cut transistor with 1 μm separation. The I_D-V_{GS} curves of the three devices are shown with (b) 1, (c) 2, and (d) 3 μm cut separations at $V_{DS} = 1$ V. The dark and red lines represent the I-V characteristics before and after the AFM scraping processes, respectively.

abrupt), so that the drain currents I_D at $V_{GS} = 0$ V are similar or only change slightly.

These experimental observations might be expected if the graphene-SiO_2 interface inside the dual-cut region was to become nearly intrinsic or less strongly p-type after the AFM scraping process. One possible scenario is that the external stress and the induced strain that resulted from the two scraping actions may easily propagate through the graphene/SiO_2 interface and become confined within the dual-cut region, which in turn changes the conformity and

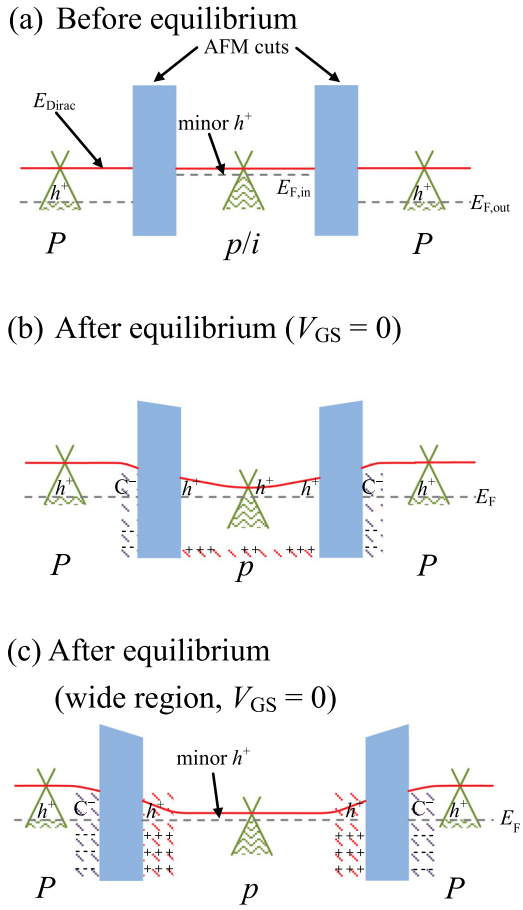


FIG. 3. (a) Schematic band diagram of the dual-cut region before equilibrium with the outside graphene is reached. (b) The band diagram near a narrow dual-cut region, and (c) the corresponding diagram for a wide dual-cut region.

the bonding structures in the region. On average, this effect weakens the coupling between the graphene and the underlying SiO_2 in the dual-cut region, and the Fermi level $E_{F,in}$ in the region may then become closer to the Dirac point before reaching equilibrium with the outside graphene, as shown in Fig. 3(a). Because the Fermi level $E_{F,in}$ is higher than the corresponding $E_{F,out}$ outside the dual-cut region, the holes (electrons) outside (inside) the dual-cut region tend to diffuse into the corresponding unoccupied area through the channel openings. This process lasts until potential barriers are formed across the AFM cuts to block this macroscopic carrier exchange. Meanwhile, the two Fermi levels merge into a single E_F, as shown in Fig. 3(b). If the dual-cut region is narrow, then the outside holes would nearly deplete the electrons in this area and pervade everywhere. In this case, the energy difference $E_{Dirac} - E_F$ has similar values inside and outside the dual-cut region, and the gate voltage at the minimum current does not change greatly. However, if the dual-cut region is sufficiently wide, the electron depletion by the outside holes may be incomplete before the electrostatic potentials across the AFM cuts are large enough to block the process. As shown in Fig. 3(c), under these circumstances, the interior of the dual-cut region can remain nearly intrinsic or slightly p-type, i.e., the difference between the Fermi level and the Dirac point is small, and we would observe a significant reduction in the gate voltage at the minimum current.

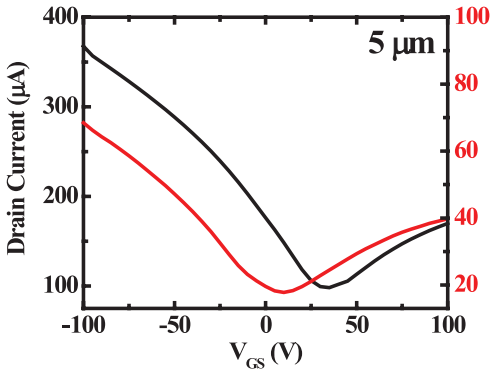


FIG. 4. The I_D-V_{GS} curves of the device with 5 μm cut separation at V_{DS} = 1 V. The dark and red curves represent the I-V characteristics before and after the AFM scraping process, respectively.

Based on our model, with the larger cut separation, the Fermi level in the dual-cut region should become closer to that of intrinsic graphene. Indeed, from the I_D-V_{GS} curves of the device with 5 μm cut separation that are shown in Fig. 4 (V_{DS} = 1 V), the measured minimum-current gate voltage is already close to the zero bias, even if the 600 nm SiO_2 layer actually lowers the true gate bias that is applied to the graphene considerably. These results have demonstrated that when using the dual-cut channel architecture, the difference between the Fermi level and the Dirac point can be tuned based on the sizes of the dual-cut regions.

Another interesting phenomenon is that all four dual-cut devices have similar minimum drain currents of about 20 μA. In theory, the carrier density should vanish when the Fermi level coincides with the Dirac point. In previous publications, the residual carrier density was attributed to charged impurities in the graphene channels.[18] If this concept were applicable in our case, the minimum drain currents of these dual-cut devices should be proportional to their respective cut separations, rather than being similar. One possible explanation for this inconsistency is that the minimum current is dominated by the edge leakage current, because the edge lengths are the same for these devices. Further investigations will be required in future work to confirm this explanation.

In conclusion, based on the dual-cut device architecture, the region between the two cuts, rather than the original sound graphene film, is converted into the conduction channel. As the dual-cut region defined by the AFM scraping becomes wider, then the minimum-current gate voltage of the device shifts closer to the zero bias condition. The results presented here have demonstrated an interesting architecture for device fabrication, Fermi level tuning, and device applications.

This work was supported in part by the National Science Council Projects Nos. NSC 102-2221-E-001-032-MY3 and NSC 102-2622-E-002-014, and the scraping processes were performed using the AFM system in the core facility of the Research Center for Applied Sciences (RCAS), Academia Sinica.

[1]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).

[2]G. Jo, M. Choe, S. Lee, W. Park, Y. H. Kahng, and T. Lee, Nanotechnology **23**, 112001 (2012).
[3]Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and Ph. Avouris, Science **327**, 662 (2010).
[4]J. Chen, J. Xi, D. Wang, and Z. Shuai, J. Phys. Chem. Lett. **4**, 1443 (2013).
[5]M. Y. Lin, W. C. Guo, M. H. Wu, P. Y. Wang, T. H. Liu, C. W. Pao, C. C. Chang, S. C. Lee, and S. Y. Lin, Appl. Phys. Lett. **101**, 221911 (2012).
[6]X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo and R. S. Ruoff, Science **324**, 1312 (2009).
[7]G. Lippert, J. Dabrowskil, M. C. Lemme, C. M. Marcus, O. Seifarth, and G. Lupina, Phys. Status Solidi B **248**, 2619 (2011).
[8]S. Bae, H. Kim, Y. Lee, X. Xu, J. S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y. J. Kim, K. S. Kim, B. özyilmaz, J. H. Ahn, B. H. Hong, and S. Iijima, Nat. Nanotechnol. **5**, 574 (2010).
[9]M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, IEEE Electron Device Lett. **28**, 282 (2007).
[10]H. E. Romero, N. Shen, P. Joshi, H. R. Gutierrez, S. A. Tadigadapa, J. O. Sofo, and P. C. Eklund, ACS Nano **2**, 2037 (2008).
[11]Y. J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim, Nano Lett. **9**, 3430 (2009).
[12]S. Ryu, L. Liu, S. Berciaud, Y. J. Yu, H. Liu, P. Kim, G. W. Flynn, and L. E. Brus, Nano Lett. **10**, 4944 (2010).
[13]Z. Cheng, Q. Zhou, C. Wang, Q. Li, C. Wang, and Y. Fang, Nano Lett. **11**, 767 (2011).
[14]S. M. Song, J. K. Park, O. J. Sul, and B. J. Cho, Nano Lett. **12**, 3887 (2012).
[15]M. Ishigami, J. H. Chen, W. G. Cullen, M. S. Fuhrer, and E. D. Williams, Nano Lett. **7**, 1643 (2007).
[16]X. F. Fan, W. T. Zheng, V. Chihaia, Z. X. Shen, and J. L. Kuo, J. Phys.: Condens. Matter **24**, 305004 (2012).
[17]L. Weng, L. Zhang, Y. P. Chen, and L. P. Rokhinson, Appl. Phys. Lett. **93**, 093107 (2008).
[18]K. Nagashio, T. Nishimura, and A. Toriumi, Appl. Phys. Lett. **102**, 173507 (2013).