Submicron T-Shaped Gate HEMT Fabrication Using Deep-UV Lithography

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Abstract— **A new combination of low/high/low sensitivity trilayer (PMMA/PMIPK/PMMA) resist system was used for deep UV lithography to fabricate submicron T-shaped gate. Gate length as narrow as 0.2 μm is achieved. The GaAs HEMT's with 0.3 μm T-shaped Ti/Pt/Au gate is fabricated using this technology. The HEMT demonstrated a 0.6 dB noise figure and 13 dB associated gain at 10 GHz. This deep UV lithography process provides a high throughput and low cost alternative to E-beam lithography for submicron T-gate fabrication.**

I. Introduction

In order to fabricate high performance receivers for satellites and other applications, GaAs FET's (field effect transistor) with very low noise figure are needed. To achieve high gain and low noise applications, T-shaped gate with short gate length and low gate resistance are required. In the T-gate structure, the upper wide layer increase the cross-section area of the gate, thus reducing the gate resistance, and the small foot print of the gate reduces the gate capacitance. Electron-beam lithography is the most widely used tool to fabricate the submicron T-gate because the resolution is better than 0.1 μm [1]–[6]. Chao *et al.* demonstrated an improved undercut profile by PMMA (poly methyl methacrylate)/PMMA-PMAA (poly methyl methacrylate-methacrylic acid)/PMMA (poly methyl methacrylate) trilayer system using E-beam lithography. However, the very low throughput and expensive equipment cost are the major disadvantages for the E-beam lithography process. In this paper, we present a new method of manufacturing submicron T-gate using deep UV lithography and PMMA (poly methyl methacrylate)/PMIPK (poly methyl isopropenyl ketone)/PMMA (poly methyl methacrylate) trilayer resists.

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II. Experimental Procedures

This new combination of trilayer resist structure is consisting of 0.3 μm PMMA for the bottom layer (30 cp, 1000 rpm), 0.9 μm PMIPK for the middle layer (170 cp, 5000 rpm), and 0.1 μm PMMA for the top layer (30 cp, 2000 rpm). Deep UV contact aligner with 250 nm light source is used for this study. The masks used are 4 inch masks with pattern size of 0.3 μm and 0.5 μm. All the pattern are exposed by one shot deep UV exposure. The gate metals Ti/Pt/Au are sequentially deposited by e-gun evaporator. Deposition rate is kept at 100 Å/s and the total thickness is about 6000 Å. The substrate temperature is limited below 100 °C during metal evaporation. The HEMT's (high electron mobility transistor) processed are AlGaAs/InGaAs based pseudomorphic HEMT. The epitaxy materials of the HEMT devices are grown by MBE (molecular-beam epitaxy). The device process includes: wet chemical etch for mesa isolation, electron-beam evaporated AuGeNi for ohmic contacts and Ti/Pt/Au for Schottky gate. The silicon nitride film is used for passivation. The T-shaped resist profiles are formed using the PMMA/PMIPK/PMMA trilayer resists technique using one shot deep-UV exposure ($\sim$1.5 J/cm^2).

III. Results and Discussion

We have designed the PMMA/PMIPK/PMMA trilayer combination with the low/high/low sensitivity resists to form the T-shaped cavity. The reason that PMMA/PMIPK/PMMA is chosen instead of PMMA/PMMA-PMAA/PMMA as used in E-beam lithography is because that PMIPK is more sensitive (about five times) to the deep-UV light source than PMMA-PMAA. For an ideal T-shape cavity, the ratio of the dimension of the top opening to the dimension of the bottom opening must keep high and the dimension of the bottom opening must be as small as possible. In the PMMA/PMIPK/PMMA system, the sensitivity of middle layer PMIPK is much higher than PMMA (about 30 times), therefore an improved undercut profile for T-shaped cavity is realized. High dissolution rate developer is selected for developing top layer, while the lower dissolution rate developer is used for developing bottom layer. These resist layers are developed layer by layer in various developers. First, top layer is developed in MIBK, after that the middle PMIPK layer is developed in its developer (MIBK based solution). Finally, the bottom layer is developed in MIBK and IPA mixture (1:3). The top opening determines the gate resistance, and the bottom opening defines the effective

Fig. 1. The PMMA/PMIPK/PMMA trilayer resist profile after developed.

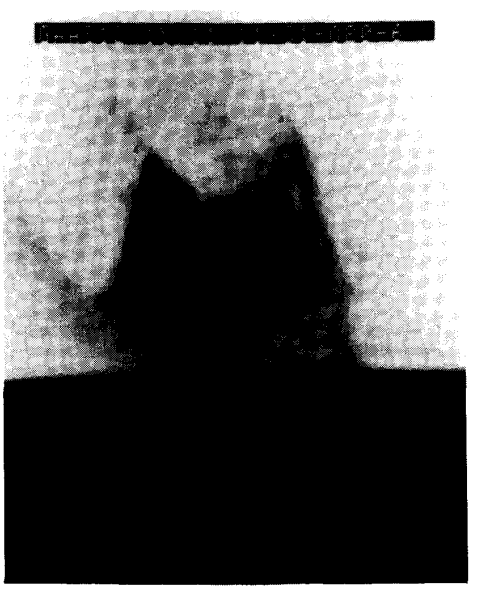
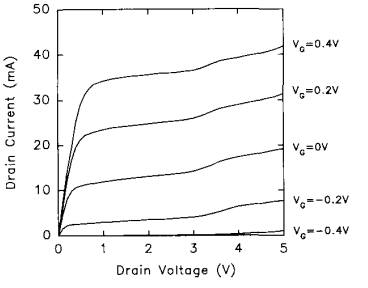
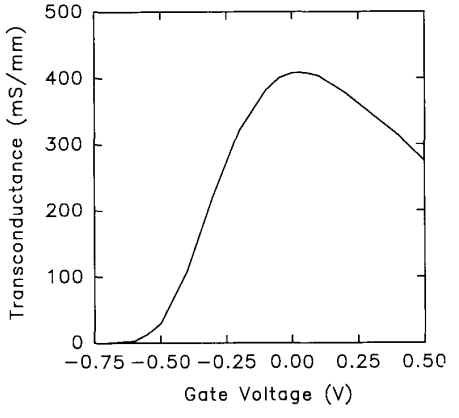


Fig. 2. The 0.2 μm foot-print T-shaped gate on GaAs formed by PMMA/PMIPK/PMMA trilayer resists.

gate length and can be adjusted through different combinations of developers. Because of faster dissolution rate in MIBK solution, the development time must be well-controlled. It is a critical step during the development process. Fig. 1 is the trilayer resist profile after developed in the forementioned solutions. The ratio of the top opening to bottom opening is more than 4 (the ratio of PMMA/PMMA-PMAA/PMMA is about 3). The thickness of the gate after lift-off is limited not only by the thickness of the resists but also by the upper layer resist opening during metal evaporation. Because of high ratio of top layer opening to bottom layer opening as shown in Fig. 1 and high resolution definition on bottom layer, nearly ideal 0.2 μm T-shaped gate (with 0.3 μm mask) on GaAs can be obtained as shown in Fig. 2. The 0.3 μm T-shaped gate GaAs HEMT's are processed using this PMMA/PMIPK/PMMA trilayer resists technology (with 0.5 μm mask). Fig. 3(a) and 3(b) show the electrical characteristics of one of these HEMT's. The maximum transconductance and cut-off frequency are 408 mS/mm and 23 GHz, respectively. The minimum noise figure is 0.6 dB at 10 GHz and the associated gain at this frequency is 13 dB. The transconductance deviation within twelve percent are obtained across the 3 inch wafers and the yield of the wafers is over 80% using this technique. Four 3 inch wafers are processed using the same mask and process and show the similar gate profile and electrical results.



(a)



(b)

Fig. 3. (a)/(b) The output characteristics of the HEMT devices with 0.3 μm gate length.

IV. Conclusion

A 0.2 μm foot print of the T-shaped gate is realized by using PMMA/PMIPK/PMMA trilayer resists and one shot deep-UV lithography. The GaAs HEMT's with 0.3 μm T-shaped Ti/Pt/Au gate are fabricated using this trilayer process. This HEMT's show well-controlled profile and excellent electrical properties (noise figure is 0.6 dB and associated gain is 13 dB at 10 GHz). The yield of these wafers is about 80%. Four 3 inch wafers are processed which showed similar electrical results and yield. This trilayer resists is more reproducible and controllable than PMMA/PMMA-PMAA/PMMA trilayer

resists using deep UV lithography. This process is simple and reproducible and provides a high throughput and low cost alternative to conventional E-beam lithography.

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