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Novel gate-all-around polycrystalline silicon nanowire memory device with HfAlO charge-trapping layer

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Gate-all-around (GAA) nanowire (NW) memory devices with a SiN- or Hf-based charge-trapping (CT) layer of the same thickness were studied in this work. The GAA NW devices were fabricated with planar thin-film transistors (TFTs) on the same substrate using a novel scheme without resorting to the use of advanced lithographic tools. Owing to their higher dielectric constant, the GAA NW devices with a HfO_2 or HfAlO CT layer show greatly enhanced programming/erasing (P/E) efficiency as compared with those with a SiN CT layer. Furthermore, the incorporation of Al into the Hf-based dielectric increases the thermal stability of the CT layer, improving retention and endurance characteristics.
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1. Introduction

Recently, polycrystalline silicon (poly-Si)-based devices have received much attention for the integration of nonvolatile memory cells in ultrahigh-density arrays.[1–3] Moreover, the low-temperature fabrication and high flexibility of poly-Si field-effect transistors (FETs) make such FETs feasible for integration with other circuit components, such as drivers, converters, processors, and memories, on the same chip or panel.[4–6] Among a number of flash memories, the gate-all-around (GAA) nanowire (NW) charge-trapping (CT)-type memory is considered to be one of the most promising structures for future NAND flash technologies.[7,8] Due to its enhanced gate controllability, the GAA NW device shows excellent electrical characteristics, such as a steep sub-threshold swing (~200 mV/dec or smaller), a high ON/OFF current ratio ($>10^7$), and a high immunity against short-channel effects.[9,10] Furthermore, owing to the tiny NW channel, a small numbers of discrete trapped charges in the trapping layer can result in a large sensing window. The NW memory devices also show a lower programming/erasing (P/E) operation voltage and a much higher speed than the planar memory devices.[11,12]

Recently, high-κ dielectrics, such as HfO_2 and Al_2O_3, have been explored as materials to replace nitride in the SONOS CT-type memory.[13,14] Compared with nitride, the high-κ trapping layer can improve the P/E efficiency and enlarge the programming window owing to its reduced equivalent oxide thickness (EOT) and higher charge-trapping density.[15] Furthermore, the reduced electric field across the blocking oxide also resolves the overerasing issue. From previous studies,[16,17] the HfO_2 CT layer shows a high P/E efficiency but a low retention level because of its liability to recrystallize. On the other hand, the Al_2O_3 CT layer shows a low P/E efficiency but a high retention level owing to its deep trap states.[18] It has also been reported that HfAlO is a promising material with a high crystallization temperature and can preserve the specific advantages associated with HfO_2 and Al_2O_3.[17,19]

In this work, we study memory devices with a GAA NW channel and a Hf-based CT layer. In order to realize low-cost, high-performance, and low-power portable electronic products, the integration of logic circuits and memory components on the same panel or chip is necessary. However, the fabrication of NW devices typically requires advanced lithographic tools. This is an issue in the manufacturing of flat-panel products where the device feature size is generally 5 to 10 µm. To address this concern, we propose a simple approach that is capable of fabricating planar and NW poly-Si devices simultaneously without resorting to the use of advanced lithographic tools. Greatly enhanced P/E efficiency and retention characteristics of the GAA NW structure with respect to the planar counterpart of the poly-Si devices are clearly evidenced by the measured results.

2. Device fabrication

Figure 1 shows the process sequence for fabricating planar poly-Si thin-film transistors (TFTs) together with the GAA NW CT-type memory device simultaneously. In addition, the cross-sectional view of the device structure and the top view of the device layout at key steps are also shown to help elucidate the process features. The fabrication began on a Si wafer capped with a thick thermal oxide layer to simulate a glass substrate. First, 80-nm-thick silicon nitride, 30-nm-thick tetraethoxysilane (TEOS) oxide, and 30-nm-thick silicon nitride layers were deposited on the wafer surface sequentially by low-pressure chemical vapor deposition (LPCVD), as shown in Fig. 1(a). After a conventional lithographic process, anisotropic dry etching was performed to etch the nitride and TEOS oxide layers to form a dummy pattern on the surface, as shown in Fig. 1(b). Then, HF-based wet etching was performed to selectively remove the oxide layer from the sidewall of the stack and form cavities underneath the top nitride layer at the sidewall of the dummy structure, as shown in Fig. 1(c). This was followed by the deposition of a 100 nm amorphous silicon (a-Si) layer by LPCVD, and the cavities were fully refilled with the a-Si layer that was subsequently transformed into a polycrystalline phase by solid-phase crystallization (SPC) at 600 °C in N_2 ambient for 24 h, as shown in Fig. 1(d). Afterwards, photoresist (PR) patterns were generated to cover the source/drain (S/D) regions of the NW memory device and the active region of the planar device [see Fig. 1(e)], followed by an anisotropic dry etching process to define these regions. The Si film contained in the cavities remained after the etching process and subsequently formed the NW channels. When

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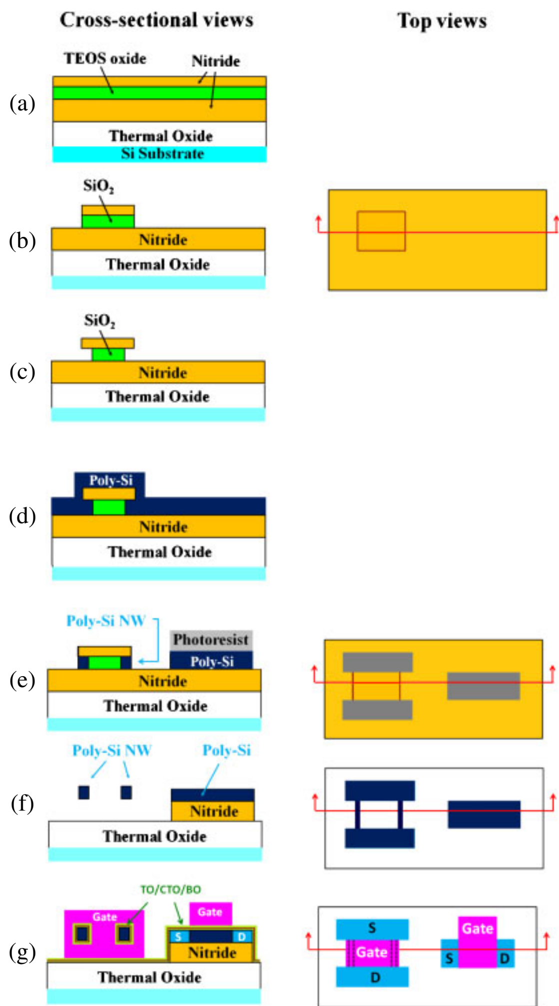
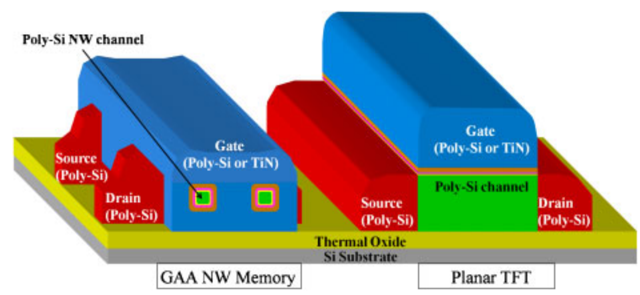


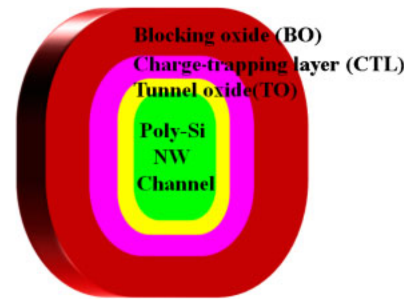
Fig. 1. (Color online) Schematic diagrams of the fabrication process of planar TFTs and GAA NW HfAlO CT memory devices. The left figures show cross-sectional views of the devices at key steps, and the right figures are the corresponding top views.

Table I. Sample and material/thickness for the dielectric stack and electrode layer. The atomic ratio of HfAlO is Hf 14% : Al 30% : O 56%.

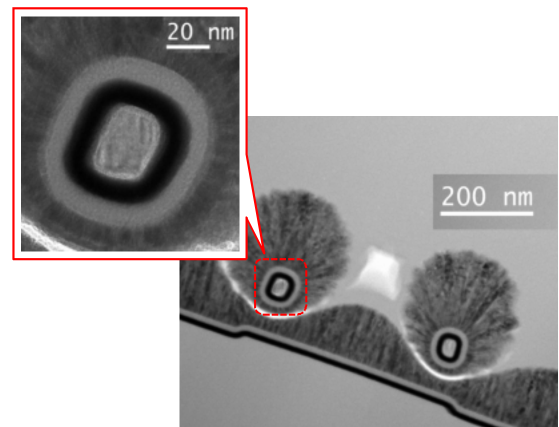
Sample split	Tunnel oxide (3 nm)	CT layer (10 nm)	Blocking oxide (11 nm)	Gate electrode (150 nm)
SiN	SiO_2	SiN	SiO_2	n^+ poly-Si
HfO_2	SiO_2	HfO_2	Al_2O_3	TiN
HfAlO	SiO_2	HfAlO	Al_2O_3	TiN



(a)



(b)



(c)

Fig. 2. (Color online) (a) Stereoscopic view of the completed GAA NW and planar devices. (b) Channel cross sections of the GAA NW CT-type device under various TO/CTL/BO and gate conditions. (c) Cross-sectional TEM image of a NW device with HfAlO as the CT layer.

the top nitride, side TEOS oxide, and bottom nitride layers were selectively removed, the Si NWs hung between the source and drain regions, as shown in Fig. 1(f). Then, a stack consisting of tunnel oxide/CT layer/blocking oxide (3 nm/10 nm/11 nm) and gate layers was sequentially deposited. Three types of memory devices with various dielectric stacks and gate electrodes were fabricated in this work. Details of their structural conditions are shown in Table I. The TEOS oxide layer deposited by LPCVD was used as the tunnel oxide layer. The CT layers for the three types of memory devices are SiN, HfO_2, and HfAlO (the atomic ratio of Hf/Al/O is 0.14/0.30/0.56). SiN was prepared by LPCVD, while both HfO_2 and HfAlO were prepared by atomic layer deposition (ALD). For the HfO_2 and HfAlO splits, an Al_2O_3 blocking oxide layer was also deposited by ALD.

The gate electrode was subsequently defined by dry etching, and then self-aligned phosphorus ion implantation (25 keV, $2 \times 10^{15}\,cm^{-2}$) was carried out to dope the S/D regions of the devices, as shown in Fig. 1(g). Finally, a passivation oxide layer was deposited to cover the fabricated devices, followed by normal metallization steps to form Al–Si–Cu metal contacts. Finally, after the deposition of gate dielectrics and electrodes, all devices were treated by postmetallization annealing (PMA) at 600 °C for 30 s.

A stereoscopic view of the completed GAA NW and planar devices is shown in Fig. 2(a). Figure 2(b) shows the channel cross section of the GAA NW CT-type device. Various tunnel oxide/charge trapping layer/blocking oxide (TO/CTL/BO) and gate conditions are shown in Table I. A transmission electron microscopy (TEM) image of a NW device with HfAlO as the CT layer is shown in Fig. 2(c).

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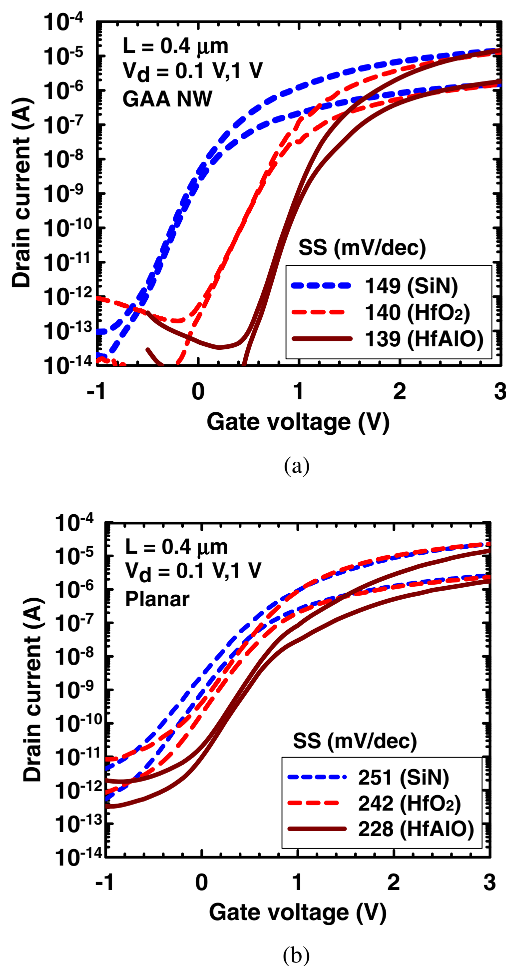

Fig. 3. (Color online) Transfer characteristics of (a) GAA and (b) planar devices with HfAlO, HfO_2, and SiN CT layers.

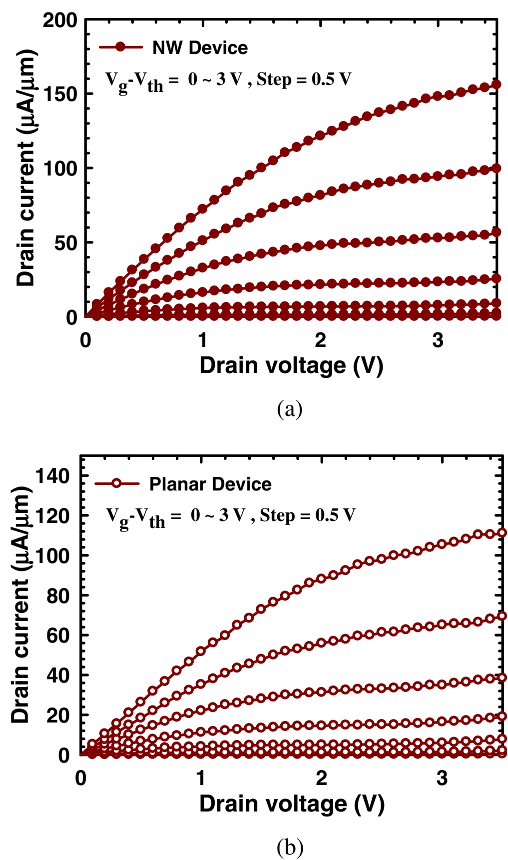

Fig. 4. (Color online) Output characteristics of (a) GAA device and (b) planar TFT with HfAlO CT layer.

3. Results and discussion

3.1 Basic electrical characteristics

With the proposed scheme, conventional planar and GAA NW devices are fabricated and integrated easily on the same substrate. According to the process conditions mentioned in the previous section, the major split condition of the fabrication is the CT dielectric material; thus, in the following analysis and discussion, we simply use the CT dielectric to denote each split. Figures 3(a) and 3(b) show the transfer characteristics of all splits of the devices with GAA NW and planar structures, respectively. The channel lengths of these devices are 0.4 μm. Good device characteristics are demonstrated in both types of structures. The shift in threshold voltage (V_{th}) is attributed to the differences in the gate workfunction and fixed charge density in the CT dielectric. However, among the devices with the same CT dielectric, the GAA NW device always shows better short-channel characteristics than its planar counterpart, such as a smaller subthreshold swing (SS <150 mV/dec), negligible drain-induced barrier lowering (DIBL) values (55.6, 12.8, and 61.1 mV/V for SiN, HfO_2, and HfAlO devices, respectively), and a lower off-state leakage. This is attributed to the GAA configuration, which enhances the gate controllability over the channel potential, and the tiny NW channels, which tend to reduce the off-state leakage.[20–22] Furthermore, the standard deviations of the ON currents (I_{on} at $V_g - V_{th} = 1.5$ V, $V_d = 0.1$ V) of all the GAA NW devices are very small, i.e., 96.7, 103.6, and 128.3 nA for the SiN, HfO_2, and HfAlO devices, respectively.

The output characteristics of the HfAlO GAA NW and planar TFTs are shown in Figs. 4(a) and 4(b), respectively. Good performance is obtained for the two devices. However, the normalized ON current is much higher for the NW TFT. This is again attributed to its tiny channel, which contains much fewer grain boundary defects than the 100-nm-thick channel of its planar counterpart.[23] It is well known that the transport of carriers in a poly-Si channel is greatly impeded by the potential barrier at the grain boundaries.[24,25] It was pointed out previously[26] that the modulation of the barrier height at the grain boundaries by the gate bias is more efficient in a multigate NW device than in planar devices. This explains why the drain current of the GAA NW device outperforms that of the planar device, as shown in Figs. 4(a) and 4(b).

3.2 P/E characteristics

For P/E operations, a high gate voltage is applied while grounding both the source and the drain. For simplicity, V_{th} is obtained from the transfer curves with the drain current of 10^{-9} A at V_d of 0.1 V. Figure 5(a) shows the V_{th} shift versus the programming time for NW devices with a HfAlO CT layer programmed at 14, 15, and 16 V. To illustrate the improvement of the GAA NW configuration, the characteristics of the planar counterpart programmed at 14 V are also

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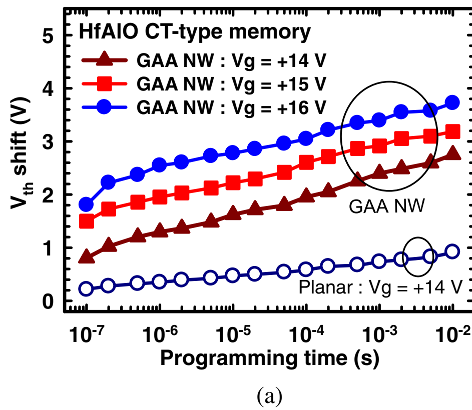
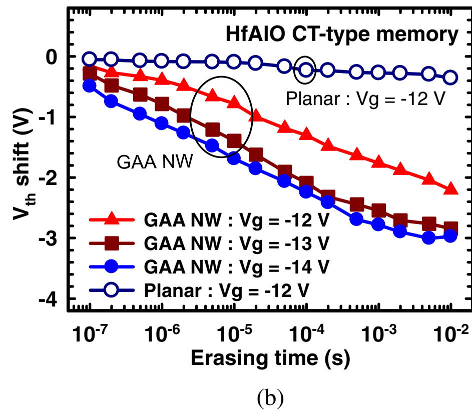
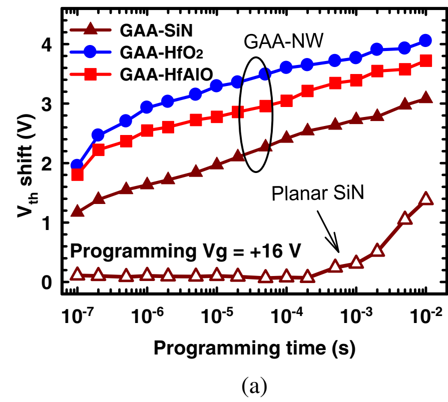


(a)

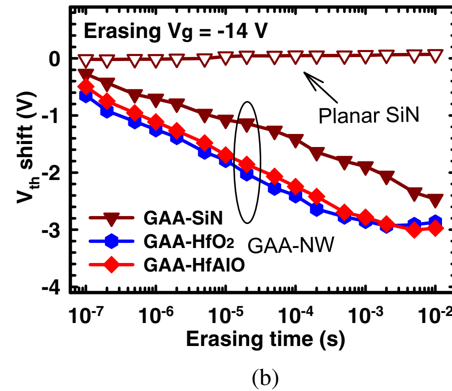


(b)

Fig. 5. (Color online) V_{th} shift as a function of (a) programming time and (b) erasing time for GAA NW devices with HfAlO CT layer at different voltages. The results for the planar device stressed at 14 and −12 V are also shown in (a) and (b), respectively.



(a)



(b)

Fig. 6. (Color online) V_{th} shift as a function of programming time for the three splits of GAA NW devices stressed at (a) 16 and (b) −14 V. The results for a planar SONOS device are also shown.

included in the figure. Owing to the higher electric field across the tunnel oxide layer that resulted from the use of the NW channel,[27] the GAA NW devices exhibit an enhanced operation efficiency as compared with the planar one and achieve a 3 V shift in 50 µs at the gate bias of 16 V. The erasing characteristics of the programmed HfAlO GAA NW devices are also studied. Figure 5(b) shows the results of the V_{th} shift of HfAlO GAA NW devices as a function of erasing time at the gate biases of −12, −13, and −14 V. The erasing characteristic of a planar counterpart is also shown in Fig. 5(b). Still, the HfAlO GAA NW devices show a higher erasing speed than the planar ones and achieve a shift of >2 V in 100 µs at the gate bias of −13 V. It can be seen that the rate of the V_{th} shift decreases when the erasing time is longer than 0.5 ms, which is presumably related to the injection of electrons from the gate.[17]

To further illustrate the merits of the high-κ CT layer and GAA configuration, typical P/E characteristics of the NW devices with various CT layers and planar SONOS devices are shown and compared in Figs. 6(a) and 6(b). The P/E performance of the conventional planar SiN device clearly lags far behind that of the GAA NW ones. Furthermore, among the three splits of GAA NW devices, the HfO_2 split shows the highest efficiency, while the HfAlO split exhibits comparable performance, indicating that the P/E speed of the HfAlO split is similar to that of HfO_2 split. This is attributed to the higher electric field across the tunnel oxide layer that resulted from the use of thinner EOTs; thus, the HfO_2 and HfAlO devices exhibit a greatly enhanced operation efficiency as compared with the SiN GAA device.

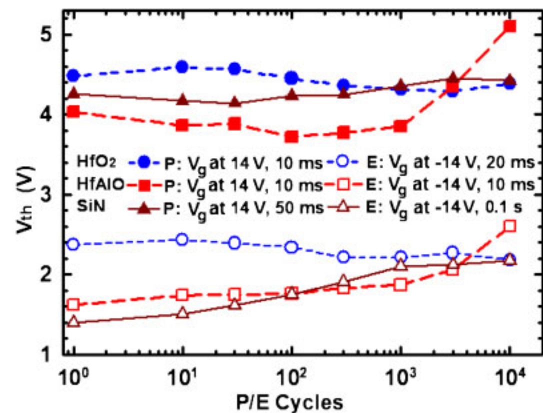


Fig. 7. (Color online) Endurance characteristics for the three splits of the fabricated devices at room temperature. The solid and open symbols stand for the threshold voltages in the programmed and erased states, respectively.

The endurance characteristics of the three splits of the GAA NW devices are shown in Fig. 7. The P/E conditions used in each split to create comparable windows are also given in the figure. It is seen that all the devices maintain acceptable memory windows after 10^4 P/E cycles. Nevertheless, the memory window of the SiN memory device shrinks slightly, primarily owing to the increase in V_{th} for the erased state. The V_{th} of the two logic states of the HfO_2 device clearly increases after 10^3 P/E cycles. To gain insights into the origins of the increase in V_{th} for the HfO_2 device after

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10^3 P/E cycles, we inspected the evolution of transfer characteristics after various numbers of P/E cycles. Figure 8 shows transfer characteristics of the three GAA NW devices after various numbers of P/E cycles (1 to 10^4). It is clear that the SS values of the SiN and HfO_2 devices degrade markedly after 10^3 P/E cycles, while the HfAlO GAA NW device exhibits only minor changes even after 10^4 P/E cycles. In the SiN GAA memory device, the lowest P/E efficiency is obtained [as shown in Figs. 6(a) and 6(b)]. In order to obtain a memory window comparable to those of the Hf-based splits, a much longer P/E stress time on the SiN device is needed. This is believed to be responsible for the degradation of SS in Fig. 8(a). The increase in V_{th} for the SiN device in the erased state after 100 P/E cycles is attributed to the largest SS value and the accumulation of residual charges in the SiN device during the P/E operations.[28]

In the HfO_2 GAA device, the most severe degradation of SS and the largest drift in V_{th} after 10^4 P/E cycles are observed among all the splits, as shown in Fig. 8(b). The severe degradation of SS should be related to the generation of extra interface state traps as well as nonuniform charge trapping. The situation is significantly improved when HfAlO is used instead of HfO_2 as the CT layer, as shown in Fig. 8(c). The different outcomes of the two splits are attributed to the different crystallinities of the CT layers. It was reported that a HfO_2 film starts to crystallize at 300 °C,[29,30] while a HfAlO film remains amorphous even after annealing at 800 °C for a considerable period.[17,31] Therefore, the PMA treatment (600 °C) in the fabrication process should make the HfO_2 trapping layer polycrystalline and generate grain boundaries (GBs) in the thin film. Since the defect density is high at or near the GBs, the use of the polycrystalline CT layer may result in a nonuniform distribution of the charges stored inside the layer. The excessive charges stored in or near the GBs should leak out easily owing to the increase in local electric potential. As a result, after a sufficient number of P/E cycles, the nearby tunnel oxide layer should experience far more carrier tunneling events than elsewhere and thus more damage. This leads to the degradation observed in the *I*–*V* curves. By incorporating Al into the dielectric, the thermal stability is promoted by increasing the recrystallization temperature to 800 °C. Therefore, in contrast to the HfO_2 device, the HfAlO one shows the best endurance characteristics and exhibits minor changes in transfer characteristics even after 10^4 P/E cycles.

Figures 9(a) and 9(b) show the retention characteristics of the three splits of the GAA NW devices at 25 and 85 °C, respectively. The HfAlO device clearly outperforms the SiN and HfO_2 ones according to the figure. The extrapolated window after ten years for the HfAlO device is about 2.1 V, which is much larger than those of the HfO_2 (~1 V) and SiN (~0.6 V) devices. As compared with the SiN split, the Hf-based ones show better retention performance because of the deeper traps in the trapping layers.[16] Furthermore, as compared with the HfO_2 split, the HfAlO split shows outstanding retention performance. Such an improvement is also a result of the higher crystallization temperature.

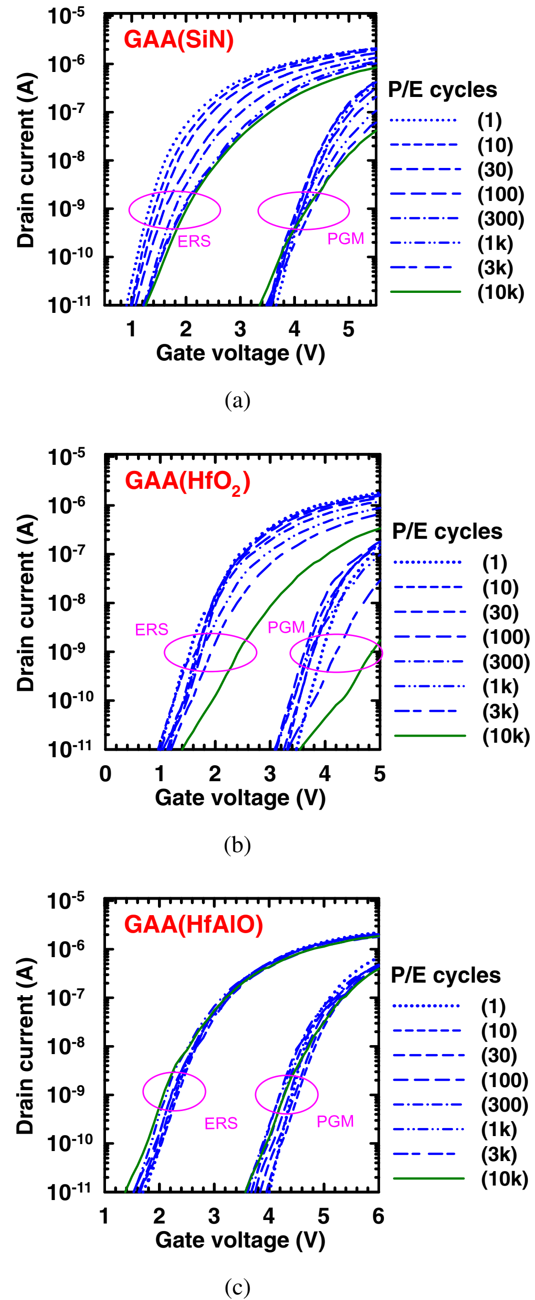

Fig. 8. (Color online) Subthreshold characteristics of (a) SiN, (b) HfO_2, and (c) HfAlO CT-type GAA devices measured after various numbers of P/E cycles. Among them, the HfAlO device shows the best endurance characteristics, such as the smallest shift in SS and drift in V_{th} even after 10^4 P/E cycles.

4. Conclusions

GAA NW CT-type memory devices with various CT materials were characterized. These devices were fabricated on the same substrate with planar TFT devices using a process that can easily be implemented in a modern manufacturing process. Equipped with a GAA configuration and a poly-Si NW channel, the devices with a HfO_2 CT medium show a high P/E speed but low retention and endurance characteristics. Nonuniform charge trapping in the polycrystalline HfO_2 trapping layer is believed to be responsible for the above reliability issues. In contrast, the memory device with the HfAlO CT layer shows comparable P/E efficiency but superior retention and endurance characteristics as compared with the HfO_2 device. The improvements are attributed to the retardation of recrystallization with the incorporation of Al into the Hf-based dielectric.

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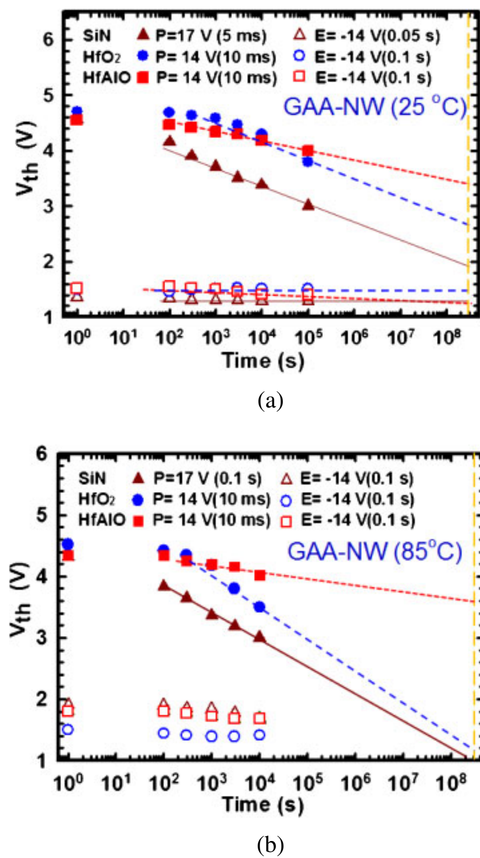

Fig. 9. (Color online) Retention characteristics for the three splits of the fabricated devices at (a) 25 and (b) 85 °C. The HfAlO split shows superior data retention characteristics.

Acknowledgments

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