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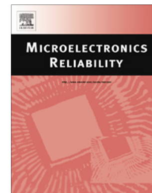

SCR-based transient detection circuit for on-chip protection design against system-level electrical transient disturbance

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ABSTRACT

A new silicon controlled rectifier (SCR)-based transient detection circuit for on-chip protection design against system-level electrical transient disturbance is proposed. The circuit function to detect positive or negative electrical transients during system-level electrostatic discharge (ESD) and electrical fast transient (EFT) tests has been verified in silicon chip. The experimental results in a 0.18-μm CMOS process have confirmed that the new proposed detection circuit can successfully memorize the occurrence of system-level electrical transient disturbance events. The detection results can be cooperated with firmware design to execute system recovery procedures, therefore the immunity of microelectronic systems against system-level ESD or EFT tests can be effectively improved.

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1. Introduction

System-level electrical transient disturbance has become an important immunity issue in microelectronic products which are equipped with CMOS integrated circuits (ICs) [1–6]. With the increase of electromagnetic emission sources in a microelectronic system, the environment where the CMOS ICs located has more electrical transient disturbance than before. The microelectronic systems were typically requested to pass the immunity tests, including the system-level electrostatic discharge (ESD) test of IEC 61000-4-2 standard [7] and the electrical fast transient (EFT) test of IEC 61000-4-4 standard [8].

Compared with the component-level ESD tests (where the objects under test are ICs), the system-level ESD test aims to evaluate the robustness of microelectronic products against ESD events. The equivalent circuit of human body model (HBM) in the component-level ESD test is shown in Fig. 1(a). The HBM has the charging (energy-storage) capacitor of 100 pF and a discharging resistor of 1.5 kΩ. The equivalent circuit of ESD gun used in the system-level ESD test is shown in Fig. 1(b), where the charging capacitor (discharging resistor) is 150 pF (330 Ω) [7]. Thus, comparing to the ESD current in component-level ESD test, the system-level ESD test with the same ESD voltage has much larger peak ESD current (5–6 times larger) to cause serious damages on electronic products. During the system-level ESD test, the voltage waveforms on the power line of the IC inside the microelectronic system would no longer maintain their normal voltage levels. The typical underdamped sinusoidal voltage with the amplitude of several tens volts induced by system-level ESD test is shown in Fig. 2. In addition, the simplified circuit diagram of EFT generator is shown in Fig. 3 with the impedance matching resistor R_m of 50 Ω and the dc blocking capacitor C_d of 10 nF, as specified in the EFT test standard of IEC 61000-4-4. The EFT is a test with repetitive burst string consisting of a number of fast pulses, coupled into power lines, control line, and signal ports of microelectronic system. For EFT pulses with the repetition frequency of 5 kHz, the measured 200-V voltage waveforms on the 50 Ω load are shown in Fig. 4. Due to impedance matching, the measured output voltage pulse peak is half of the EFT voltage pulse. The waveform of a single pulse has a rise time of ~5 ns and the pulse duration of ~50 ns, as shown in the inset figure of Fig. 4.

Such ESD/EFT-generated transient voltages are quite large (with the amplitude of several tens to hundreds volts) and fast (with the period of several tens nanoseconds), those could randomly couple to the power, ground, or input/output (I/O) pins of ICs inside the microelectronic system. Such fast transients often cause the microelectronic system to be upset or frozen after the system-level ESD or EFT tests. It was reported that, the underdamped sinusoidal voltage waveforms during system-level ESD tests coupled on V_{DD} and V_{SS} pins of a super twisted nematic (STN) liquid crystal display (LCD) driver circuit caused abnormal display function of LCD panel [9]. It was also proven that the EFT-induced transient disturbance can cause electrical-over-stress (EOS) damage in a AC-power equipment [10]. Such high-energy ESD/EFT-induced fast transients caused serious reliability events on CMOS ICs inside the microelectronic products [11–18].

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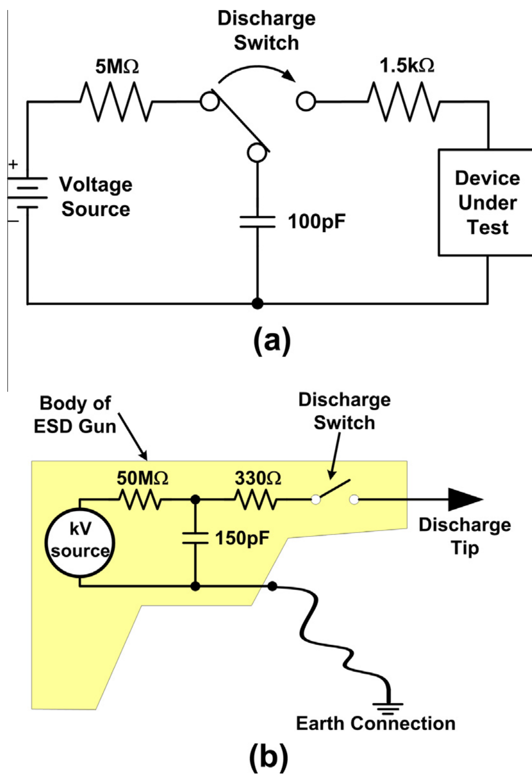


Fig. 1. Equivalent circuits of (a) human body model (HBM) used in the component-level ESD test, and (b) ESD gun used in the system-level ESD test. The charging (energy-storage) capacitors and the discharging resistors are different in these two different ESD test standards.

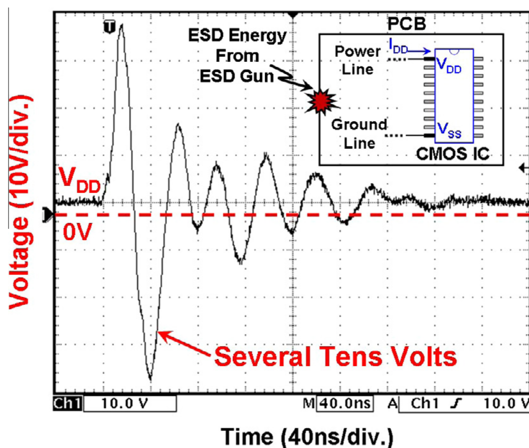


Fig. 2. The measured waveforms of transient noise voltage on the power pin of CMOS IC in the equipment under test (EUT) during the system-level ESD test.

The additional noise filter networks, such as the magnetic core, capacitor filter, ferrite bead (FB), transient voltage suppressor (TVS), or RC filters, were often used to improve the immunity of microelectronic products against electrical transient disturbance [19,20]. However, the additional discrete noise-bypassing components substantially increase the total cost of microelectronic products. Therefore, the chip-level solutions to meet system-level ESD/EFT specifications for microelectronic products without using additional discrete noise-decoupling components on the printed circuit board (PCB) are highly desired by IC industry [21–26].

In this work, a new on-chip SCR-based transient detection circuit is proposed to detect the system-level electrical transient disturbance under the system-level ESD or EFT tests [27]. In this new design, the p-type substrate-triggered SCR (P_STSCR) device is used as the storage cell [28–30] to memorize the occurrence of system-level ESD or EFT events. Such a SCR-based circuit design to detect the electrical transient disturbance is first reported in the literature. The transient-induced latchup (TLU) measurement [31], system-level ESD gun [32], and EFT test [33] are used to evaluate the detection function of the new proposed detection circuit. The experimental results with the chip fabricated in a 0.18-μm CMOS process have verified that the new proposed on-chip SCR-based transient detection circuit can successfully detect and memorize the occurrence of electrical transients generated by system-level ESD or EFT tests.

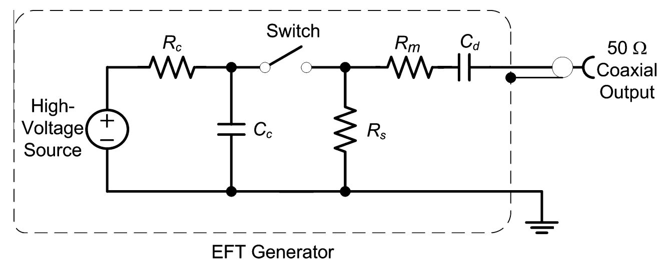


Fig. 3. Simplified circuit diagram of EFT generator [8], which was specified in IEC 61000-4-4.

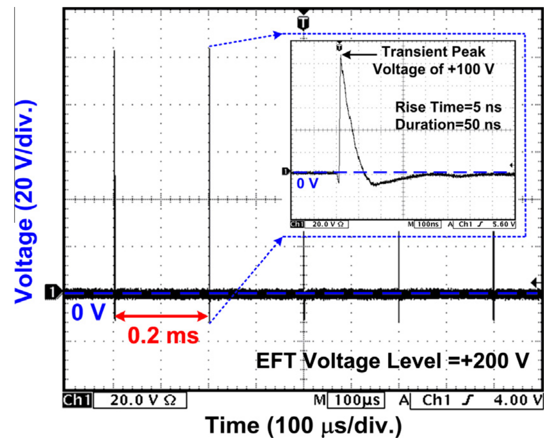


Fig. 4. Measured voltage waveforms of EFT pulses on a 50-Ω load with the repetition rate of 5 kHz and EFT voltage of +200 V.

2. Solutions to overcome system-level transient disturbance

2.1. Traditional solution

In order to meet the system-level ESD specifications, there are two main methods [19,20]. One method is to add some discrete noise-bypassing components or board-level noise filters into the microelectronic products to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD or EFT tests. As shown in Fig. 5, some discrete components (such as the ferrite bead (FB) and RC low-pass filters) are added into the printed circuit board (PCB) of an universal serial bus (USB) product to restrain the electrical transients. The immunity of microelectronic system (equipped with CMOS ICs) against electrical transient disturbance can be significantly enhanced by choosing proper noise filter networks. The other method is to regularly check the system abnormal conditions by using an external hardware timer, such as

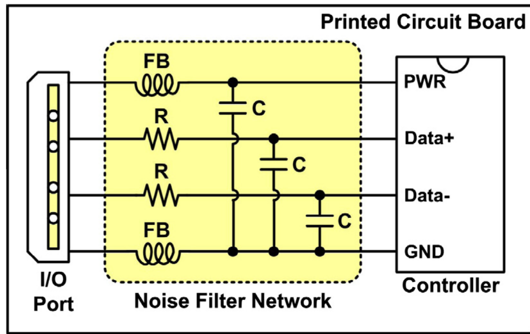


Fig. 5. A traditional solution to overcome the system-level electrical transient disturbance by adding board-level discrete components, such as the ferrite bead (FB) and RC low-pass filters.

watch dog timer. The additional hardware timer is often designed with registers or flip flops as a reference clock for system operation if the main program was locked or frozen due to some fault conditions. However, during system-level ESD or EFT tests, the logic states stored in the registers or flip flops of hardware timer would be also destroyed, which still causing malfunction or frozen condition in the system operation.

2.2. Hardware/firmware co-design

It had been reported that the hardware/firmware co-design can effectively improve the system-level ESD susceptibility of the CMOS IC products [21]. As shown in Fig. 6 with hardware/firmware co-design, when ESD-induced transient disturbance coupling to V_{DD}/V_{SS} lines, the detection results (V_{OUT}) from the on-chip transient detection circuit can be temporarily stored as a system recovery index for firmware check. For example, the output (V_{OUT}) state of the on-chip transient detection circuit and the firmware index are initially set to logic "1". When the fast electrical transient happens, the on-chip transient detection circuit can detect the fast electrical transient and then change the output state (V_{OUT}) from logic "1" to logic "0". The system recovery index is therefore flagged at logic "0", which will inform the firmware to recover all system functions to a stable state as soon as possible. After the recovery procedure, the output state of the on-chip transient detection circuit and the firmware index are re-set to logic "1" again for detecting the next electrical transient disturbance events.

Table 1
Classifications of system-level ESD test.

Criterion	Classification
Class A	Normal performance within limits specified by the manufacturer, requestor or purchaser.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention. (Automatic Recovery)
Class C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention. (Manual Recovery)
Class D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

In IEC 61000-4-2 standard, four classifications of system-level ESD test results have been defined, as listed in Table 1. In order to solve the frozen states caused by system-level ESD test, microelectronic products can be manually reset by operator intervention, which meets the criterion of "Class C" in the standard. However, most microelectronic products are required to automatically recover the system functions without operator intervention to meet the "Class B" criterion by IC industry. By cooperating with the on-chip transient detection circuit, a hardware/firmware co-design solution can be provided to release the locked states caused by electrical transient disturbance without additional manual operations.

3. New on-chip SCR-based transient detection circuit

The new SCR-based transient detection circuit is designed to detect the positive or negative fast electrical transients during the system-level ESD or EFT tests. Under the normal circuit operation condition (V_{DD} = 3.3 V), the output state of the new proposed SCR-based transient detection circuit is kept at 3.3 V as logic "1". After the transient disturbance, the output state will transit from

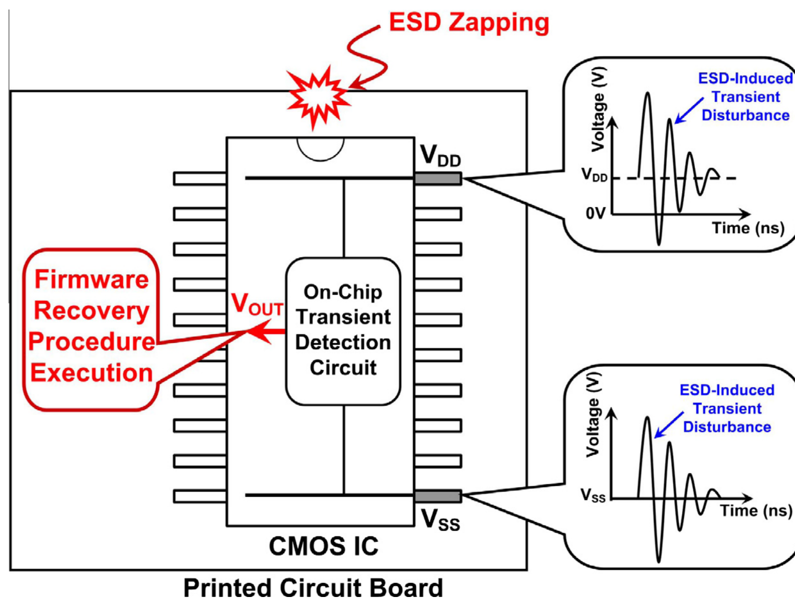


Fig. 6. Hardware/firmware co-design for system recovery by using the detection results of the on-chip transient detection circuit.

3.3 V to 0 V. Therefore, the new proposed SCR-based transient detection circuit can memorize the occurrence of system-level electrical transient disturbance events.

3.1. Silicon controlled rectifier (SCR)

The silicon controlled rectifier (SCR) was traditionally used as the on-chip ESD protection device due to its high ESD robustness within small layout area [34]. The anode of SCR is connected to the P+ and N+ diffusions in N-well (NW), whereas the cathode of SCR is connected to the N+ and P+ diffusions in P-well (PW). The equivalent circuit of the SCR structure is composed of a lateral NPN and a vertical PNP bipolar transistor to form the 2-terminal/4-layer PNPN (P+/NW/PW/N+) structure. The original switching voltage of the SCR device is decided by the avalanche breakdown voltage of the N-well/P-well junction. It has been reported that the turn-on mechanism of SCR device is essentially a current triggering event [35]. While a current is applied to the base or substrate of SCR device, the SCR can be quickly triggered into its latching state. The device cross-sectional view and the layout top view of the p-type substrate-triggered SCR (P_STSCR) are shown in Fig. 7(a) and (b), respectively. An extra P+ diffusion is inserted into the P-well of the P_STSCR device structure and connected out as the p-trigger node of the P_STSCR device. The layout parameters, D and W, represent the distance between the anode and cathode, and the distance between the adjacent well contacts, respectively. In this work, the P_STSCR structure with the layout parameters of $D = 0.86\ \mu m$ and $W = 3.8\ \mu m$ in a 0.18-μm CMOS process with 3.3-V devices is used as the memory unit to memorize the occurrence of electrical transient disturbance. The SCR in this work is not used as on-chip ESD protection device, but as the memory unit in the transient detection circuit.

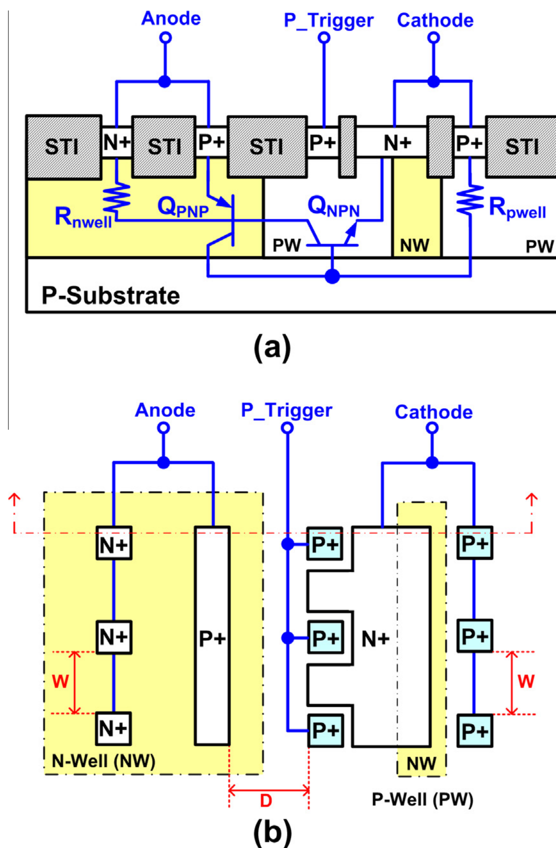


Fig. 7. (a) Device cross-sectional view and (b) layout top view, of the p-type substrate-triggered SCR (P_STSCR) with the layout parameters of $D = 0.86\ \mu m$ and $W = 3.8\ \mu m$.

The setup to measure the dc current–voltage (I–V) curves of the fabricated P_STSCR device under substrate-triggered current (I_{bias}) is shown in Fig. 8. The measured dc I–V curves of the P_STSCR under different substrate-triggered currents are shown in Fig. 9. When the substrate-triggered current applied to the p-trigger node is increased from 1 mA to 4 mA, the switching voltage of P_STSCR is reduced from 8.6 V to 1.5 V. With the substrate-triggered current, the P_STSCR structure can be triggered into the latching state without involving the avalanche junction breakdown.

3.2. SCR-Based transient detection circuit

In the previous works, some on-chip transient detection circuits were reported to detect the electrical transient disturbance under system-level ESD or EFT tests [21–26]. The traditional memory unit used to memorize the occurrence of system-level electrical transient disturbance was the “latch”, which was formed by two inverters.

The new proposed on-chip SCR-based transient detection circuit of this work is shown in Fig. 10. The P_STSCR device shown in Fig. 7 is used as the memory unit to memorize of the occurrence of system-level electrical transient disturbance. It has been proven

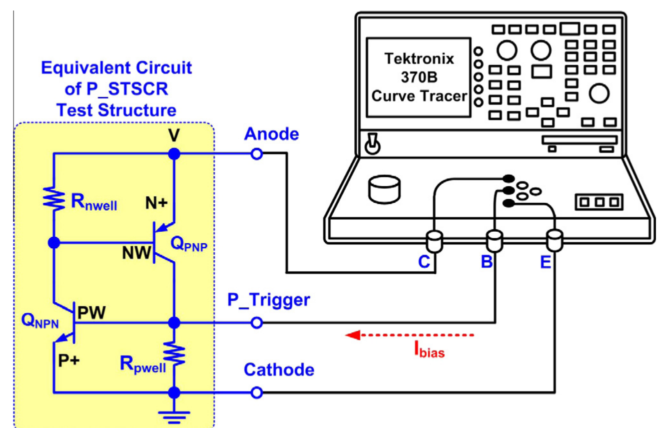


Fig. 8. Measurement setup of P_STSCR device under different trigger currents.

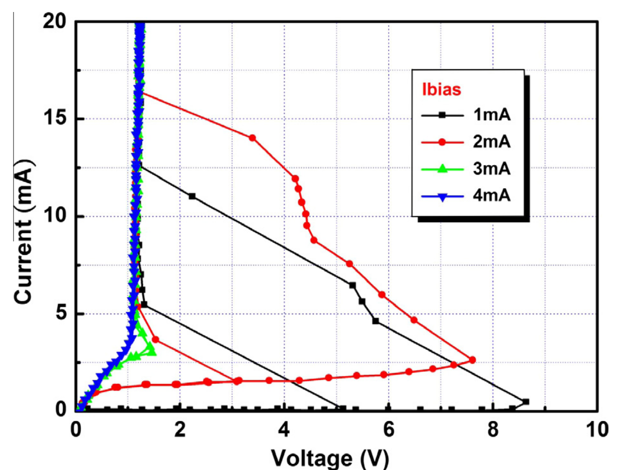


Fig. 9. The measured I–V characteristics of P_STSCR device under different trigger currents.

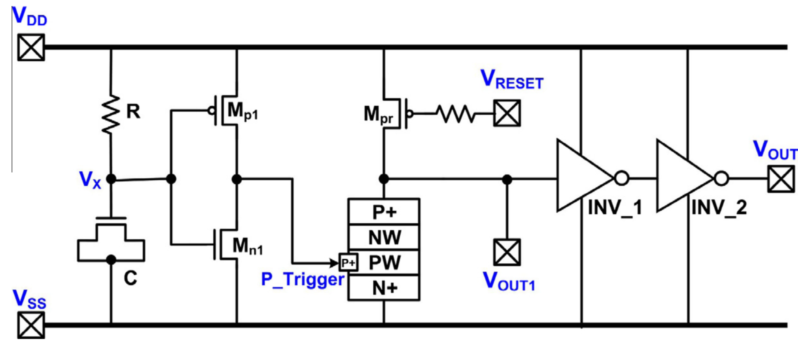


Fig. 10. The new proposed on-chip SCR-based transient detection circuit. The P_STSCR is used as memory cell to memorize the occurrence of electrical transient disturbance.

that SCR device can be triggered under system-level ESD or EFT tests, no matter which polarity (positive and negative) of the ESD or EFT voltage is [6]. The anode of P_STSCR is connected to the drain of PMOS (M_{pr}) device. The gate of PMOS (M_{pr}) is biased to V_{SS} by the initial reset signal (V_{RESET}) to set the initial output voltage (V_{OUT2}) at 3.3 V. The RC-delay circuit and the inverter are designed to provide the SCR triggering current. Under the system-level ESD or EFT events, the transient voltage has a fast rise time in the order of nanosecond (ns). The voltage level of V_X in the RC-delay circuit is initially biased at V_{DD} and has slower voltage response, because the RC-delay circuit is designed with a time constant in the order of microsecond (μs). When the electrical transient disturbance coupling to the V_{DD} line, the PMOS device (M_{p1}) can be turned on by the overshooting voltage at V_{DD} to conduct trigger current into the p-trigger node. The SCR device is therefore turned on to pull down the output voltage (V_{OUT1}) level to the SCR holding voltage of ~1.2 V. In the two-inverter buffer stage, the logic threshold voltage of inverter1 (INV_1) is designed at ~2.3 V and that of inverter2 (INV_2) is ~1.7 V. Therefore, after electrical transient disturbance, the V_{OUT2} of the proposed detection circuit will be changed from 3.3 V to 0 V to memorize the occurrence of system-level ESD/EFT-induced transient disturbance. The current flowing through the turned-on SCR is limited by the PMOS device (M_{p1}), which will not cause reliability issue on the SCR used in the proposed transient detection circuit. The reset function (V_{RESET}) is used to release the turn-on state of SCR device by turning M_{pr} off, and then reset the output voltage (V_{OUT2}) back to 3.3 V again for detecting the next system-level transient disturbance.

4. Experimental results

The proposed detection circuit has been designed and fabricated in a 0.18-μm CMOS process with 3.3-V devices. The fabricated test chip with the silicon area of 125 μm × 150 μm for the SCR-based transient detection circuit is shown in Fig. 11.

4.1. Transient-induced latchup (TLU) test

To evaluate the system-level ESD immunity of a single IC inside the equipment under test (EUT), a component-level transient-induced latchup (TLU) measurement setup was reported with the following two advantages [31]. First, the TLU immunity of a single IC can be evaluated by the measured voltage and current waveforms through the oscilloscope. Second, with the ability of generating an underdamped sinusoidal voltage, it can be accurately simulated how an IC inside the EUT is disturbed by the ESD-generated transient disturbance during the system-level ESD test. Fig. 12 illustrates such a component-level TLU measurement setup. A charging capacitance of 200 pF is used to store the charges as the TLU-triggering source, V_{Charge}, and then the stored charges are discharged to the device under test (DUT) through the relay. The underdamped sinusoidal voltage generated by TLU measurement is similar to the transient voltage on the power pins of CMOS ICs under the system-level ESD tests. Moreover, a small current-limiting resistance of 5 Ω is recommended to protect the DUT from electrical-over-stress (EOS) damage during the high-current (low-impedance) latching state.

Fig. 13(a) and (b) show the measured V_{DD}, V_{OUT1}, and V_{OUT2} transient voltage waveforms of the SCR-based transient detection circuit under the TLU tests with V_{Charge} of +9 V and −1 V, respectively. As shown in Fig. 13(a), under the TLU test with V_{Charge} of +9 V, V_{DD} begins to increase rapidly from 3.3 V with positive-going underdamped sinusoidal voltage waveform. During the TLU test, V_{OUT1} and V_{OUT2} are influenced simultaneously by the positive-going underdamped sinusoidal voltage coupled to V_{DD} power line. After the TLU test with the V_{Charge} of +9 V, the output voltage V_{OUT1} of the proposed transient detection circuit is changed from

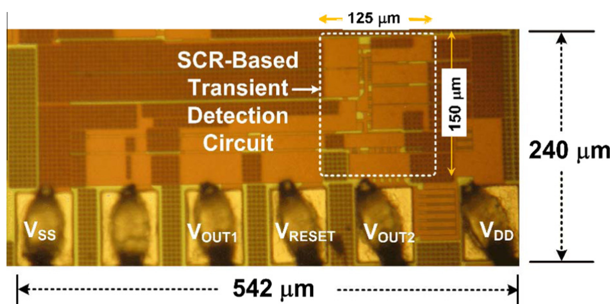


Fig. 11. Chip photo of the new proposed on-chip SCR-based transient detection circuit fabricated in a 0.18-μm CMOS process with 3.3-V devices. The silicon area occupied by the SCR-based transient detection circuit is only 125 μm × 150 μm.

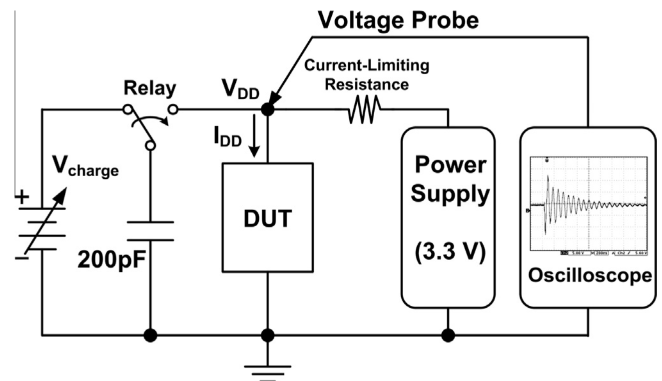


Fig. 12. Measurement setup for transient-induced latchup (TLU) [31].

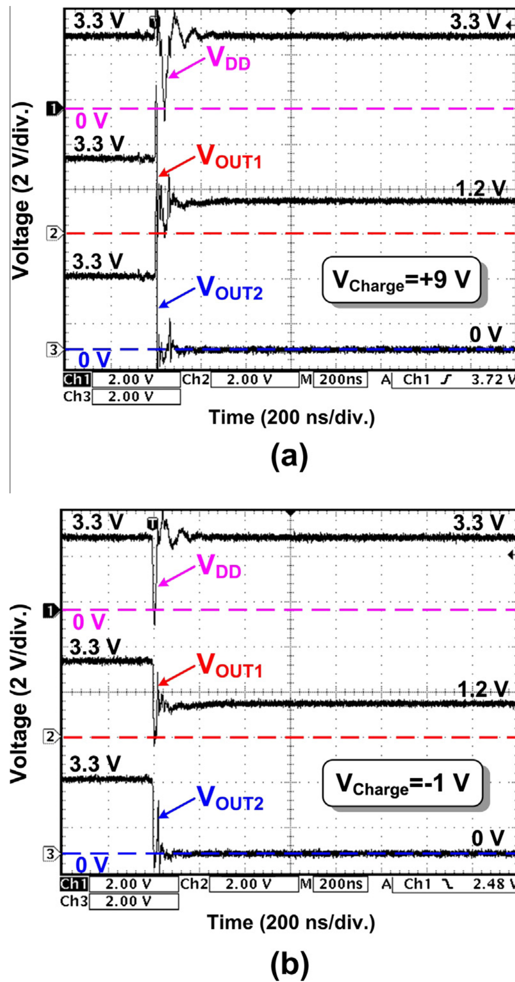


Fig. 13. Measured V_{DD} and V_{OUT} waveforms on the SCR-based transient detection circuit under TLU tests with the V_{Charge} of (a) +9 V and (b) −1 V.

3.3 V to 1.2 V (the SCR holding voltage). Through two-inverter buffer stage, V_{OUT2} of the proposed detection circuit is pulled down to 0 V. In Fig. 13(b), under the TLU test with V_{Charge} of −1 V, V_{DD} begins to decrease rapidly from 3.3 V with negative-going underdamped sinusoidal voltage waveform. During this TLU test, V_{OUT1} and V_{OUT2} are influenced simultaneously by the negative-going underdamped sinusoidal voltage. After the TLU test with the V_{Charge} of −1 V, the V_{OUT2} of the proposed transient detection circuit also transits from 3.3 V to 0 V.

From the TLU test results, the proposed SCR-based transient detection circuit can successfully memorize the occurrence of electrical transients. With positive or negative underdamped sinusoidal voltages coupling to V_{DD} power line, the output voltage (V_{OUT2}) of the proposed SCR-based transient detection circuit can be changed from logic "1" to logic "0" after TLU tests.

4.2. System-level ESD test

In IEC 61000-4-2, two test modes have been specified, which are the air-discharge and contact-discharge test modes. The contact discharge is applied to the conductive surfaces of the EUT (direct application) or to the coupling planes (indirect application). Contact discharge is further divided into direct discharge to the system under test, and indirect discharge to the horizontal or vertical coupling planes. Fig. 14 shows the measurement setup of the system-level ESD test standard with indirect contact-discharge test mode. The measurement setup of system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulation plane is used to separate the EUT from the horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470 kΩ resistors in series [7]. When the ESD gun zaps the HCP, the electromagnetic interference (EMI) coming from ESD gun will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

By monitoring in the oscilloscope, the transient responses on the power lines of CMOS ICs can be recorded and analyzed. Before each system-level ESD test, the initial output voltages (V_{OUT1} and V_{OUT2}) of the proposed detection circuit are all reset to 3.3 V. After each system-level ESD test, the output voltages (V_{OUT1} and V_{OUT2}) are monitored to check their final voltage levels. Thus, the function of the proposed detection circuit can be evaluated by system-level ESD tests in such a measurement setup.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms of the proposed detection circuit under system-level ESD test with the ESD voltage of +0.35 kV zapping on the HCP are shown in Fig. 15(a). V_{DD} begins to increase rapidly from the normal voltage level of 3.3 V. Meanwhile, V_{OUT1} and V_{OUT2} begin to change under such a high-energy ESD stress. During the fast transient disturbance, V_{DD}, V_{OUT1}, and

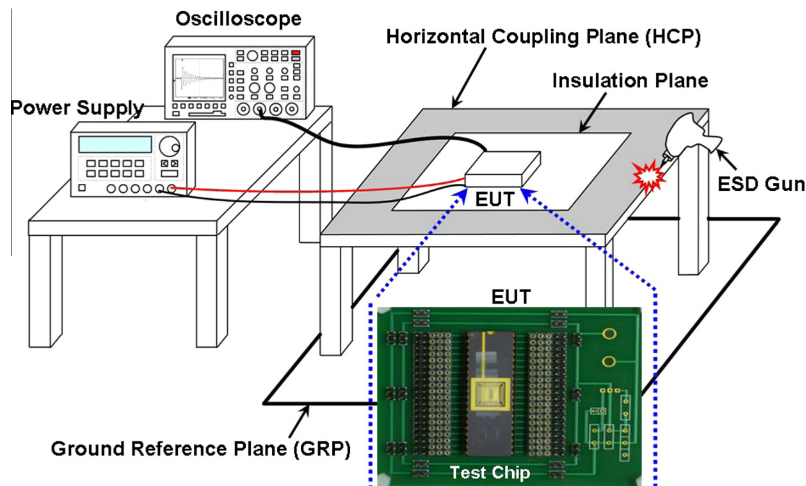
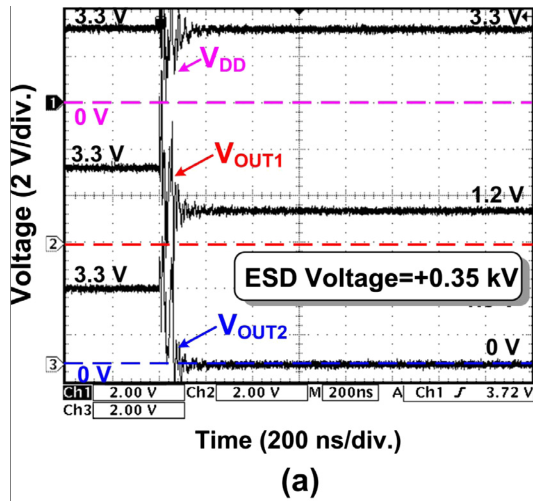


Fig. 14. Measurement setup for system-level ESD test with indirect contact-discharge test mode [7] to evaluate the detection function of the SCR-based transient detection circuit.



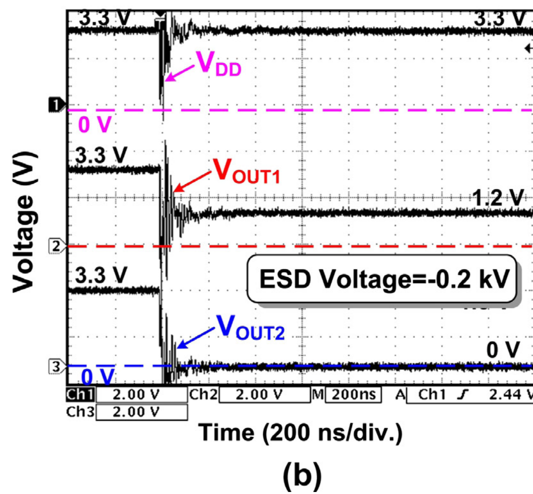


Fig. 15. Measured V_{DD} and V_{OUT} transient voltage waveforms of the SCR-based transient detection circuit under system-level ESD tests with ESD voltage of (a) +0.35 kV and (b) −0.2 kV.

V_{OUT2} are influenced simultaneously. Finally, V_{OUT1} is pulled down to 1.2 V. Through buffer stages, V_{OUT2} of the proposed detection circuit transits from 3.3 V to 0 V.

The measured V_{DD}, V_{OUT1}, and V_{OUT2} waveforms of the proposed detection circuit under system-level ESD test with the ESD voltage of −0.2 kV zapping on the HCP are shown in Fig. 15(b). During the ESD-induced transient disturbance, V_{DD} begins to decrease rapidly from the original voltage level of 3.3 V. Finally, the output voltage (V_{OUT2}) of the proposed transient detection circuit is changed from 3.3 V to 0 V.

Therefore, the new proposed SCR-based transient detection circuit can successfully detect the electrical transients under system-level ESD tests with positive or negative ESD voltages.

4.3. Electrical fast transient (EFT) test

The measurement setup for EFT test combined with attenuation network is shown in Fig. 16. EFT generator is connected to the DUT with V_{DD} of 3.3 V through the attenuation network. In order to simulate the degraded EFT-induced transient disturbance on CMOS ICs inside the microelectronic products, the attenuation network with −40 dB degradation is used in this work. The amplitude of EFT-induced transients can be adjusted by the attenuation network.

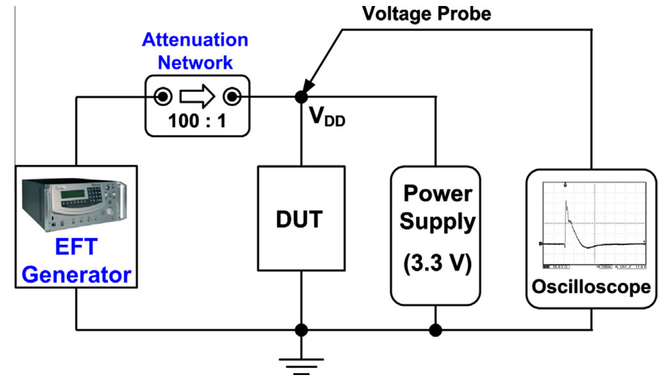
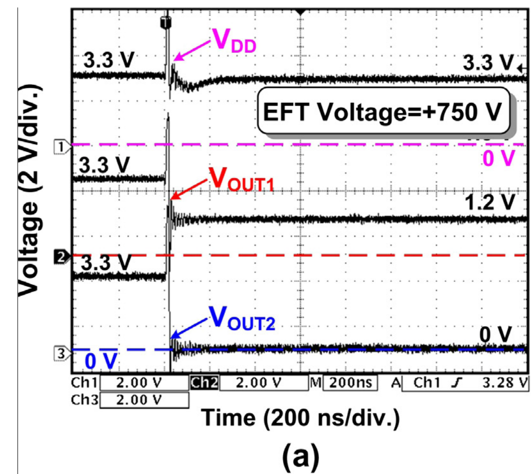


Fig. 16. Measurement setup for EFT test combined with attenuation network [8].



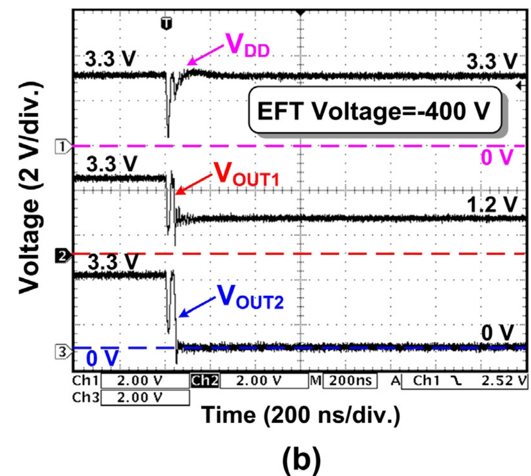


Fig. 17. Measured V_{DD} and V_{OUT} waveforms on the SCR-based transient detection circuit under EFT tests with (a) +750-V and (b) −400-V EFT voltages combined with attenuation network.

Fig. 17(a) and (b) show the measured V_{DD}, V_{OUT1}, and V_{OUT2} transient responses of the proposed detection circuit under the EFT tests with input EFT voltages of +750 V and −400 V, respectively. As shown in Fig. 17(a), under the EFT test with positive voltage of +750 V, V_{DD} begins to increase rapidly from 3.3 V with positive exponential voltage pulse. During the EFT test, V_{OUT1} and V_{OUT2} are influenced simultaneously by the positive exponential voltage pulse coupling to V_{DD} power line. After the +750-V EFT test, the

output voltage V_{OUT1} (V_{OUT2}) of the proposed detection circuit transits from 3.3 V to 1.2 V (0 V). In Fig. 17(b), under the EFT test with negative voltage of −400 V, V_{DD} begins to decrease rapidly from 3.3 V with negative exponential voltage pulse. After the EFT test, the output voltage V_{OUT2} of the proposed detection circuit transits from logic "1" to logic "0".

From the EFT test results shown in Fig. 17(a) and (b), with positive or negative EFT voltages coupled to V_{DD} power line, the output voltage (V_{OUT2}) of the proposed detection circuit can be changed from 3.3 V to 0 V. Therefore, the new proposed on-chip SCR-based transient detection circuit can successfully memorize the occurrence of EFT-induced exponential pulse transient disturbance.

5. Conclusion

A new SCR-based transient detection circuit to detect system-level electrical transient disturbance has been implemented in a 0.18-μm CMOS process with 3.3-V devices. By using P_STSCR device and RC-delay circuit, the proposed detection circuit is designed to detect fast electrical transients during the system-level ESD or EFT tests. Experimental results in silicon chip have successfully verified that the proposed detection circuit can successfully memorize the occurrence of electrical transients during system-level ESD or EFT tests. With hardware/firmware co-design method, the output state of the proposed SCR-based transient detection circuit can be used as the firmware index to provide an effective solution against the system malfunction caused by system-level electrical transient disturbance.

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