Studies of Safe Operating Area of InGaP/GaAs Heterojunction Bipolar Transistors

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***Abstract*— The safe operating area (SOA) of InGaP/GaAs heterojunction bipolar transistors has been studied in detail both experimentally and theoretically. Devices without ballasting resistors were measured in dc to reveal the intrinsic SOA characteristics, which are influenced by both self-heating and the breakdown effect. Two distinct regions in the SOA boundary were observed indicating two different dominating failure mechanisms at different bias conditions. The theoretical analysis, which took into consideration all the relevant effects, was able to explain all the features in the measured results. Secondary unstable points beyond the SOA boundary were found theoretically. These secondary failure points and the gap between the two branches of the SOA boundary explain why the device failure points when measured in constant I_b mode were different from those measured in constant V_b mode.**

***Index Terms*— Device ruggedness, heterojunction bipolar transistors (HBTs), power amplifiers, safe operating areas (SOAs).**

I. Introduction

IN ORDER for a semiconductor device to operate safely, one has to limit the device to work within certain current, voltage, or power range—the so called safe operating area (SOA). This area is determined by the physical mechanism that the devices are operated with and varies from technology to technology. For devices that are required to operate at extreme conditions, such as high powers and high voltages, it is especially important to know the SOA in advance before the devices are put in test.

GaAs-based heterojunction bipolar transistors (HBTs) are widely used for power amplification applications in today's wireless communication systems. This technology offers high power density, high efficiency, and high linearity. But the increasing demand for high performance puts a stringent requirement for the device ruggedness [1]–[7]. A clear understanding of the devices' SOAs and an accurate way to characterize them are extremely important.

For Si bipolar junction transistors (BJTs) and Si/Ge HBTs, there have been quite a few studies on their SOAs both experimentally and theoretically [8]–[13]. But for GaAs-based HBTs, the studies on SOAs are relatively fewer. It is known that both thermal effect and impact ionization are important factors that can cause device failure and limit the SOAs. Self-heating causes semiconductor's energy bandgap to shrink creating an electro-thermal feedback and eventually the current runs away. Impact ionization happens in the collector when the electric field is high. The minority carriers generated in the collector can back inject to the base and that also causes a positive feedback for the transistor action inducing more current to flow through the transistor.

Compared with Si BJTs, GaAs-based HBTs are more sensitive to the failure mechanisms mentioned above. First of all, the thermal conductivity of GaAs is much lower than that of Si and that makes the GaAs devices more prone to the self-heating effect. Second, the current density used for GaAs HBTs is usually much higher than that used for Si-based transistors and the collectors of GaAs HBTs are usually very lightly doped. So, the Kirk effect can happen more easily. This will cause the breakdown voltage to drop drastically as the collector current increases. This Kirk effect-induced breakdown voltage reduction can seriously impact the SOA of the device. While the impact of self-heating and the effect of electro-thermal feedback on GaAs HBTs' instability have been well known [14], the role of the Kirk effect on breakdown and devices' SOA is rarely studied [7].

Because of the difficulty in measurement, GaAs HBTs SOAs are rarely measured in detail. Since each data point on an SOA boundary requires a device (to be operated to failure), the data points are usually scarce and it is difficult to perform the theoretical analysis based on the limited data points.

We have recently carried out an extensive study on InGaP/GaAs HBTs produced by TriQuint. A large quantity of identical devices was tested. The SOAs were clearly determined experimentally and the measured curves provided us a good base for theoretical analysis and enabled us to unambiguously identify the failure mechanisms at different operating conditions. For the first time, we are able to capture all the features of device characteristics at extreme conditions and at failure points theoretically and match with the experimental results. Hidden unstable points or secondary SOA boundaries have been discovered, and they explain the discrepancy between the SOAs determined by constant V_{be} inputs and constant I_b inputs. As hundreds of millions of InGaAs/GaAs HBTs are being used in today's cell phones and mobile communication systems, the ruggedness of these devices become extremely important. The results presented

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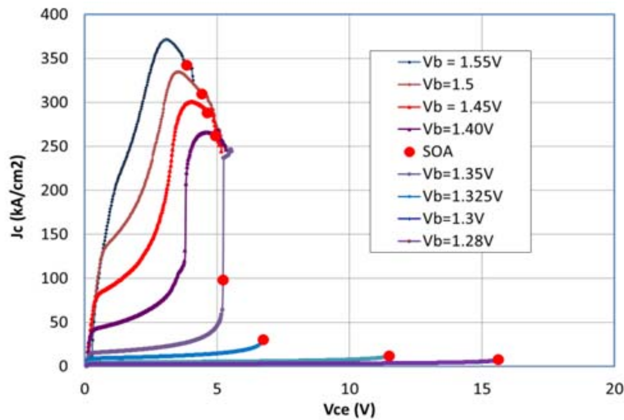

Fig. 1. SOA measurement with constant V_b inputs. The dots indicate the failure points.

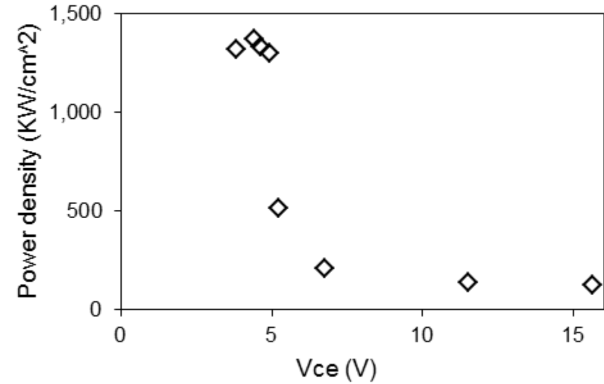

Fig. 2. Power density at failure points along the SOA boundary.

here not only explain the various mechanisms that influence the device failure, but also provide guidelines for device operation and device design.

II. Device Description and Measured Result

The NPN InGaP/GaAs HBTs used in this paper were from one of TriQuint standard HBT products [15]. The devices had a two layer collector design for improved ruggedness [7]. The resulting BV_{cbo} was ~23 V and BV_{ceo} ~ 12 V. The saturated current gain was ~100. The results presented here were obtained from devices with a two emitter finger design with a shared base in the middle. Each finger had a size of 2×6 μm^2. Devices with other dimensions and layouts have also been measured and results can be found in [4].

The SOA was measured at dc. A constant base voltage was applied to the device while the collector voltage was swept from 0 V until it failed. As described in [7], this (with constant V_b inputs) is the correct way to measure SOAs. A total of eight devices were measured with each biased at different base voltages from 1.28 to 1.55 V. Fig. 1 shows the measured I–V curves with the dot at the end of each curve indicating the failure point. The devices had no ballasting resistors either internally or externally. At $V_{be} = 1.55$ V, a very high peak current density of ~370 KA/cm^2 was obtained, but it failed at $V_{ce} = 3.9$ V. At higher collector voltages, the devices failed at much lower currents. The SOA is the region bounded by the dots and the line connecting the dots is the SOA boundary.

Two distinct regions are clearly seen in the SOA boundary. One is at high currents and low voltages and the other at low currents and high voltages. The transition between the two occurred at V_{be} ~ 1.35 V and a collector voltage of ~5 V. If we plot the power density at failure points (Fig. 2), we can see these two regions even more clearly. At low voltages, the power density can reach more than 1.4 MW per unit (1 cm^2) emitter finger area. At high voltages, the power density, the devices can sustain, is much lower. At $V_{ce} = 15$ V, the power density was ~125 KW/cm^2. We need to keep in mind that the BV_{ceo} of this device is ~12 V and there are no ballasting resistors. So with a voltage above BV_{ceo}, a bare device without ballasting resistors can survive a power density above 100 KW/cm^2 is quite remarkable. The I–V characteristics before failure in these two regions are very different. At low voltages and high currents, the current goes up quickly with V_{ce}, reaches a maximum and then comes down before it fails. At low currents and high voltages, however, the current usually bends up before it fails. The reason for this phenomenon will be discussed in Section III when we present the theoretical analysis.

The SOA shown in Fig. 1 was measured in dc. The SOA of the device under RF operation will be much larger [5]. As we have discussed previously [7], the absence of temperature fluctuation due to self-heating in each RF cycle will greatly improve the SOA. So the SOA shown here represents the worst case scenario. With the presence of self-heating, many temperature-dependent phenomena are important for the SOA determination. So, the dc SOAs contain a lot more information and physics than the RF SOAs and give us a good opportunity to investigate the various mechanisms that cause device failure.

We have also measured the device characteristics up to the failure points with constant base current inputs. Although the measured result may not reflect the true SOA because the devices can fail earlier due to the way that the devices are measured (sweeping V_{ce} and monitoring I_c), the failure points should fall on the SOA boundary if the I–V curves are able to reach that far. Fig. 3 shows the measured results for devices operated at different base currents. The negative slopes of the I–V curves at high base currents indicate that the devices were severely self-heated. A close inspection of the curves shows that the devices fail suddenly without the currents being bent up or down. So the failure was not caused by the I–V (bending backward) and measurement. It should be caused by the I–V curve hitting the SOA boundary. But if we compare Fig. 3 with Fig. 1, we can see that the failure points determined by the constant I_b measurements are beyond the SOA boundary. This is a very puzzling phenomenon, which we will explain in Section III when we look more closely at the physics of SOAs.

III. Theoretical Analysis of SOAs

HBTs, being a bipolar junction device, are very sensitive to temperature and prone to the adverse effects caused by the feedback of minority carriers in the presence of junction

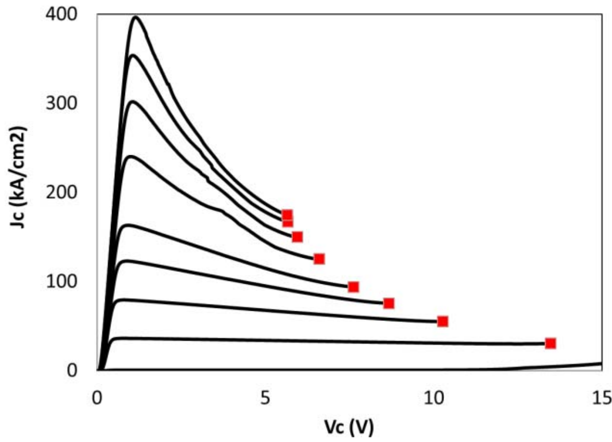

Fig. 3. I–V curves measured with constant I_b inputs. The devices were measured up to the failure points.

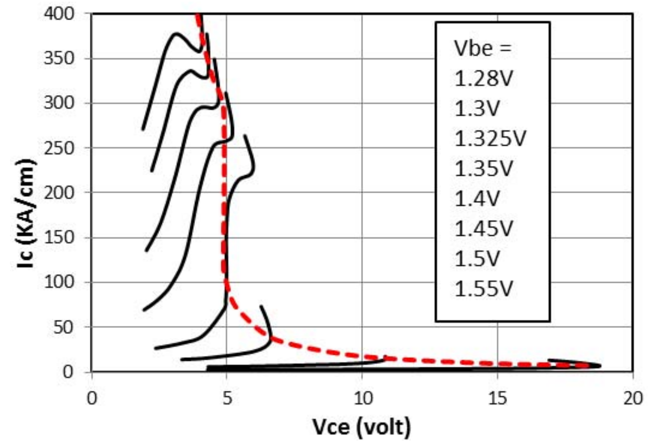

Fig. 5. Calculated I–V curves at different V_b inputs. The dashed line connecting all the bending over points is the SOA boundary. This figure should be compared with the measured data shown in Fig. 1.

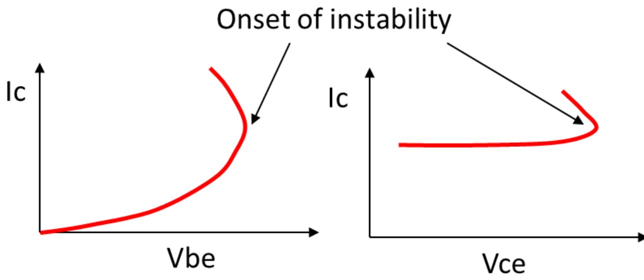

Fig. 4. Device I–V showing the onset of instability in the I_c–V_{be} and I_c–V_{ce} planes.

breakdown. The equation that governs the collector current when the devices are subject to self-heating and impact ionization can be expressed by [7], [14]

$$I_c = \alpha M I_0 \exp\left(\frac{q}{kT}(V_{\text{be}} - R_e I_e - R_b I_b + R_{\text{th}} \varphi I_c V_c)\right) \quad (1)$$

where R_{th} is the thermal resistance, φ is the thermal-electrical feedback coefficient, α is the common base current gain, and M is the multiplication factor. All other symbols have their normal meaning. The last term in the exponent represents the positive feedback from the self-heating effect. The resistive voltage drops in the emitter and the base act to suppress the feedback. When the electric field in the collector is high enough, impact ionization happens. The holes generated in the collector back inject to the base and cause the base current to drop and, in some cases, even to reverse the sign of the base current [7], [16], [17]. We can see from the equation, this also acts as a positive feedback and causes more current to be injected from the emitter. This effect gets worse when there is Kirk effect. At high currents, when the base pushes out and the high field region moves to the collector/subcollector junction, the breakdown voltage can be greatly reduced. The reduction of the breakdown voltage will aggravate the positive feedback due to impact ionization and reduce the SOA.

The result of the effects mentioned above gives rise to device instability, which is shown in Fig. 4. If we plot the device I–V on the I_c–V_{be} plane, the I–V curve at certain V_{ce} bias will bend over at a critical base voltage. For the same reason, if we plot the device I–V on the I_c–V_{ce} plane for certain V_{be} bias, the curve will also bend over at certain critical voltage. When the device reaches the bend over point, it becomes unstable because it can go into two paths (two solutions), one with a high current and the other with a low current. In cases of multiple finger transistors, multiple solutions result and the currents of some fingers can easily run out of control. Even for single finger transistors, any nonuniformity in the material can result in some hot spot causing device failure.

We have developed a way to theoretically solve the I–V relations under various conditions and search for the unstable points. Both self-heating and impact ionization were taken into consideration. The detail of the calculation can be found in [7]. To analyze the devices studied here, we first calculate the breakdown voltage $V_{\text{br}}(I)$ at various current injection levels to take into account the charge compensation of the injected carriers in the collector's space charge region and the Kirk effect. We then use the formula

$$M = \frac{1}{1 - \left(\frac{V_{\text{bc}}}{V_{\text{br}}(I)}\right)^n} \quad (2)$$

to obtain the multiplication factor. The thermal resistance and the current gain were taken as functions of power consumption. It should be mentioned that although the equations used in calculation are pretty simple, the physical picture they represent is clear. In contrast to complex numerical calculations, this paper requires very few parameters and no unphysical fitting parameter was used. As can be seen in the following, all the figures were generated through this calculation procedure and the results captured all the features observed experimentally with very good agreement.

Fig. 5 shows the calculated I–V curves for the same bias condition as that used in measurement (Fig. 1). The calculated curves capture all the features of the measured I–Vs and a very close agreement was obtained. Different from the measured curves, which stop at the failure points, the calculated curves are able to show the I–Vs beyond the

failure points. Clearly the devices fail when the I–V curves bends over.

At high currents and low voltages, the devices fail at points after the currents reach a maximum. The current first rises quickly with the collector voltage because of self-heating. But at the same time, the current gain drops (because of self-heating and the Kirk effect), which means a lot of current injected from the emitter has to recombine with the base current and cannot reach the collector. This causes the collector current to drop and works against the self-heating effect. Eventually, the current, after reaching a maximum, has to come down because of the severe drop in the current gain and the base transport factor. Then, the failure mechanism kicks in due to the Kirk effect-induced breakdown and the curve bends up and backward. The device fails at the bend-over point. At low currents and high voltages, the behavior of the I–V curves is very different. The currents do not rise very much and they do not go up and then come down before failure. Instead, the current continues to go up to the bend-over (failure) points. If we connect all the failure points together, we obtain the SOA boundary shown as the red dash line in Fig. 5. Like the measured result, two distinct regions are clearly seen. At low voltages and high currents, the failure is controlled by the impact ionization because of the Kirk effect-induced breakdown. At low currents and high voltages, the failure is governed by the self-heating effect. It may sounds against intuition but it becomes clear if we look at the thermal SOA curve, which can be easily derived from (1) assuming $\alpha = 1$ and $M = 1$ [14]

$$I_c = \frac{kT/q}{R_{\text{th}}\varphi V_{\text{ce}} - \left(R_e + \frac{R_b}{\beta}\right)}. \tag{3}$$

It is clear from this equation that there is no solution when the collector voltage is below $V_{ce} = (R_e + R_b/\beta)/R_{th}\varphi$, where the collector current goes to infinity. In other words, the thermal effect cannot cause device failure when V_{ce} is below this critical value. In our case, this voltage happens at ~5 V. Below 5 V, the self-heating is not in control of the device failure. On the other hand, when V_{ce} is higher than this value, the current goes down quickly. At high collector voltages, the currents at failure actually can be very low. A clear evidence of what stated here is shown in Fig. 6, where the multiplication factor at failure is shown as a function of collector voltage. We can see clearly that at low currents and high voltages, $M \approx 1$. But when $V_c < 5$ V, M suddenly jumps higher. So the dominant failure mechanism at low voltages is the (Kirk effect induced) breakdown effect, while at high voltages it switches to the thermal effect.

In all of Figs. 1, 5, and 6, we see a transition region at $V_{ce} \approx 5$ V. It happens at a V_{be} bias of ~1.35 V. This is the point that the denominator of (3) goes to zero. In other words, the thermal effect no longer causes device failure and the breakdown effect takes over. If we look carefully at the I–V curve of $V_{\text{be}} = 1.35$ V of Fig. 5, we actually see three points with the slope goes to infinite. In other words, all these three points can cause devices to fail. Normally in constant V_{be} measurement, we always encounter the one with the lowest

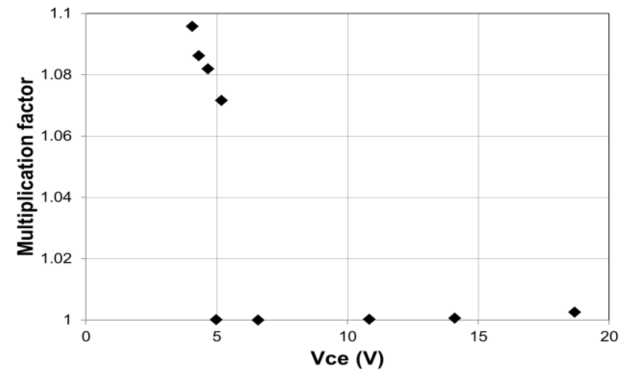

Fig. 6. Multiplication factor at the failure points along the SOA boundary.

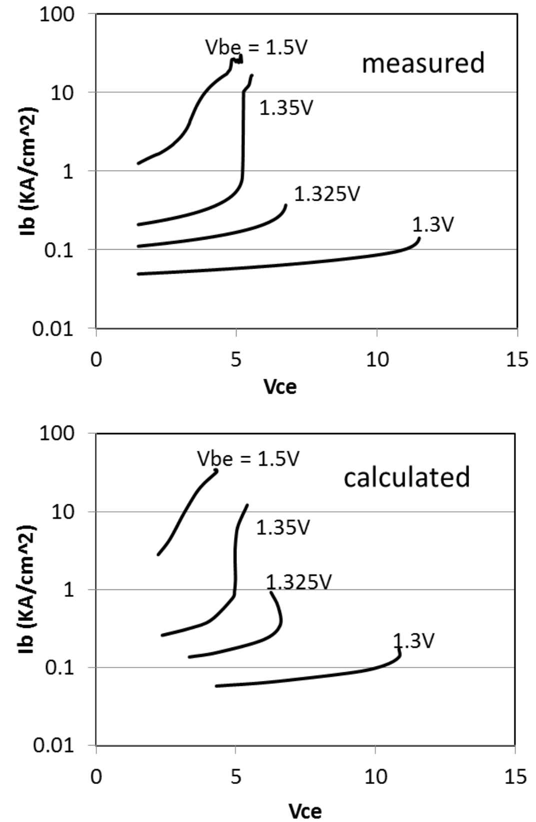

Fig. 7. Measured (top) and calculated (bottom) I_b versus V_{ce} at different base voltages.

current first, so we can never see the upper two unstable points. While it is reasonable to define the SOA boundary in a more conservative way by choosing the lowest current one, the upper two unstable points are also real and can cause device failure if the device ever goes there. We will have more detailed discussion on the upper unstable points later in this paper.

We have also compared the calculated base currents of the curves shown in Fig. 5 with those measured at the same bias conditions and the results are shown in Fig. 7. Again excellent agreement was obtained. We notice that the behavior of the base current also undergoes a transition at $V_{\text{ce}} = 5$ V

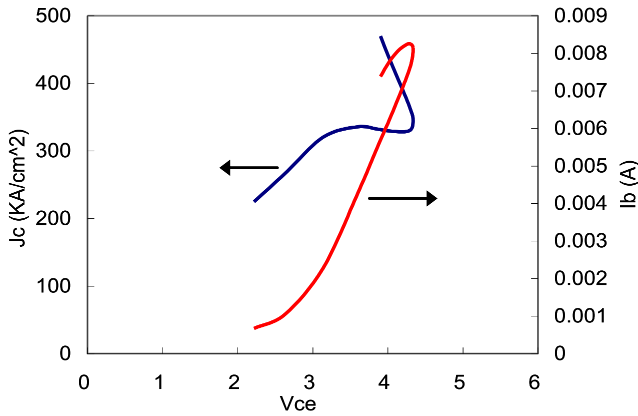

Fig. 8. Collector current and the base current versus collector voltage at $V_{\rm be} = 1.5$ V. The base current starts to bend down when the collector current snaps back at the failure point. It is a clear indication that the breakdown effect is the dominant factor for device failure.

and $V_{\rm be} = 1.35$ V. When $V_{\rm be}$ is <1.35 V, the base current does not change very much before the device fails. But when $V_{\rm be}$ is above 1.35 V, the base current rises sharply until the device fails. The reason for such phenomenon is the same as we described earlier. At high $V_{\rm be}$ (or high currents and low collector voltages), self-heating is not in control, so the base current can go very high as the Kirk effect takes place and the temperature rises. However, as the breakdown effect kicks in at the failure point, we should see a reduction of the base current as the impact ionized holes back inject to the base. The reason that we do not see it in Fig. 7 is because the current is shown in log scale and the calculation was stopped right after when the device fails. Fig. 8 shows the base current and the collector current at $V_{\rm be} = 1.5$ V in a linear scale and the calculation was extended beyond the failure point. It is very clear that the base current starts to bend down close to the failure point. It will eventually go to negative (base current reversal) if we continue the calculation. When $V_{\rm be}$ is below 1.35 V, however, the base current continues to rise after failure and does not go down. So this is also a clear evidence that at high currents and low voltages, the dominant mechanism for device failure is the breakdown effect and at high voltages and low currents, the dominant mechanism is the thermal effect.

For Si-based bipolar transistors, different device failure mechanisms at different operating regions have been discussed in [10] and [11], but the observed result is contrary to what we observed here. In those Si-based devices, the breakdown effect was the controlling mechanism for SOA at low currents and high voltages while the thermal effect was the controlling mechanism at high currents and low voltages. This could be caused by: 1) at high voltages and low currents, Si has a better thermal conductivity, so the thermally controlled SOA boundary is beyond the breakdown voltage and 2) at low voltages and high currents, Si transistors do not have Kirk effect because of lower current densities used and higher collector doping compared with those for GaAs HBTs. As a result, the breakdown controlled SOA lies above the thermally controlled SOA. We have to bear in mind that the Si transistors are very different from the GaAs-based HBTs in structures and in operating conditions. So it is not surprising that the results

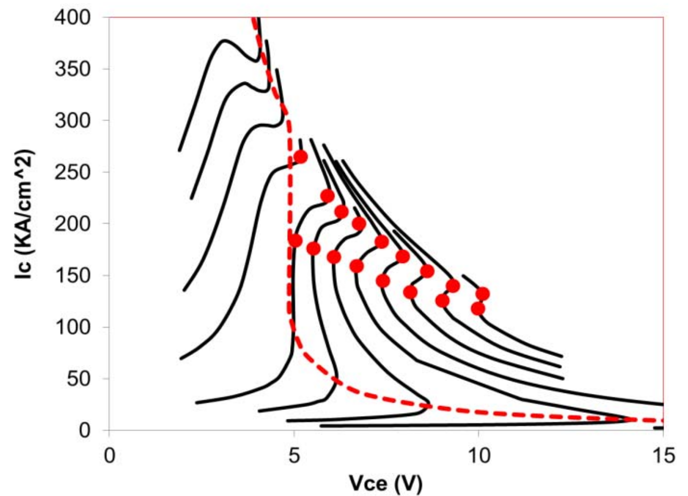

Fig. 9. Calculated I–V curves with constant V_b inputs. The curves include all the unstable points. The dashed line is the SOA boundary while the dots mark the upper unstable points.

observed for these two different kinds of technologies are very different. GaAs HBTs are usually operated at a much higher current density than the Si devices. So the Kirk effect-induced breakdown can happen at voltages lower than the thermally defined SOA voltages at high currents.

If we extend the calculation beyond the failure points at low currents and high voltages, we can actually see other unstable points. The complete calculated I–V curves (with constant $V_{\rm be}$ inputs) showing all the unstable points are shown in Fig. 9. We can see how the I–V curve evolves as $V_{\rm be}$ increases. At low $V_{\rm be}$s, the I–V curves snap back twice, resulting in three unstable points, where the slopes of the I–V curves are infinite. The upper two are marked by dots and the lowest one lies on the SOA line. When $V_{\rm be}$ is increased above 1.35 V, the first and the second unstable points disappear and only the top one remains. So we can see that the unstable points at high currents continue beyond the transition region at $V_{\rm ce} = 5$ V. If we plot the base currents together with the collector currents, we can see more clearly the difference between the two snapback points. Fig. 10 shows those curves at four different $V_{\rm be}$ bias conditions 1.3, 1.325, 1.4, and 1.5 V. For $V_{\rm be} = 1.4$ and 1.5 V, as mentioned before, the base currents start to bend down at the failure points because of the breakdown effect. For $V_{\rm be} = 1.3$ and 1.325 V, where there are two snapbacks, the base current continues to go up after the first snapback until it reaches the second snapback point (or the third unstable point). The base current bends down at this point. So these upper snapback points are also due to the breakdown effect.

But because of the appearance of the unstable points at low currents due to self-heating, these upper unstable points are outside of the normally defined SOA. While the upper unstable point in the S-shaped I–V for $V_{\rm be} < 1.35$ V is due to the breakdown effect and the lower unstable point is caused by self-heating, the middle one is simply caused by the transition between the two. An interesting question is whether we will be able to see the upper unstable points predicted by the theory but hidden beyond the SOA.

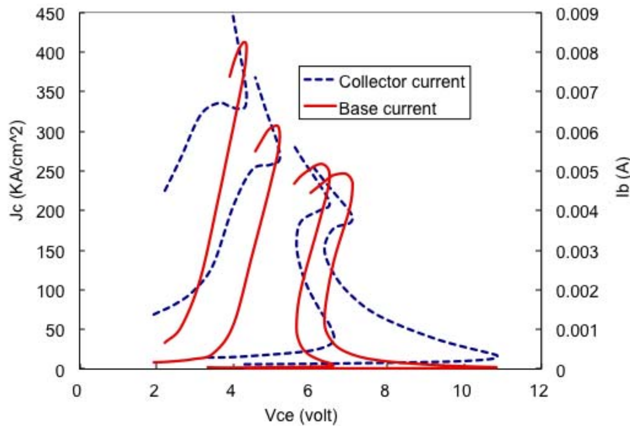

Fig. 10. Collector currents and base currents as functions of collector voltages at $V_{\rm be} = 1.3$ V, 1.325 V, 1.4 V and 1.5 V. It can be seem that at the upper snapback points at high voltages, the base currents also bend down indicating that they are caused by the breakdown effect.

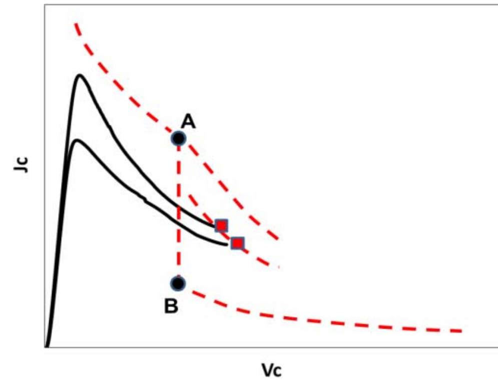

Fig. 11. Device I–V in constant I_b mode showing how the curves go through the SOA gap between A and B. The devices fail when the I–V curves hit the upper unstable lines.

We notice that the high voltage SOA curve, which is defined by the lower unstable points, stops at $V_{\rm ce} = 5$ V and then continues at high currents and low voltages with the SOA curve determined by the breakdown effect. A large gap or discontinuity exists at the transition point at $V_{\rm ce} = 5$ V. The vertical line connecting the two branches of SOA at the transition point actually is not part of the SOA boundary. There are no failure points along this line. In other words, the device will not fail if it touches this line. It is possible for certain operation conditions, the device can pass this line and go into the region above the SOA boundary at high voltages. It, however, does not mean that the device will not fail. In this situation, the device failure is controlled by the upper unstable points above the lower branch of the SOA curve shown in Fig. 9. This situation can be illustrated in Fig. 11 and it explains why the devices fail beyond the (normally considered) SOA boundary when they were measured in the constant I_b mode shown in Fig. 3. Because of severe self-heating, the I–V curves bend down as the collector voltage increases. Although the peak current can reach very high at high base currents, the large negative output conductance causes the I–V curve to have enough bending to avoid the breakdown limited SOA (upper branch of the SOA) and the curve goes through the gap between the upper branch and the lower branch of the SOA. But once it passes this line (between A and B in Fig. 11), the device failure will be controlled by the unstable lines defined by the upper unstable points mentioned above. When the I–V curves hit those upper lines, the devices fail right there. We will not see the curves bending up or down when they approach the failure points because the failure has nothing to do with the I–V curves themselves.

The modeling of the dc SOA is not trivial because both the thermal effect and the breakdown effect need to be considered. While it is relatively easy to fit the experimentally measured SOA at low voltages/high currents (upper branch) and high voltages/low currents (lower branch), it is difficult to obtain accurate upper unstable lines hidden beyond the SOA. The temperature dependences of the current gain and the thermal resistance as well as the current-dependent breakdown all have strong influence on the positions of those upper unstable points. Although the failure points measured in Fig. 3 does not exactly lie along the second or the third failure curves shown in Fig. 9, the qualitative agreement does show the transition behavior and the gap between the two branches of the SOA boundary. We have to keep in mind, however, the devices that we measured did not have any ballasting resistors and were measured in dc. In real applications, HBTs are usually designed with some serially connected ballasting resistors. In such case, the transition point, as shown in (3), will move to higher voltages and the gap will become smaller or even disappear. Besides, during RF operation, self-heating does not cause device failure by itself and the SOA in the high voltage part will be greatly widened. In such case, there is also no transition and gap in the SOA boundary.

The multiple snapback behavior in the I–V curves has also been reported for Si BJTs when impact ionization was considered [10]. But, different from ours, the second snapback points were always hidden beyond the thermal SOA. So those points were not observable.

IV. Conclusion

SOAs of InGaP/GaAs HBTs were studied in detail both experimentally and theoretically. The failure points were measured at different bias conditions and with both constant V_b and constant I_b modes. The devices had no ballasting resistors and were measured in dc. So the measured data reveal the intrinsic SOA characteristics of bare (unprotected) InGaP/GaAs HBTs under the influence of both self-heating and breakdown effect. The SOA boundary had two distinct regions. At low voltages and high currents, the current usually drops before the device fails, while at high voltages and low currents, the device current bends up before it fails. There is a large gap (in current) between the two branches of the SOA boundary. Using theoretical modeling, we were able to identify the failure mechanisms at different regions or bias conditions and explain all the features in the measured characteristics. The calculated result agrees very well with the measured result. At high voltages, we also found, through theoretical analysis, there are other unstable points above the

normal SOA boundary in the I_c–V_{ce} plane. The existence of the gap between the two SOA branches allows the devices to go beyond the SOA boundary when measured in constant I_b conditions. In such case, the device failure is determined by the upper unstable points hidden beyond the normally considered SOA boundary. This paper clarified the complex behaviors of the SOA of HBTs, which are prone to self-heating, impact ionization, Kirk effect induced early breakdown, and the associated feedback phenomena. The theoretical analysis provides a good guideline for the design of future more rugged HBTs.

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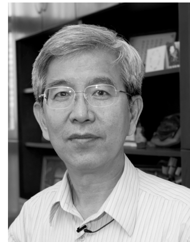

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