Characteristic Evolution from Rectifier Schottky Diode to Resistive-Switching Memory With Al-Doped Zinc Tin Oxide Film

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***Abstract*— We demonstrate a metal sandwiched Al-doped zinc tin oxide (AZTO) thin-film device to exhibit a characteristic evolution process from Schottky junction diode to resistive-switching random access memory (RRAM) applications. The proposed TiN/Ti/AZTO/Pt device can initially show good rectifying characteristics and high forward-bias current for Schottky diodes. After applying with an electrically triggered forming process, the transition of electrical behavior occurs and evolves from the diode to RRAM characteristics. The RRAM device exhibits the coexistence of bipolar and unipolar resistive-switching modes through the positive-bias forming and reversed-bias forming process, respectively. In addition, the RRAM device with bipolar mode can perform the functionality of multilevel cell storage, while the one with unipolar mode shows stable resistive-switching performance. Furthermore, one-transistor and one-resistor (1T1R) architecture with an RRAM cell connected with a thin-film transistor (TFT) device is developed in this paper. The TFT device using AZTO film as an active channel layer performs good electrical characteristics for a driver in the 1T1R operation scheme. The integration of AZTO-based electronic devices has great potential for increasing the application diversity of metal oxide AZTO thin film as well as the flexibility of circuit design in the emerging optoelectronic technologies.**

***Index Terms*— Al-doped zinc tin oxide (AZTO), one transistor and one resistor (1T1R), resistive-switching random access memory (RRAM), Schottky junction diode, thin-film transistor (TFT).**

I. INTRODUCTION

IN RECENT years, metal oxide-based electronic materials have attracted popular attentions in both research and industrial communities, including the applications for capacitor dielectric, oxide thin-film diode, oxide-based resistive-switching random access memory (RRAM), and thin-film transistor (TFT) technologies [1], [2]. In addition, transparent amorphous oxide semiconductors (TAOSs) are highly received candidates for large-sized liquid-crystal displays (LCDs) and active-matrix organic light-emitting diode displays (AMOLEDs). It owns lots of desirable features, such as the high optical transparency, low processing temperature, and high electron mobility, even when it is deposited at room temperature without any thermal annealing processes [3], [4]. Among several TAOS materials, the amorphous aluminum (Al)-doped zinc (Zn) tin (Sn) oxide (a-AZTO) is receiving great interests due to its low material cost, and its components free of indium (In) and gallium (Ga), which are rare elements on the earth [5]–[7]. In this paper, we demonstrate the diversity of a-AZTO thin film for optoelectronics device applications by studying the Schottky junction diode, RRAM, and TFT devices. With a given electrical trigger, the characteristics of Schottky diode can be obviously switched to the RRAM behavior. The RRAM devices can be for use in next-generation nonvolatile memory technologies owing to its simple device structure, low power consumption, favorable scalability, and fast switching [1], [2]. Furthermore, one-TFT and one-resistor (1T1R) configuration is demonstrated for low-power and system-on-panel applications in active-matrix flat-panel displays.

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II. EXPERIMENT

A simple metal/insulator/metal structure, which consisting of titanium nitride (TiN)/titanium (Ti)/AZTO/platinum (Pt) structures, was fabricated at room temperature. First, titanium oxide (TiO_2) was deposited to be a buffer layer by electron-gun (e-gun) evaporation process for enhancing the adhesion to a silicon substrate. Then, a 50-nm-thick Pt acting as a bottom electrode was also formed by the e-gun evaporation. It was followed that a 50-nm-thick AZTO resistive-switching layer was deposited by radio-frequency (RF) magnetron sputtering with an AZTO ceramic plate target consisted of ZnO, SnO_2, and Al_2O_3 (67:30:3 mol%). The Ar gas flow rate was set to 10 sccm, while the sputtering pressure and power were 3 mtorr and 80 W, respectively. Finally, a 10-nm-thick Ti and 20-nm-thick TiN bilayer were deposited to form bilayer top electrodes [8], [9]. The insertion of Ti layer between TiN and AZTO will be beneficial for resistive-switching performance [10]. With the oxygen-getting ability of Ti layer, the resultant formation of TiO_x layer would cause extra oxygen vacancies to be within the AZTO matrix. It thereby achieved the stable resistance switching characteristics for the AZTO RRAM device. The size of the memory cell was patterned by shadow mask with a diameter of 0.2–0.6 mm. TFT devices with a bottom-gate inverted staggered structure were also fabricated in this paper. At first, a layer of 100-nm-thick silicon dioxide was thermally grown on n-type

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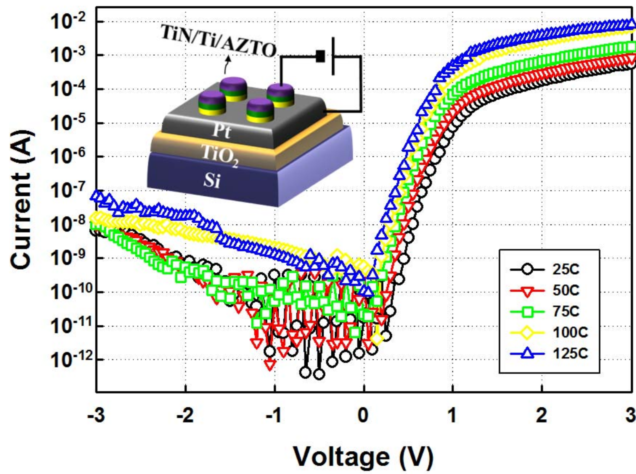

Fig. 1. Temperature dependence of I–V characteristics for the Schottky diode with TiN/Ti/AZTO/Pt device structure.

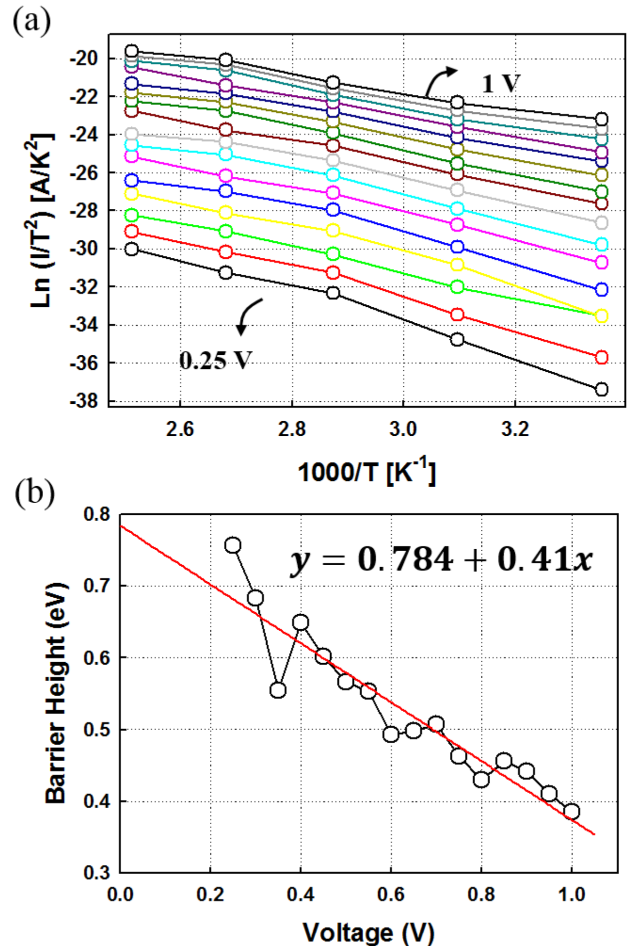

Fig. 2. (a) Richardson ln(I/T^2) versus 1000/T plot for the device TiN/Ti/AZTO/Pt Schottky diode, showing thermionic emission behavior. (b) Extracted values of Schottky barrier heights as a function of applied voltages.

silicon wafers. The 25-nm-thick a-AZTO films were deposited by RF sputtering system. The deposition condition of a-AZTO layer was the same as the RRAM fabrication process except the oxygen flow rate was set to 2 sccm. A layer of 100-nm-thick tin oxide (ITO) film was deposited subsequently by RF sputtering, and patterned through a shadow mask for the formation of source and drain (S/D) electrodes. The channel width and length were 2000 and 200 μm, respectively. The a-AZTO TFT devices were thermally annealed at 450 °C for 1 h in a thermal furnace under the nitrogen atmosphere. As for the manufacture of 1T1R configuration, the RRAM device was formed directly on S/D electrodes of TFT device through a 5-nm-thick Ti buffer layer for enhancing the adhesion between Pt bottom electrode and ITO S/D electrode. All electrical measurements were conducted by the Keithley 4200 semiconductor characterization analyzer.

III. Results and Discussion

Fig. 1 shows the temperature dependence of current–voltage (I–V) characteristics of the TiN/Ti/AZTO/Pt device, exhibiting temperature stability from room temperature to 125 °C. A good rectifying characteristic was observed with a rectification ratio $I_{\mathrm{ON/OFF}}$ of 10^6 at ± 1 V, and also showing high forward-bias current about 0.5 mA at 3 V. The current transport through a Schottky junction diode can be described by thermionic emission of majority carriers over the junction barrier [11]

$$I = AA^*T^2 \exp\left(\frac{-q(\phi_B - \sqrt{qV/4\pi\varepsilon d})}{kT}\right) \tag{1}$$

where A is the area of the diode, q is the elementary electric charge, ε is the dielectric permittivity, d is the dielectric thickness, k is Boltzmann's constant, T is the absolute temperature, and A^* is the effective Richardson constant. Fig. 2 plots the relationship of ln(I/T^2) versus 1000/T for the TiN/Ti/AZTO/Pt device. A good linear fit explains Schottky emission-like conduction mechanism, which is induced by the thermionic effect caused by electron transport across the potential energy barrier via field-assisted lowering at the interface between metal electrode and AZTO film. In this paper, the energy barrier height of 0.78 eV was extracted and similar to the case of Pt/InGaZnO Schottky barrier diode [12], [13].

The TiN/Ti/AZTO/Pt Schottky diode device is capable of being switched from the rectifying mode to the resistive-switching characteristics by applying positive dc sweeping voltages on the TiN/Ti top electrode, as shown in Fig. 3. A typical bipolar resistance I–V characteristic of the AZTO RRAM device is exhibited under dc sweeping mode at room temperature. In the beginning, the a-AZTO layer of RRAM device is gradually activated to form a conductive path, called the forming process. A sudden increase in current occurs at forming voltage, and the cell was transformed from high-resistance state (HRS) to low-resistance state (LRS). After sweeping the bias over the reset voltage around -1.8 V, an abrupt decrease in current was observed where the memory cell switches from LRS to HRS, called as reset process. Inversely, the cell turns back to LRS while applying a positive bias over the set voltage ($\sim$1.1 V), and a compliance current (I_{cc}) of 10 mA is assigned to prevent the permanent breakdown.

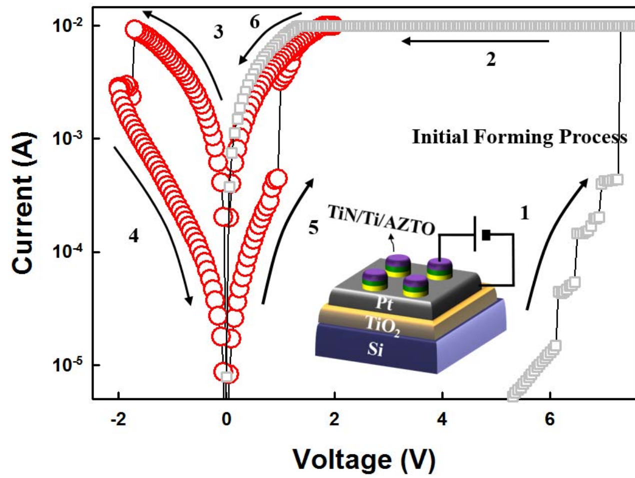

Fig. 3. Typical bipolar I–V curves of TiN/Ti/AZTO/Pt device with resistance-switching characteristics. The sequence of forming process (arrow number 1 and 2), reset process (arrow number 3 and 4), and set process (arrow number 5 and 6) was presented by voltage swept. Inset: schematic plot of resistive memory devices with titanium nitride (TiN)/titanium (Ti)/AZTO/platinum (Pt) structure.

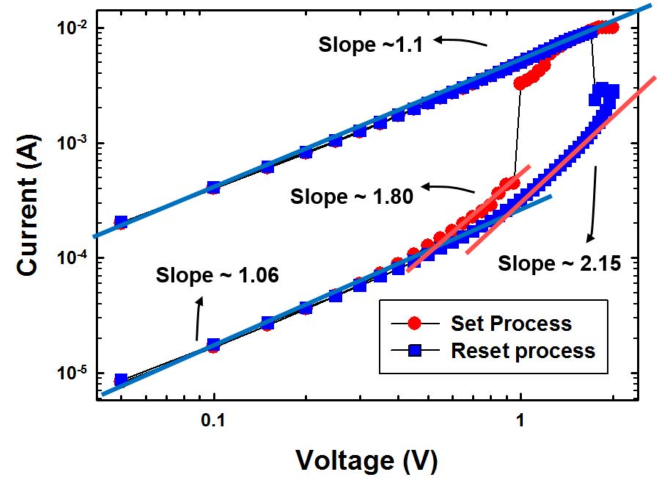

Fig. 4. Double logarithmic plot of I–V characteristics for TiN/Ti/AZTO/Pt RRAM device, showing the SCLC conduction dominant in the HRS, while ohmic-like behavior for the LRS.

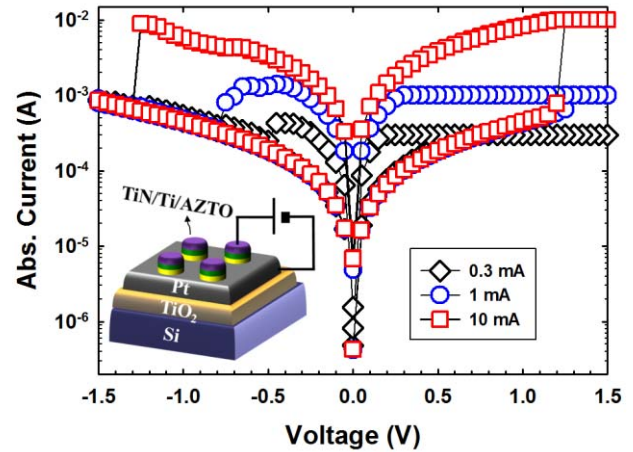

Fig. 5. Multilevel cell characteristics of TiN/Ti/AZTO/Pt RRAM device controlled by setting the compliance current to 0.3, 1, 10 mA, respectively. The ability of two-bit per cell is clearly exhibited and is potential for high-density memory applications.

In [7], oxygen vacancies have been examined to be initially existed in the pristine AZTO film. As a result, the resistive-switching phenomena can be attributed to the electrochemical reaction within the AZTO matrix during voltage sweep operation. A downward electric field can be generated to force O^{2-} ions to move into the Ti layer acting as an oxygen reservoir and then oxidize the anode, when a positive bias was applied to the TiN top electrode. Meanwhile, the oxygen vacancies drift or diffuse to the bottom electrode Pt, and are reduced at the cathode. The conduction path consisted of accumulated oxygen vacancies starts to grow from the cathode to the anode, and forms the conducting filaments. As a negative bias is applied to the top electrode, an upward electric field is generated and the reversed reduction–oxidation (REDOX) process occurred. The oxygen ions migrate back to the AZTO film and recombine with the oxygen vacancies. This causes the conducting filaments to be partially breached near Ti layer, and thereby making the resistance state of RRAM device switched from LRS to HRS. Because of the residual conducting filaments, the conductivity at HRS is higher than the one before the forming process. It is also the reason that the voltage of SET process less than the one of the forming processes ($V_{\mathrm{SET}} < V_{\mathrm{FORMIN}}$). The formation and rupture of the conducting filaments are mainly due to the REDOX process near the top electrode, so that the bipolar switching behavior is observed.

The mechanism of current transport for the AZTO RRAM device is explored through the analysis of I–V characteristics displayed with double-logarithmic scale, as shown in Fig. 4. Both set and reset process in LRS exhibit the linear dependence with a slope of 1.1 and indicated that ohmic-like behavior was dominant. The linear slope changes from 1.06 to 1.8 during the set process, and 2.15 to 1.06 during the reset process, when the transition from HRS to LRS and LRS to HRS, respectively. It also suggested that the mechanism of space charge limited current (SCLC) dominated the current transport in the a-AZTO RRAM device [14].

Furthermore, it is observed that the resistance states can be controlled by setting the compliance current properly in the set process, as shown in Fig. 5. Obviously, a lower resistance value of LRS could be reached when imposing a higher I_{cc} on the RRAM device. Four levels of states also can be clearly distinguished from the dependence of I_{cc} and resistance, as shown in Fig. 6(a). The smallest resistance ratio of the RRAM devices is around two, which will be promising for RRAM circuit design [15]. The effect of reset voltage (V_{RESET}) and maximum reset current ($I_{\mathrm{MAXIMUM,\,RESET}}$) with different values of I_{cc} also was shown in Fig. 6(b). Both the $I_{\mathrm{MAXIMUM,\,RESET}}$ and V_{RESET} decrease with the reduction of I_{cc}. These results demonstrated the promising application for multibit storage memory technology.

On the other hand, it is observed that a forming process in a reverse bias direction also can be occurred by applying

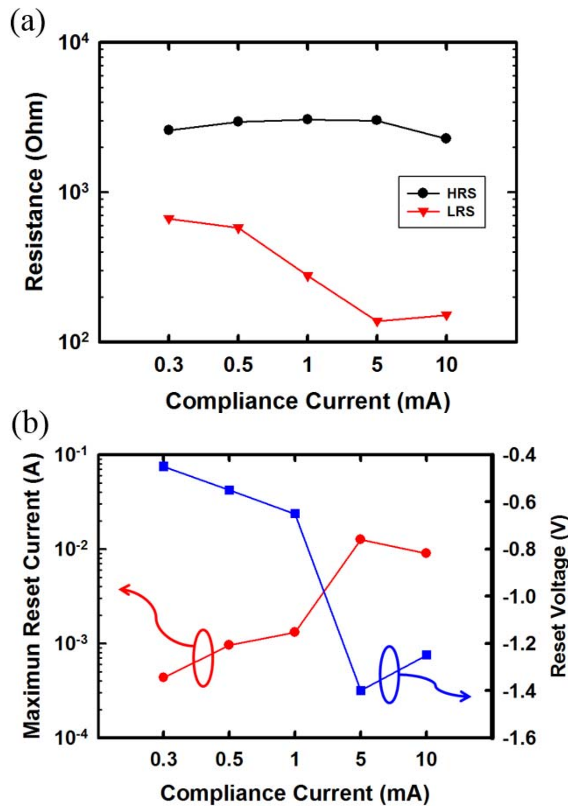

Fig. 6. (a) Dependence of compliance current (I_{cc}) on LRS value for the TiN/Ti/AZTO/Pt RRAM device. (b) Relationship between $I_{MAXIMUM, RESET}$ and V_{RESET}.

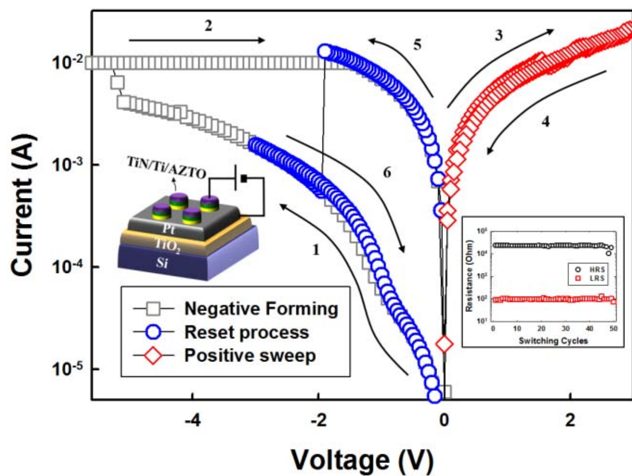

Fig. 7. Reverse forming process of TiN/Ti/AZTO/Pt RRAM device using negatively sweeping voltage bias (arrow number 1 and 2), failed reset process when we applied positive bias sweep on the top electrode (arrow number 3 and 4), and negative reset process (arrow number 5 and 6) showing a functionality of unipolar mode with stable resistive-switching cycles.

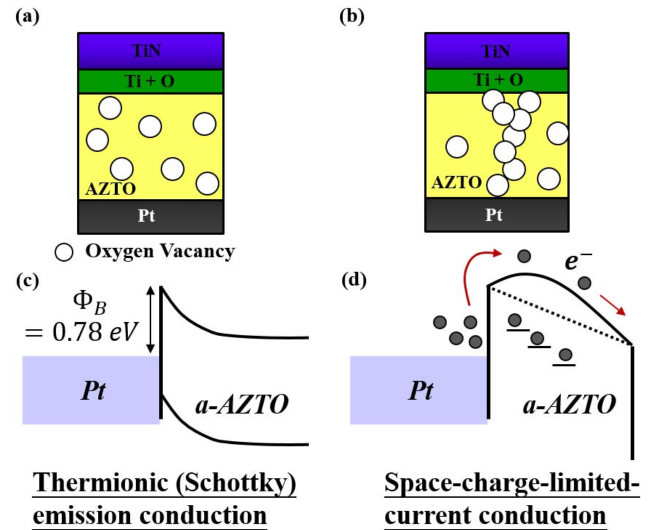

Fig. 8. Characteristic evolution from rectifier diode to resistive-switching memory. (a) Schematic description on the distribution of oxygen vacancies in TiN/Ti/AZTO/Pt device before the forming process. (b) Corresponding energy band diagram of (a). (c) Schematic diagram of TiN/Ti/AZTO/Pt after forming process. (d) Corresponding energy band diagram of (b).

negative voltage bias on the top electrode of AZTO RRAM, as shown in Fig. 7. In addition, applying a negative reset process with a negative bias sweeping, the RRAM cell can be switched from LRS to HRS. The set/reset operation under dc sweep mode can be achieved and the resistance ratio of HRS to LRS (R_{HRS}/R_{LRS}) is around 100 times at a reading voltage of 0.2 V, as well as it show a robust resistance state after continuous I–V sweep 50 cycles at least. These above results show that the proposed TiN/Ti/AZTO/Pt device possesses both Schottky diode and RRAM characteristics. With electrical triggering appropriately, the a-AZTO RRAM operated in unipolar mode has great potential to be connected with AZTO Schottky diode demonstrating the one-diode one-resistor configuration for high-density memory array applications [16], [17].

Finally, the model of the characteristic evolution process from Schottky junction diode to RRAM was proposed. Fig. 8 shows the schematic transition diagram and energy band diagram of the TiN/Ti/AZTO/Pt devices through a forming process. In the pristine state shown in Fig. 8(a), the device exhibits the rectifying behavior. The current transport mechanism is governed by the Schottky emission due to a high work function of Pt (∼5.4 eV), which forms a barrier height, as shown in Fig. 8(b), to the n-type AZTO layer. In Fig. 8(c), it shows that more oxygen vacancies in AZTO were produced to activate the resistance-switching characteristics after the forming process. More and more filaments are developed across the entire region of AZTO by the oxygen migration and Joule heating effects [18]. The filaments consisted of oxygen vacancies, which extending into the metal/oxide interfaces, would destroy the Schottky barriers. Therefore, the generated oxygen vacancy may contributed to the SCLC conduction behavior [Fig. 8(d)].

Another application of RRAM cells could be developed to be integrated with TFT devices for AMLCDs and AMOLEDs to achieve low-power and system-on-panel technology [7]–[9]. The TFT device with AZTO film as an active layer was also fabricated in this paper. The cross-sectional view of AZTO TFT device structure is shown schematically in the inset of Fig. 9. The transfer characteristics of AZTO TFTs measured at $V_{ds} = 10$ V are shown in Fig. 9. The saturation mobility (μ_{sat})

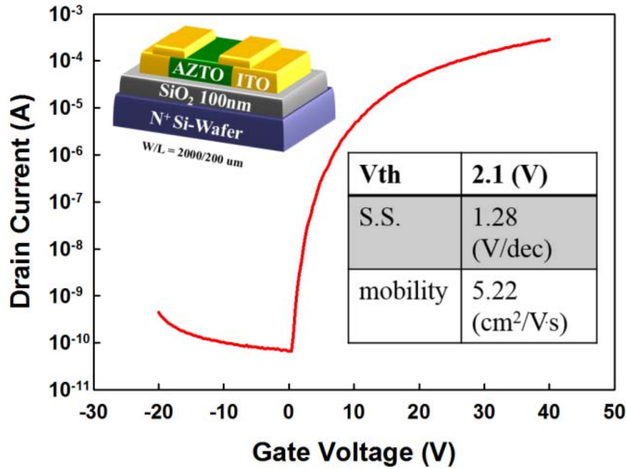

Fig. 9. Transfer characteristics of TFT device with a-AZTO as an active layer.

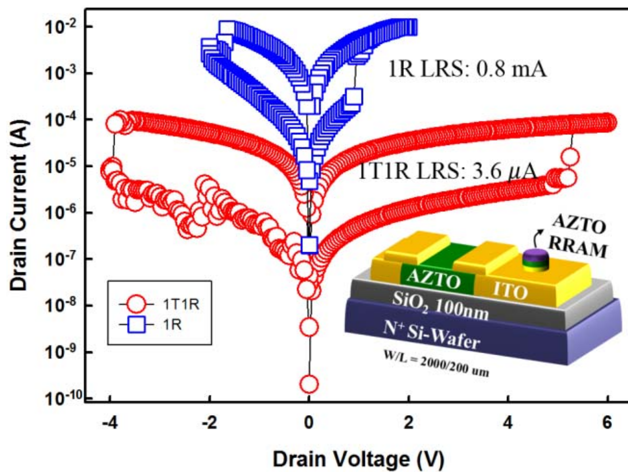

Fig. 10. Comparison of typical bipolar I–V curves for a single RRAM (1R) cell and 1T1R configuration with the a-AZTO TFT connected with RRAM device.

derived from the transconductance (g_m) maximum value method using the MOSFET drain current equation

$$I_{\rm ds} = \frac{1}{2}\mu_{\rm sat} C_{\rm ox} \frac{W}{L}(V_{\rm gs} - V_{\rm th})^2 \tag{2}$$

where W is the channel width, L is the channel length, and $C_{\rm ox}$ is the gate insulator capacitance per unit area. The threshold voltage ($V_{\rm th}$) was extracted from the voltage when normalize drain current ($\text{NI}_{\rm ds}$) at 10^{-8} A. The subthreshold swing (SS) was defined as the amount of gate voltage required to increase and decrease drain current by one order of magnitude. The device parameters including $V_{\rm th}$, SS, and saturation mobility were 2.1 V, 1.28 V/decade, and 5.22 cm^2/V s, respectively. The AZTO TFT connected with AZTO RRAM to form 1T1R architecture, shown in the inset of Fig. 10, is investigated as followed. Fig. 10 compares I–V characteristics of 1R and 1T1R structures. In 1T1R configuration, the set process was functioned by operating TFT with drain voltage ($V_{\rm ds}$) = 6 V sweep and gate voltage ($V_{\rm gs}$) = 30 V, whereas the reset process was at $V_{\rm ds}$ = −4 V sweep and $V_{\rm gs}$ = 30 V. The TFT device played a role of current limiter so that the significant decrease of current can be observed in the 1T1R configuration, while in 1R configuration, a maximum current level was enforced by setting a current compliance limit in the parametric analyzer to control the device under test. The response time for a typical analyzer was usually longer than the characteristic times of the forming process. Thus, it is easy to cause a current overshoot over the desired limit and results in a high required reset current and power consumption issues [19]. In contrast, the integration of TFT and RRAM to form a 1T1R configuration can effectively reduce the issue of overshoot current. The current at LRS is reduced from 0.8 mA to 3.6 μA at a reading voltage of 0.2 V, and thereby the LRS power consumption is significantly decreased from 0.16 mW to 0.72 μW.

IV. Conclusion

In summary, this paper has studied the AZTO-based electronic devices including diode, RRAM, and TFT. The performance of AZTO Schottky diode exhibited good rectification ratios of $I_{\rm ON/OFF} > 10^6$. With electrical triggering properly, the diode-like behavior can be transferred to the RRAM characteristics, which revealed the coexistence of both bipolar and unipolar resistive-switching behavior. The RRAM cell with the bipolar mode also behaved the characteristics of two bits per cell. Furthermore, the electrical performance of AZTO TFT device was studied, showing superior transfer characteristics with threshold voltage 2.1 V, saturation mobility 5.22 cm^2/V s, and SS 1.28 (V/decade). The integration of AZTO TFT and AZTO RRAM devices was finally completed to form 1T1R configuration with low power consumption of 0.72 μW. It is promising make the 1T1R possible for the applications of low-power active-matrix flat-panel displays.

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