Low-Temperature Bonded Cu/In Interconnect With High Thermal Stability for 3-D Integration

Yu-San Chien, Yan-Pin Huang, Ruoh-Ning Tzeng, Ming-Shaw Shy, Teu-Hua Lin, Kou-Hua Chen, Chi-Tsung Chiu, Ching-Te Chuang, *Fellow, IEEE*, Wei Hwang, *Fellow, IEEE*, Jin-Chern Chiou, *Member, IEEE*, Ho-Ming Tong, *Fellow, IEEE*, and Kuan-Neng Chen, *Senior Member, IEEE*

***Abstract*—Low-temperature (170 °C) Cu/In wafer-level and chip-level bonding for good thermal budget has been successfully developed for 3-D integration applications. For the well-bonded interconnect, Cu_2In and Cu_7In_3 phases with high melting temperature of 388.3 °C and 632.2 °C can be formed, indicating high thermal stability. In addition, stable low specific contact resistance of bonded interfaces can be achieved with the values of approximately 0.3 x 10^{-8} Ω-cm^2. In addition to exceptional electrical characteristics, the results of electrical reliability assessments including current stressing, temperature cycling, and unbiased HAST show excellent stability of Cu/In bonds without obvious deterioration. The low-temperature Cu/In bonding technology presents good bond quality and electrical performance, and possesses a great potential for future applications of 3-D interconnects.**

***Index Terms*—3-D integration, Cu/In bonding, interconnect.**

I. Introduction

THREE-DIMENSIONAL (3-D) integration can provide a viable solution to allow the extension of Moore's law and it has also made a significant progress in the development of electronic products with enhanced performance and functional diversification [1]–[4]. Among the different bonding technologies in 3-D integration, metal-to-metal bonding with good electrical connection and sufficient bonding strength appears to be the mainstream for the development of 3-D interconnects [5].

Conventional thermal-compression metal bonding requires high bonding pressure and bonding temperature to achieve high yields [6] that may lead to bonding misalignment and thermal damages of devices. Hence, developing a low-temperature bonding scheme is significant to meet the low thermal budget requirement [7].

Diffusion soldering has a great potential for the formation of thermally and mechanically stable bonds in electronic applications. Depending on the materials system involved, the bonding process can be performed at low temperature because interconnects consist of intermetallic phases with melting temperature much higher than the fabrication temperature. To achieve this goal, low-melting-point metals, such as In, can be considered as the interconnect material to be bonded during 3-D integration process. After bonding, complete consumption of low-melting-point In is required to avoid reliability issues in the following processes and in future operations.

In a previous work, Tian *et al.* [8] studied two identical Cu/In interconnects bonded at 260 °C, but only material investigation was reported without any electrical and reliability data. Sakuma *et al.* reported Cu/Ni/In and Cu/Ni/Au bonding results. However, the structure was complicated and no reliability test was evaluated [9]. In this paper, we report a low-temperature (170 °C) Cu/In bonding with an investigation on the structural quality, electrical characteristics, and reliability assessment. This bond scheme is simple, using only Cu and In direct bonding. With the obtained excellent bonding results and electrical performance, Cu/In bonding can be recommended as a promising solution for low-temperature bonding.

II. Experiment and Investigation of Cu/In Bonded Interconnects

Copper interconnects for bonding were prepared on silicon wafers with 500-nm TEOS by sputtering 300 nm of Cu and 30 nm of Ti layers in a multitarget chamber with approximate sputtering rates at 0.6 and 0.1 Å/s, respectively. The deposition process was under the working pressure of 7×10^{-3} torr with a base pressure of 1×10^{-6} torr. Indium interconnects for bonding were prepared by evaporating In and 30 nm of Ti layers with deposition rates at 1.5–1.8 Å/s for In and 1 Å/s for Ti, under a base pressure of 2–4 × 10^{-6} torr. The two different interconnects were then bonded face to face at 1.91 MPa, 170 °C for 30 min. Both chip-to-chip bonding and wafer-to-wafer bonding schemes were performed. The formation of intermetallic phases in the Cu/In bonds, by changing the thickness of In, was studied. The bond quality and the materials of

Manuscript received July 24, 2013; revised October 13, 2013; accepted January 8, 2014. Date of publication February 19, 2014; date of current version March 20, 2014. This work was supported in part by the Ministry of Education in Taiwan under the ATU Program, in part by the Advanced Semiconductor Engineering Group, and in part by the National Science Council under Grant NSC 101-2628-E-009-005 and Grant NSC 102-2221-E-009-160. The review of this paper was arranged by Editor S. Deleonibus.

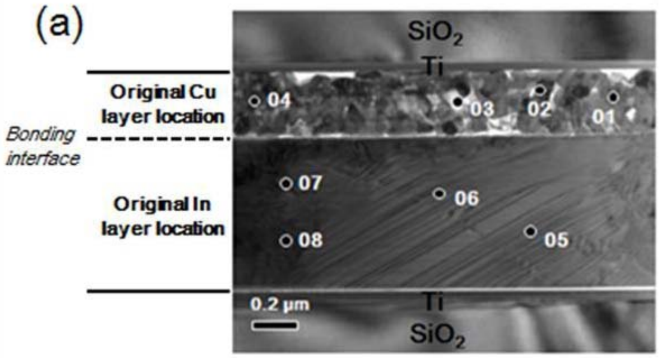
Y.-S. Chien, Y.-P. Huang, R.-N. Tzeng, C.-T. Chuang, W. Hwang, and K.-N. Chen are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan (e-mail: knchen@mail.nctu.edu.tw).

M.-S. Shy, T.-H. Lin, K.-H. Chen, C.-T. Chiu, and H.-M. Tong are with the Advanced Semiconductor Engineering Group, Kaohsiung 81170, Taiwan.

J.-C. Chiou is with the National Chiao Tung University, Hsinchu 300, Taiwan, and also with China Medical University, Taichung 40402, Taiwan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2014.2304778



(b)

Spectrum	In (at.%)	Cu (at.%)
1	56.2	43.8
2	55.8	44.2
3	53.1	46.9
4	54.3	45.7
5	53.5	46.5
6	52.8	47.2
7	51.8	48.2
8	51.2	48.8

Fig. 1. Structural characteristics of Cu/In bonded interconnect. (a) Cross sectional view of Cu/In bonded structure with the position of EDX spot and (b) corresponding composition with 680-nm thick In layer.

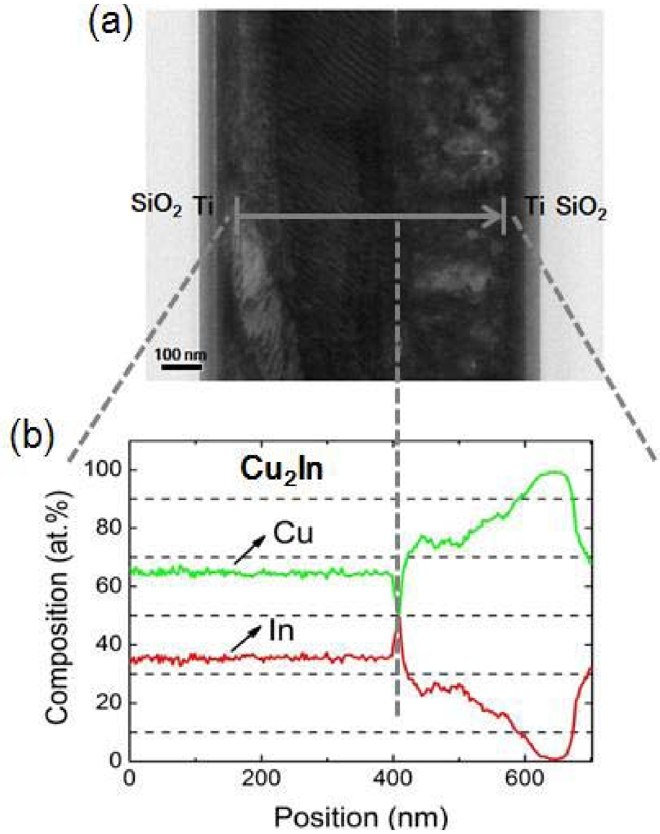


Fig. 2. Structural characteristics of Cu/In bond. (a) Cross sectional view of Cu/In bonded structure with the EDX scanning direction and (b) composition profile obtained by EDX line-scan with 400-nm-thick In layer.

bonded interconnects were analyzed through scanning acoustic tomograph (SAT), transmission electron microscope (TEM), and energy-dispersive X-ray spectrometer (EDX).

The cross sectional views of the Cu/In bonded structures and the composition profiles with different thicknesses (680, 400, 270, and 220 nm) of In are shown in Figs. 1–4. According to EDX analysis, the sample with the largest amount of In shows that Cu and In are uniformly mixed with no apparent IMC phases presented, as shown in Fig. 1. With a smaller amount of In, EDX results in Figs. 2 and 3 show that Cu_2In and Cu_7In_3 phases are formed in the structure. For the sample with the least In, no IMC phase is formed in the structure, as shown in Fig. 4.

To explain the inconsistent results for the four cases with different thicknesses of In, the reaction mechanism of Cu/In bonding has been proposed. According to the Cu-In phase diagram, three intermetallic phases can be formed under the bond temperature of 170 °C: $Cu_{11}In_9$, $\eta(Cu_2In)$, and $\delta(Cu_7In_3)$ [10]. The first IMC of $Cu_{11}In_9$ is formed by the reaction of liquid In and solid Cu. Then, the second Cu-richer IMC of Cu_2In starts to form through the interdiffusion between solid Cu and $Cu_{11}In_9$. On heating, the Cu_7In_3 phase with the richest Cu is formed by consumption of Cu_2In and Cu [8]–[14].

III. Case Studies

For the case of 680-nm In, as shown in Fig. 1(a) and (b), the absence of IMC is due to excessive In and fast interdiffusion between In and Cu. During the 30-min bonding, with a large amount of In compared with Cu, the liquid In was not able to fully react with Cu. Therefore, the first IMC of $Cu_{11}In_9$ did not form. Instead, Cu and In were uniformly mixed, which implies that the bonded structure is not preferred and may cause reliability issues.

For the case of 400-nm In, after liquid In reacted with Cu, the first IMC of $Cu_{11}In_9$ was formed. During the 30-min bonding, as the heating process went on, the Cu-richer second IMC of Cu_2In started to form by the diffusion of Cu and solid $Cu_{11}In_9$ consumption, as shown in Fig. 2(a) and (b). There was no apparent Cu_7In_3 detected in this structure owing to the insufficient time for the formation and growth of Cu_7In_3. Because the growth of Cu_2In and Cu_7In_3 at low temperature requires a large incubation time (longer than 30 min), the reaction was stopped before the appearance of Cu_7In_3. In addition, no $Cu_{11}In_9$ phase is detected, indicating a complete consumption of $Cu_{11}In_9$ for the formation of Cu_2In.

While further decreasing In thickness to 270 nm, the third IMC with richest Cu of Cu_7In_3 (m.p. 632.2 °C) can be formed by the total consumption of Cu_2In and reaction with Cu within the 30-min bonding process time. As shown in Fig. 3(a) and (b), there is no In detected in IMC and Cu regions. With the good bonding result of Cu_7In_3 (m.p. 632.2 °C) formation and the absence of In, the almost defect-free bond structure is preferred for the application of 3-D interconnects.

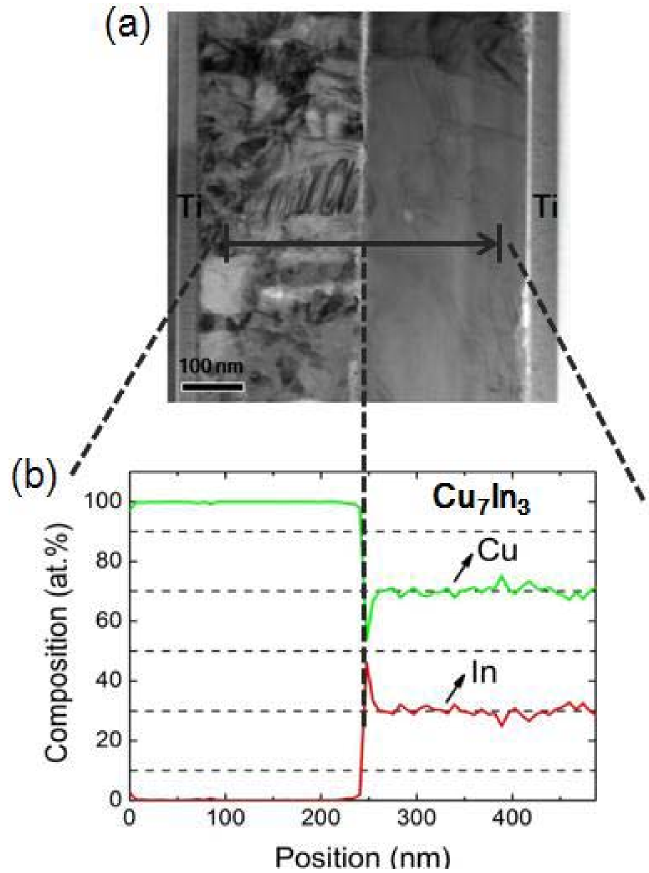
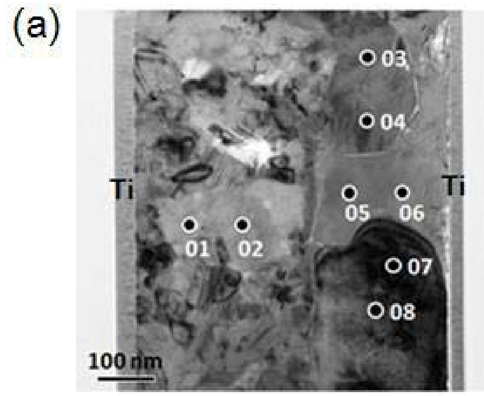


Fig. 3. Structural characteristics of Cu/In bond. (a) Cross sectional view of Cu/In bonded structure with the EDX scanning direction and (b) composition profile obtained by EDX line-scan with 270-nm-thick In layer.

With the investigation of bond results of 680, 400, and 270 nm In layers, when the thickness of Cu is fixed, the thinner In layer has the better bond quality. However, for the case with thinnest In of 220 nm, the results in Fig. 4(a) and (b) show that Cu atoms have dissolved into liquid In and formed uneven mixture. The final bonded structure should be Cu/Cu_7In_3 in this case based on previous results. To explain this phenomenon, the surface morphologies and roughness of 220-nm In were investigated prior to bonding. As shown in Fig. 5(a) and (b), independent small grains on the substrate are observed, but not a continuous film.

After a small amount of In was deposited on the substrate, separate clusters formed and grew. However, the distance for clusters to coalesce was too high during the deposition process. In addition, according to the previous study [15], due to the enhanced thermal movement and increased atomic diffusivity from the increasing temperature, big clusters of In would split into smaller clusters. Because the surface tension and the viscosity of In are very high at low bonding temperatures, the reaction time for the cluster dispersion should be longer [16]. Therefore, during the bonding process, at a temperature of 170 °C, indium melt required more time to spread over a larger area and uniformly contact with the Cu substrate. However, the reaction had stopped before the occurrence of IMC. Therefore, after 30-min bonding, there is only Cu/In mixed region and unreacted Cu shown in the bonded structure. With the absence of IMC, the bonded structure may remelt and cause serious reliability problems during the following process and electrical operation.



(b)

Spectrum	In (at.%)	Cu (at.%)
1	0	100
2	0	100
3	39.94	60.06
4	40.35	59.65
5	70.5	29.5
6	71.7	28.3
7	53.2	46.8
8	52.5	47.5

Fig. 4. Structural characteristics of Cu/In bond. (a) Cross sectional view of Cu/In bonded structure with the position of EDX spot and (b) corresponding composition with 220-nm-thick In layer.

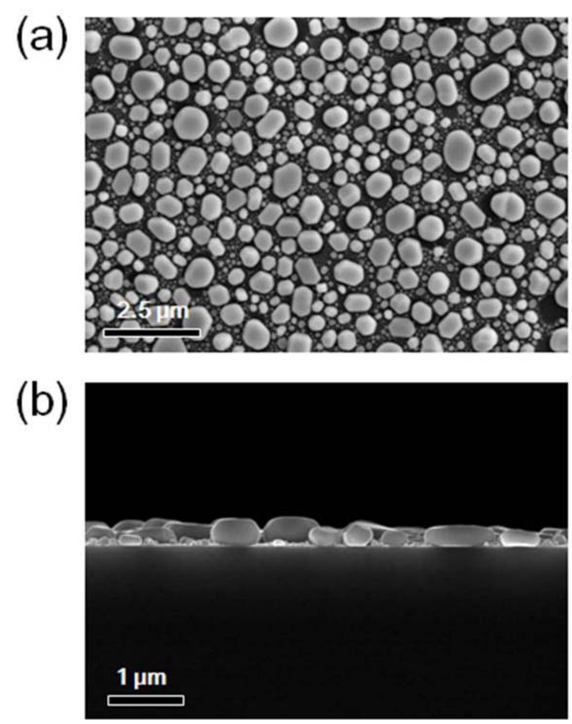


Fig. 5. Morphology of dewet In prior to bonding. (a) Top view and (b) cross sectional view.

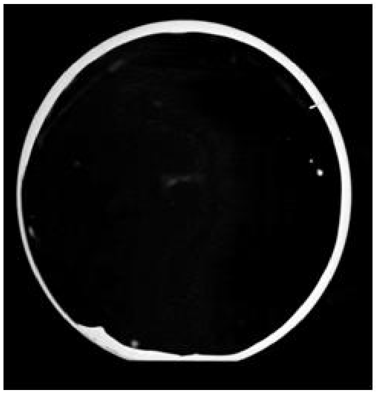


Fig. 6. Cu/In wafer bonding result by SAT analysis.

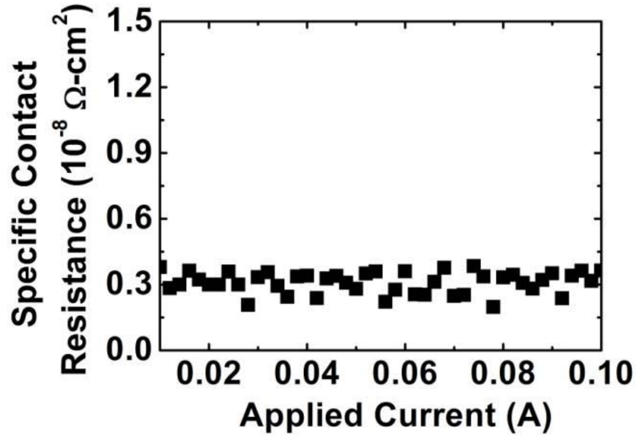


Fig. 7. Measured specific contact resistance of Cu-/In-bonded interconnect under different applied current.

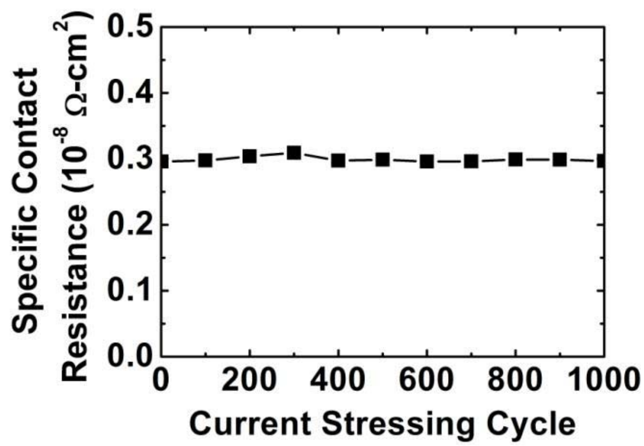


Fig. 8. Electrical characteristic of Cu-/In-bonded interconnect under current stressing test.

IV. Cu/In Bonding for 3-D Integration

With previous results, owing to its low melting temperature (156.6 °C), In needs to be completely consumed and transferred to intermetallic compounds. The usage amount of In should be kept at minimum. However, when In cannot form a continuous film on substrate, especially under the nanometer scale, the high surface roughness of In will hinder the bonding process and lead to varied formations of intermetallic compounds. Therefore, although thin In layer is preferred for Cu_7In_3 formation, the In layer is still needed to be thick enough for a continuous film and uniform contact with Cu.

The quality of In layer depends on the thickness, parameters during deposition, and substrate material used. Understanding the morphology of In layer is significant to achieve stable bond structure with the least amount of In usage. If In can be grown into a continuous film on substrate with sufficient amount of Cu for intermetallic compound formation, Cu_7In_3 phase with high thermal stability can be formed and is the best candidate for 3-D integration application.

The SAT analysis of the Cu/In wafer bonding with 270-nm-thick In layer is given in Fig. 6, which demonstrates a uniform wafer-level bonding integrity without voids. Because of its high melting temperature of 632.2 °C, the Cu_7In_3 phase can survive following CMOS and packaging processes. Therefore, this low-temperature Cu-In bond design with Cu/Cu_7In_3 formation can be applied in 3-D integration, such as the wafer-level lock-n-key scheme. In this scheme, In is designed for the lock structure with its surface lower than dielectric/SiO_2 surface, which can prevent In from possible dispersing during the heating process, while Cu is designed for the key structure. As the bonding process proceeds, Cu will diffuse toward In and react to form the final Cu/Cu_7In_3 bond.

V. Electrical Characteristic of Copper-/Indium-Bonded Interconnect

Specific contact resistance of the Cu-/In-bonded interconnect was measured by fabricating a Kelvin structure with the bonded area of 100 μm^2 (10 μm × 10 μm) [17]. The measurement result in Fig. 7 suggests a low specific contact resistance of approximately 0.3×10^{-8} Ω-cm^2 and a stable bonded structure with a small deviation of resistance under different applied current.

The Cu-/In-bonded interconnect was further evaluated by reliability tests. Fig. 8 also shows the low specific contact resistance after 1000 cycles of current sweeping between −0.1 and 0.1 A. In addition, it still presents a small deviation of resistance within the entire 1000 cycles of current sweeping, even at a large current density of 10^5 A/cm^2. The good stability of Cu-/In-bonded interconnect against current stressing is especially important for multiple operation and commercial application.

VI. Electrical Reliability of Cu-/In-Bonded Interconnect

To evaluate the thermal reliability of Cu-/In-bonded interconnect, temperature cycling test based on the JESD22-A104B standard was performed under temperature range of −55 to 125 °C with a duration of 15 min/zone [18]. As shown in Fig. 9, the bonded interconnect shows good stability after 1000 loops of temperature cycling, implying that the structure possesses good durability against expansion and shrinkage caused by large temperature variation.

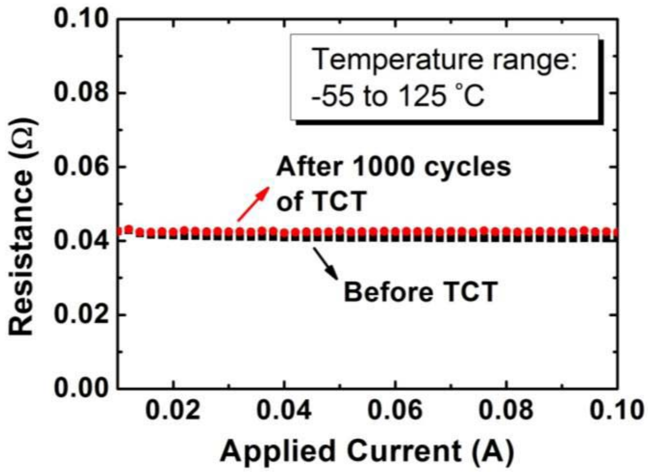


Fig. 9. Reliability test results of Cu-/In-bonded interconnect under temperature cycling test.

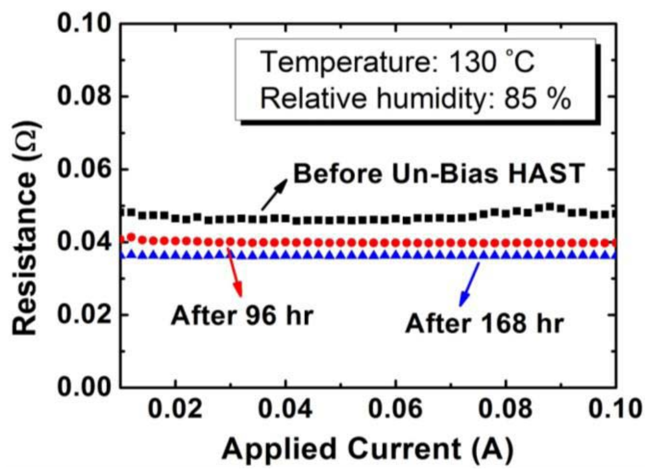


Fig. 10. Reliability test results of Cu-/In-bonded interconnect under un-biased highly accelerated stress test.

In addition, an unbiased highly accelerated stress test (unbiased HAST) based on the JESD22A-118 standard with the conditions of 85% RH and 130 °C was applied to evaluate the bonding quality of the interconnect. As shown in Fig. 10, it demonstrates good bonding quality of Cu/In bonded interconnect against moisture and corrosion from the observation of a more stable and lower resistance after 168 h of operation. The reduction of resistance may be attributed to the heat provided by the un-biased HAST that simulates the rearrangement of structures and eliminates the defects at the bonded interface [19].

According to these results, the Cu-/In-bonded interconnect is promising in terms of electrical performance and reliability, and is a possible choice for 3-D integration.

VII. Conclusion

In this paper, the scheme of reliable wafer-level and chip-level Cu-/In-bonded interconnects has been proposed and successfully demonstrated at 170 °C low temperature. The detailed study on structural characteristics of intermetallic phases formed in the Cu/In bonds has been presented in this paper. By applying the isothermal solidification reaction, it can form intermetallic compounds, Cu_2In and Cu_7In_3, which possess high thermal stability. Moreover, the evaluation of surface morphologies of In thin layer implied that it can finally form Cu_7In_3 phase in bonded structure if In grains have grown into a continuous film prior to bonding. With the complete consumption of In to react with Cu for intermetallic compounds, the Cu-/Cu_7In_3-bonded interconnect has shown the potential for future 3-D integration applications. This Cu-/Cu_7In_3-bonded interconnect possesses good bonding quality, high thermal stability, and great reliability under standard CMOS fabrication process and electrical operation conditions.

References

[1] S. J. Koester, A. M. Young, R. R. Yu, S. Purushothaman, K.-N. Chen, D. C. La Tulipe, *et al.*, "Wafer-level 3D integration technology," *IBM J. Res., Dev.*, vol. 52, no. 6, pp. 583–597, Nov. 2008.

[2] D. Sylvester and C. Hu, "Analytical modeling and characterization of deep-submicrometer interconnect," *Proc. IEEE*, vol. 89, no. 5, pp. 634–664, May 2001.

[3] A. Rahman and R. Reif, "System-level performance evaluation of three-dimensional integrated circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 6, pp. 671–678, Dec. 2000.

[4] C.-T. Ko and K.-N. Chen, "Wafer-level bonding/stacking technology for 3D integration," *Microelectron. Rel.*, vol. 50, no. 4, pp. 481–488, Apr. 2010.

[5] K. N. Chen and C. S. Tan, "Integration schemes and enabling technologies for three-dimensional integrated circuits," *IET Comput. Digital Tech.*, vol. 5, no. 3, pp. 160–168, May 2011.

[6] Y.-S. Tang, Y.-J. Chang, and K.-N. Chen, "Wafer-level Cu-Cu bonding technology," *Microelectron. Rel.*, vol. 52, no. 2, pp. 312–320, Feb. 2012.

[7] C.-T. Ko and K.-N. Chen, "Low temperature bonding technology for 3D integration," *Microelectron. Rel.*, vol. 52, no. 2, pp. 302–311, Feb. 2012.

[8] Y. Tian, N. Wang, Y. Li, and C. Wang, "Mechanism of low temperature Cu-In solid-liquid interdiffusion bonding in 3D package," in *Proc. 13th ICEPT-HDP*, Aug. 2012, pp. 216–218.

[9] K. Sakuma, P. S. Andry, B. Dang, J. Maria, C. K. Tsang, C. Patel, *et al.*, "3D chip stacking technology with low-volume lead-free interconnections," in *Proc. 57th ECTC*, Jun. 2007, pp. 627–632.

[10] Z. Bahari, E. Dichi, B. Legendre, and J. Dugué, "The equilibrium phase diagram of the copper-indium system: A new investigation," *Thermochim. Acta*, vol. 401, no. 2, pp. 131–138, May 2003.

[11] C. L. Yu, S. S. Wang, and T. H. Chuang, "Intermetallic compounds formed at the interface between liquid indium and copper substrates," *J. Electron. Mater.*, vol. 31, no. 5, pp. 488–493, May 2002.

[12] S. Sommadossi, W. Gust, and E. J. Mittemeijer, "Phase characterisation and kinetic behaviour of diffusion soldered Cu/In/Cu interconnections," *Mater. Sci. Technol.*, vol. 19, no. 4, pp. 528–534, Apr. 2003.

[13] S. Sommadossi, L. Litynska, P. Zieba, W. Gust, and E.J. Mittemeijer, "Transmission electron microscopy investigation of the microstructure and chemistry of Si/Cu/In/Cu/Si interconnections," *Mater. Chem. Phys.*, vol. 81, nos. 2–3, pp. 566–568, Aug. 2003.

[14] L. Litynska, J. Wojewoda, P. Zieba, M. Faryna, W. Gust, and E. J. Mittemeijer, "Characterization of interfacial reactions in Cu/In/Cu joints," *Microchim. Acta*, vol. 145, nos. 1–4, pp. 107–110, Apr. 2004.

[15] S.-J. Cheng, X.-F. Bian, J.-X. Zhang, X.-B. Qin, and Z.-H. Wang, "Correlation of viscosity and structural changes of indium melt," *Mater. Lett.*, vol. 57, no. 26–27, pp. 4191–4195, Sep. 2003.

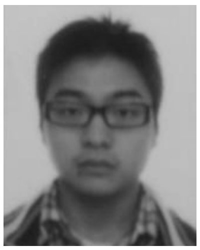
[16] M. A. McClelland and J. S. Sze, "Surface tension and density measurements for indium and uranium using a sessile-drop apparatus with glow discharge cleaning," *Surf. Sci.*, vol. 330, no. 3, pp. 313–322, Jun. 1995.

[17] K. N. Chen, A. Fan, and C. S. Tan, "Contact resistance measurement of bonded copper interconnects for three-dimensional integration technology," *IEEE Electron Device Lett.*, vol. 25, no. 1, pp. 10–12, Jan. 2004.

[18] JEDEC Standard. Arlington, VA, USA. (2005). *Temperature Cycling* [Online]. Available: http://www.jedec.org/

[19] K. N. Chen, C. S. Tan, A. Fan, and R. Reif, "Abnormal contact resistance reduction of bonded copper interconnects in three-dimensional integration during current stressing," *Appl. Phys. Lett.*, vol. 86, no. 1, p. 011903, Jan. 2005.

Yu-San Chien received the M.S. degree in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 2013.



Yan-Pin Huang received the Degree in material science engineering from the National Chiao Tung University (NCTU), Hsinchu, Taiwan, where he is currently pursuing the Ph.D. degree in electronics engineering.

Ruoh-Ning Tzeng, photograph and biography not available at the time of publication.

Ming-Shaw Shy, photograph and biography not available at the time of publication.

Teu-Hua Lin, photograph and biography not available at the time of publication.

Kou-Hua Chen, photograph and biography not available at the time of publication.

Chi-Tsung Chiu, photograph and biography not available at the time of publication.

Ching-Te Chuang (S'78–M'82–SM'91–F'94) received the Ph.D. degree in electrical engineering from the University of California, Berkeley, CA, USA, in 1982.

He is currently a Life Chair Professor with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan.

Wei Hwang (F'01–LF'09) received the Ph.D. degree from the University of Manitoba, Winnipeg, MB, Canada.

He is currently a Life Chair Professor of Electronics Engineering with the National Chiao Tung University, Hsinchu, Taiwan.

Jin-Chern Chiou (M'06) received the M.S. and Ph.D. degrees in aerospace engineering science from the University of Colorado, Boulder, CO, USA, in 1986 and 1990, respectively.

He is currently the Professor of the Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, and the Department of Medicine, China Medical University, Shenyang, China, the Vice Superintendent/Director of Biomedical Engineering Research and Development Center, China Medical University Hospital, Taichung, Taiwan.

Ho-Ming Tong (F'07) received the Ph.D. degree in chemical engineering from Columbia University, New York, NY, USA.

He is currently the Chief Research and Development Officer and the General Manager of Group Research and Development, ASE Group, Kaohsiung, Taiwan. He served with IBM Thomas J. Watson Research Center, New York, as a Research Staff Member, and as a Senior Engineering Manager with IBM's East Fishkill Facility.

Kuan-Neng Chen (M'05–SM'11) received the Ph.D. degree in electrical engineering and computer science, and the M.S. degree in materials science and engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA.

He is currently a Professor with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan. He was a Research Staff Member with the IBM Thomas J. Watson Research Center, Yorktown Heights, USA.