Numerical Study of Very Small Floating Islands

Hiroshi Watanabe, *Senior Member, IEEE*, Kira (Chih-Wei) Yao, and Jerry (Po-Jui) Lin

***Abstract*— The electrical property of very small floating island whose diameter is less than the de Broglie length is numerically investigated without fitting parameters. In general, it is difficult to well define the capacitance of very small floating islands. In this paper, instead of using the capacitance of islands, the kicking algorithm is applied for simulating the single-electron phenomena of spherical islands (the diameter: Ø = 0.6, 4, and 6 nm). As a result, the self-potentials of islands are successfully obtained within the precision equivalent to the movement of the sole electron with regard to given gate voltages. In addition, the transient simulation is demonstrated using the dwell time during which an electron is waiting for the next tunneling. The Coulomb blockade is successfully simulated without using the capacitance of very small floating islands. It is also found that trap-assisted tunneling is prohibited by Coulomb blockade at low electric field and can occur at high electric field.**

***Index Terms*— Capacitance coupling ratio, Coulomb blockade, device modeling, floating gate, floating island, silicon dot, single-electron phenomena, trap-assisted tunneling.**

I. Introduction

FLOATING islands have been extensively studied in wide area of electron devices technologies in recent years. Those islands exhibit the single-electron effect as the size is decreased. They are then classified with the size: such as floating gates of nonvolatile memories (larger than 10 nm), single-electron transistors (SETs; 2–10 nm) [1], molecular devices (less than 1 nm) [2], and dangling bonds (2–3 Å), as shown in Fig. 1. It should be noted that the single-electron effect becomes notable when floating island is smaller than 10 nm [3], which is equivalent to de Broglie length (DBL). On the other hand, dangling bonds, molecular devices, and single-electron devices (SET) may have a similar property, even though some molecular effects would be involved as the size is further decreased. It can then be regarded that SET exhibits an essential property of very small floating islands. In SET, there is a floating dot with Ø being 2–10 nm, which is isolated from source and drain by insulating film, and then the mechanism of transportation is tandem (sequential) tunneling from source to dot and then dot to drain [1]. After the first tunneling (source to dot), a transporting electron must dwell in dot while waiting for the second tunneling (dot to drain). While the electron dwells in dot, the self-potential of dot is decreased (shallower) by the negative elementary charge (q) of the electron. In the opposite case, the self-potential of dot is increased (deeper) by the decrease of the number of stored electrons. As long as source continues to supply electrons that will tunnel to dot and drain continues to absorb the electrons, the tandem tunneling will be continued. The self-potential of dot will become shallow and deep alternatively during the tandem tunneling [4]. This corresponds to the Coulomb oscillation [5]–[11]. In molecular transistors, molecular islands (e.g., C_{60}) may exhibit the Coulomb oscillation. The dangling bonds are regarded as local traps in dielectric films as long as those bonds can capture and emit electrons. It is regarded that local traps cause the issue of leakage current [12]–[14], random telegraph noise [15], and so on. The charge trapping layers made by gathering plenty of local traps therein are adopted in the early 3-D NAND flash to store the charge [16]–[18]. By this way, the essential property of very small floating islands may imply a universal problem throughout many generations, i.e., from today's reliability issues of real-life electron devices to nanoelectronics (involving molecular devices).

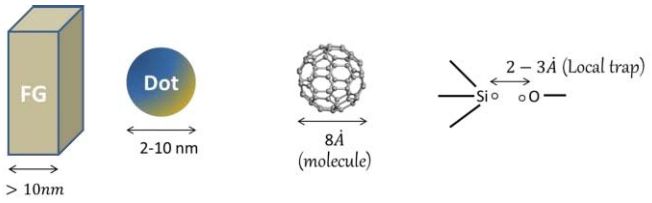

Fig. 1. Illustration of floating islands.

To carefully investigate the essential properties of very small floating islands, the single-electron sensitive computation is indispensable [4], [14]. In this paper, we will apply it to simple examples (i.e., single-electron box [3]). In Section II, we describe the calculation method. The results obtained here are shown in Section III. Sections IV and V are devoted to the discussion and the conclusion, respectively.

II. Modeling

A. Ambiguity in the Past Modeling

To design and integrate the circuit of SETs in large-scale integrated chip, the SPICE-compatible modeling is necessary [19]–[22]. The gap opens in the measured I–V characteristics, which is attributable to Coulomb blockade. The capacitance of dot was roughly estimated by dividing the elementary charge by the measured gap in voltage. The capacitance is then involved as a fitting parameter into SPICE modeling [19]–[22].

Manuscript received October 4, 2013; accepted February 12, 2014. Date of current version March 20, 2014. This work was supported in part by SK Hynix, Icheon, Korea, and in part by the National Science Council of Taiwan under Grant NSC102-2221-E-009-170. The review of this paper was arranged by Editor J. Knoch.

The authors are with the National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: hwhpnabe@gmail.com; elegant.pegasus@gmail.com; jerry76513@hotmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2014.2306935

In theory, Wang and Zunger [23] calculated the dielectric constant of silicon dot composed of several hundred atoms, and then concluded that the dielectric constant is decreased with the decrease of dot radius. However, to calculate the capacitance, more atoms of O and Si are necessary to surround the dot. Macucci *et al.* [24], [25] and Macucci and Hess [26] regarded disk whose radius is 50–200 nm as quantum dot. They, thereby, carefully studied 2-D electron gas system and then concluded that the capacitance is alternatively changeable to the number of electrons stored in disk. Kumar *et al.* [27] divided the 3-D space with dot into the plain (whose diameter is 300 nm) and the vertical axis, for solving Poisson–Schrodinger solver. They adopted the boundary condition that the normal electric field at the boundary of dot is zero. This is valid in the plain while the plain is wide enough and invalid in the vertical axis if the electric field is applied across this direction. In other words, they also considered the disk and then used 2+1-D Poisson–Schrodinger solver. It is regarded from their calculation that the capacitance of floating dot is increased with the charge stored in dot. This is not consistent with [24]–[26]. Madheswaran and Kavitha [28] carefully considered the topological deformation of the stacking layers of dots in the vertical direction in solving the Poisson equation, while not in the other direction. They also solved 2+1-D Poisson–Schrodinger solver.

On the other hand, single-dot memories have been studied in experiments [3], [29]–[31] and in simulations [34], [35]. Nakazato *et al*. [29] fabricated single-electron memory with tunnel junction and 30-nm GaAs dot and then experimentally demonstrate the Coulomb blockade phenomena at 30 mK. They expected that it may work even at room temperature if the scale of dot becomes less than 5 nm. Guo *et al.* [30], [31] fabricated 7-nm floating gate on 10-nm width channel and then observed the staircase threshold voltage change by program voltage at room temperature. Yano *et al*. [3] pointed out that the capacitance of floating dot is a key parameter to design single-electron memories. They regarded single-electron box (Fig. 2) as main component to model the single-electron memory cells in a similar manner with nonvolatile memory. They found that total capacitance related to dot (involving parasitic capacitance) should be smaller than 3 aF at room temperature. According to this scheme, Nakajima *et al*. [32] and Welser *et al*. [33] fabricated deca-nano floating gate on thin silicon-on-insulator layer independently of each other. The square disks (smaller than 50 nm) were, on the other hand, regarded as floating gate and then numerically investigated [34], [35]. It should be noted that the geometry of these memory cells is commonly analogous to the first floating-gate memory cell demonstrated in [36], while the size is quite different. Kahng and Sze [36] calculated oxide field from capacitance and stored charge of floating gate for the first time. This model has been extensively used to know self-potential of floating gate in the field of nonvolatile memory engineering.

It appears possible to determine capacitance of floating island from the Coulomb blockade measurement and then use it to know self-potential of floating island at a given charge in device simulation. However, none has proved that the capacitance determined from Coulomb blockade is equivalent to that used in device simulation. It should be noted that surface charge cannot be defined if island's diameter is smaller than DBL, while floating gate is larger than DBL in the modeling of Kahng and Sze. In addition, the spatial geometry of devices used in measurements is generally different from that used in device simulation. Overall from the literature, we can remark as follows.

1) The capacitance of floating islands has been regarded as fitting parameter.
2) The calculation of capacitance of very small floating island is difficult.
3) No visible relation has been found between the capacitance that determined by Coulomb blockade measurements and that used in device simulation.

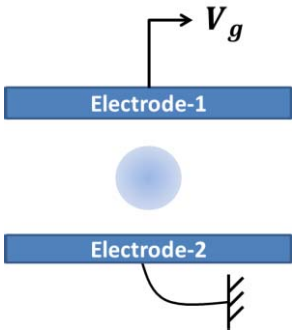

Fig. 2. Illustration of simulation structure with silicon dot.

B. Overview of Preset Condition

To focus on the technological usability of device simulation with floating islands (floating gates, molecular islands, local traps, and so on), we ignore the impact of any molecular perturbation. In other words, we deal with the impact of stored charge. We ignore the interface states at the curved interface of silicon dot [37] and molecular relaxation (or bond rupture) owing to charge-state change [38]. The higher order approximation like those will be left in the future study.

No well-defined surface charge exists as long as the size of floating island is smaller than the DBL. To save the computational resource, we also assume that the profile of the electron density is homogeneous inside floating islands. We accordingly focus on the investigation of the essential electrical property of floating islands, which is caused by stored charge.

Instead of these simplifications, we must solve 3-D Poisson equation with the highest precision, which is equivalent to the movement of sole electron in device. To demonstrate and validate our simulation method, we select a simplest structure with a spherical silicon dot (single-electron box [3]), as shown in Fig. 2. From hereafter, we may regard spherical island as dot. The dot exists between electrode-1 and electrode-2 in vertical direction. The electrode-1 is the gate (in which the gate voltage V_g is applied) and the electrode-2 is grounded. The entire space other than silicon dot is occupied by SiO_2 whose dielectric constant is 3.9. The dielectric constant of silicon dot is, *a priori*, assumed to be same as that of bulk

silicon, 11.7. It should be noted that the interface dielectric constant differs from that of bulk [39] owing to the molecular perturbation that is ignored here for the simplicity. It is still hard to self-consistently complete material science simulation and 3-D Poisson solver. The higher order perturbation like this will be left to the future study, as mentioned earlier.

The element of hopping transport via dot is composed of tunneling between dot and an electrode. That is, the initial and final points of tunneling are divided into dot and an electrode. If we are subjected to quantum mechanics, we must consider all possible paths of tunneling at the given potential profile. The tunneling flux is calculated across each tunnel path that connects initial and final points of tunneling using Harrison's formula [40]. Since we selected the simplest structure, as shown in Fig. 2, we may ignore the curved tunnel paths [4], [14]. The tunnel flux divided by the elementary charge is regarded as the inverse of the dwell time after the previous tunneling [4], [14]. The time is updated by the obtained dwell time, while updating the number of electrons stored in dot (N) according to the tunneling. If an electron tunnels from an electrode to dot, N is increased by unity. On the contrary, if an electron tunnels from dot to an electrode, N is decreased by unity. Without the precision equivalent to the movement of sole electron [i.e., single-electron sensitivity (SES)] in solving Poisson's equation, it would be impossible to perform the transient simulation in this manner.

To make clear the advantage, let us discuss more about the floating dot problem in solving Poison's equation. Since Poisson's equation is a boundary value problem, we need to know the self-potential of floating dot as a part of boundary condition. Provided that we knew the capacitance coupling ratio (C_r), it was possible to calculate the self-potential using $C_r \times V_g$. However, the diameter of floating dots considered here is less than 10 nm, i.e., the DBL. Because of the quantum mechanical effect, the stored charge can be no more accumulated at the surface of floating dot. The electric field across oxide layers is thereby determined by the total amount of stored charge in floating dot and not by the surface charge. Therefore, we can no more use the capacitance coupling ratio to obtain the self-potential. In reply to this serious situation, we use the kicking algorithm that is briefly described in Section II-C and already used in [4] and [14].

C. Single-Electron Sensitivity

First, we solve 3-D Poisson equation at a given N in a conventional manner. It should be noted that the entire device region is composed of a silicon dot, the oxide region which surrounds the dot, and the electrodes defining the boundary condition. Once it is converged, we can obtain the charge stored in dot (Q) from the calculation result of 3-D Poisson solver as follows:

$$Q := -\iiint_{\text{dot}} \varepsilon_{\text{Si}} \nabla^2 \varphi d^3 r. \tag{1}$$

The ε_{Si} shows the permittivity of silicon (the dielectric constant is 11.7.) and φ is the obtained potential. The integration is performed within the entire dot. It should be noted that $|N + Q/q|$ must be less than the predetermined error as long as the calculation is appropriately converged. However, since the dot is floating, $|N + Q/q|$ cannot be generally less than the predetermined error even though 3-D Poisson solver is converged. We then kick the floating island with the kick potential (V_{kick}) as follows: $\varphi_{\text{dot}} = \varphi_{\text{dot}} + V_{\text{kick}}$, where φ_{dot} is a potential inside dot. In this paper, we have set V_{kick} as homogeneous inside dot for simplicity, while φ_{dot} is generally inhomogeneous

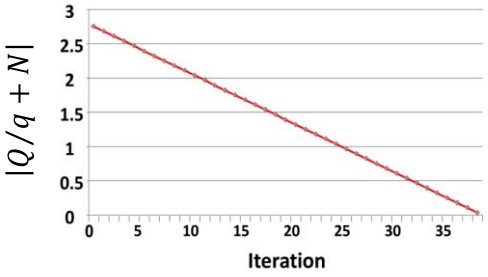

Fig. 3. Calculated error with regard to the iteration. The SES is achieved at the 32th iteration.

$$V_{\text{kick}} = \begin{cases} -\delta & \text{for} \quad N > 0 \quad \text{and} > -\dfrac{Q}{q}; \; N < 0 \quad \text{and} > -\dfrac{Q}{q} \\ +\delta & \text{for} \quad N > 0 \quad \text{and} < -\dfrac{Q}{q}; \; N < 0 \quad \text{and} < -\dfrac{Q}{q}. \end{cases} \tag{2}$$

If N is positive and larger than $-Q/q$, we regard the negative charge as short in the current step. To compensate the lack of the negative charge, V_{kick} is a small negative voltage ($-\delta$). If N is positive and smaller than $-Q/q$, we regard the negative charge as excess in the current step. To compensate the excess negative charge, V_{kick} is a small positive voltage ($+\delta$). If N is negative and smaller than $-Q/q$, we regard the positive charge as short in the current step. To compensate the lack of the positive charge, V_{kick} is a small positive voltage. If N is negative and larger than $-Q/q$, we regard the positive charge as excess in the current step. To compensate the excess positive charge, V_{kick} is a small negative voltage. The amplitude of V_{kick} is empirically determined by considering the computational speed and the robustness. In this paper, we have set: $|V_{\text{kick}}| = \delta = 1$ mV.

Once the floating island is kicked at the end of the previous step, we move on to the next step of the iteration. We solve 3-D Poisson solver again, and then compare the discrepancy $|N + Q/q|$ with the predetermined error again. As shown in Fig. 3, it is found that the discrepancy is monotonically decreased and becomes less than 0.5 at the 32th iteration. Note that $|N + Q/q|$ smaller than 0.5 corresponds to the sensitivity that is equivalent to the movement of sole electron. Here, we can achieve the SES, similar to [4] and [14]. The residual error corresponds to the amplitude of single-electron fluctuation. In this paper, we have set the predetermined error to be 0.05. If the discrepancy is smaller than the predetermined error, we end the calculation. By this way, the potential distribution is obtained for the given N and the applied voltage on the electrodes.

D. Tunnel Path Search

We describe the procedure of searching the possible tunnel paths here. In the structure that is shown in Fig. 2, the possible tunnel paths are divided into three groups:

1) group-a: between dot and electrode-1;
2) group-b: between dot and electrode-2;
3) group-c: between electrode-1 and electrode-2.

Here, we require that two paths among two different groups can be selected at the same moment, while two paths in the same group cannot be selected at the same moment. We, furthermore, suppose that the paths are all straight, because the structure to be investigated is quite simple.

Next, the entire distribution of the potential obtained by 3-D Poisson solver with the SES is loaded to the tunnel path searcher. The barrier heights are 3.34 and 3.5 eV at the interface of dot and electrodes, respectively. The tunneling electron exists at the conduction band edge of dot if the initial point of tunnel path is at the boundary of the dot. Otherwise, the tunneling electron exists at the Fermi level of electrode, which involves the initial end of the considered tunnel path. We thereby calculate the tunneling flux related to each tunnel path using Harrison's formula [40] as similar to [4] and [14]. Subsequently, the most possible path is selected from each group at the classical limit ($\hbar \rightarrow 0$). This is analogy to the Lagrange equation, which is equivalent to semiclassical approximation in quantum mechanics. By this way, path-a, path-b, and path-c are selected from group-a, group-b, and group-c, respectively, and the others are then truncated. This truncation substantially reduces the computational time; then enabling 3-D transient simulation.

Subsequently, the dwell time (τ) is calculated as the time, which has passed until an electron tunnels via selected path. In this paper, we select the shortest dwell time path among path-a, path-b, and path-c. The charge distribution is thereby updated by the tunneling of sole electron according to the selected tunnel path. The updated charge distribution is loaded to 3-D Poisson solver with the SES. The potential profile obtained by solving 3-D Poisson solver with SES is regarded as updated by the tunneling of sole electron. It should be noted that, without the SES, the loaded charge distribution would be regarded as not updated.

E. About Coulomb Blockade

Coulomb blockade cannot be well defined, as long as the capacitance of dot is not well defined. However, the self-potential of floating dot is different before and after the tunneling of electron via dot. When an electron is emitted from dot, the self-potential is increased, and then the energy level of dot is lowered in energy band diagram. When an electron is injected into dot, the self-potential is decreased and then the energy level of dot rises in energy band diagram. By this way, we need to take care of the energy level difference (δE) before and after tunneling [14]. For example, the initial end of tunnel path is the electrode that will emit a tunneling electron and the final end of tunnel path is the dot that will capture the electron. The energy loss during the considered tunneling (δE) becomes negative if the energy of tunneling electron is lower than the dot level that will be updated by the tunneling. Even though δE is negative, the tunneling electron can borrow $|\delta E|$ for the duration $(\hbar/(2|\delta E|))$. If $(\hbar/(2|\delta E|))$ is longer than the dwell time, the tandem tunneling can occur. Otherwise, the tandem tunneling is prohibited.

III. Results

To demonstrate the present method below, we adopt the structure with a spherical silicon dot (i.e., single-electron box [3]): the diameter of dot is 4 nm ($\emptyset = 4$ nm); the system volume is (10 nm $\times$ 10 nm $\times$ 10 nm); the electrode-1 is the sheet of (10 nm $\times$ 10 nm) at $Z = 10$ nm; and the electrode-2 is the sheet of (10 nm $\times$ 10 nm) at $Z = 0$ nm. Next, we set the initial condition as follows: the center of dot exists at (5 nm, 5 nm, 10 nm$-t_1$); the gate voltage applied on electrode-1 is 3 V. ($V_g = 3$ V); and the number of stored electrons is 5 ($N = 5$). This means that the negative charge is stored by $-5q$ in dot, i.e., programmed state. Here, t_1 is the shortest distance from the center of dot to electrode-1.

First, we set $t_1 = 5$ nm. This structure and the initial condition are loaded to the present simulator, and then we obtain the calculated potential profile with the SES, as shown in Fig. 4. In Fig. 4(a), the possible paths are depicted by arrows on the potential profile calculated by 3-D Poisson solver with the SES. In Fig. 4(b), there are three paths (path-a, path-b, and path-c) which are most possible in group-a, group-b, and group-c, respectively. The calculated dwell times are $2.10 \times 10^{-14}, 3.73 \times 10^{-14}$, and 2.65×10^{-14} s with path-a, path-b, and path-c, respectively. Although the structure is symmetric in Z-axis, five electrons stored in dot cause the dwell time of path-a shorter than that of path-b. In Fig. 4(c), the most possible path is path-a, since the shortest dwell time corresponds to the maximum tunnel probability.

Let us define the self-potential of floating dot ($V_{\rm dot}$) as the potential at the center of dot, measured from the grounded electrode (electrode-2). Then, we can plot the relation of the calculated $V_{\rm dot}$ and V_g at a given N, as shown in Fig. 5. We calculate two conditions that the center of dot exists at (5, 5, 5 nm) and (5, 5, 7 nm). The shortest distance from the electrode-2 to the center of dot is depicted t_2, where $t_1 + t_2 =$ 10 nm. The results of $t_1/t_2 = 5$ nm/5 nm $t_1/t_2 = 3$ nm/7 nm are plotted by the squares. The y-intercept is positive, neutral, and negative at $N = -5$, 0, and $+5$, respectively. From the least squares fitting of $t_1/t_2 = 3$ nm/7 nm, it is found that the slope is $0.7000 \pm 0.05\%$ irregardless of N, while the y-intercept is 0.6239, 4×10^{-17}, and -0.6239 V at $N = -5$, $N = 0$, and $N = 5$, respectively. In nonvolatile memory cells, we know $\Delta V_{\rm fg} = C_r \times \Delta V_g$, where $V_{\rm fg}$ is the self-potential of floating gate, according to [36]. We can thereby regard the slope $(\Delta V_{\rm dot}/\Delta V_g)$ as the equivalent capacitance coupling ratio ($\rm EC_r$). The obtained $\rm EC_r$ is thereby independent of the charge state of dot: programmed, neutral, and erased, respectively. On the other hand, the y-intercept is sensitive to the change of the charge state, e.g., 0.6239 V to the change from $N = 0$ (neutral) to $N = -5$ (erased) and -0.6239 V to the change from $N = 0$ (neutral) to $N = 5$ (programmed). The y-intercept, accordingly, is -0.12478 V at $\Delta N = 1$ in this

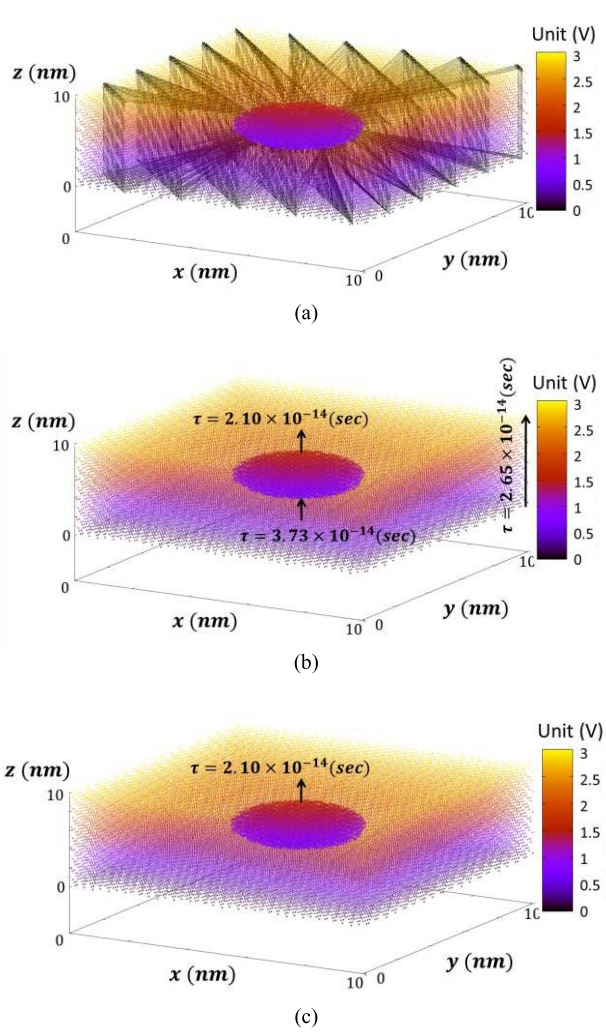

Fig. 4. The calculated potential profile when Ø = 4 nm, $N = 5$, and $V_g = 3$ V. There is a gradation of potential even inside dot. (a) The all possible tunneling paths from group-a, group-b, and group-c. (b) The tunnel paths with shortest dwell time from each group: dot to electrode-1 (upper electrode) (dwell time being 2.10×10^{-14} s), electrode-2 to dot (dwell time being 3.73×10^{-14} s), and electrode-2 to electrode-1 (dwell time being 2.65×10^{-14} s). (c) The tunnel path with shortest dwell time among all possible tunnel paths.

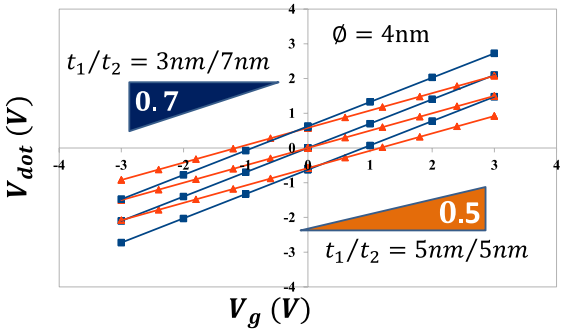

Fig. 5. Calculated self-potential ($V_{\rm dot}$) and the gate voltage (V_g). The t_1 and t_2 show the shortest distance from the center of the dot to the electrode-1 and that from the center of the dot to the electrode-2, respectively. The diameter of the dot is 4 nm.

structure. Regarding that $\mathrm{EC}_r = 0.7$, the equivalent threshold voltage shift per electron (EVT) is 0.12478 V/0.7 ≅ 0.178 V. We can plot this by the circle with the past result of NAND

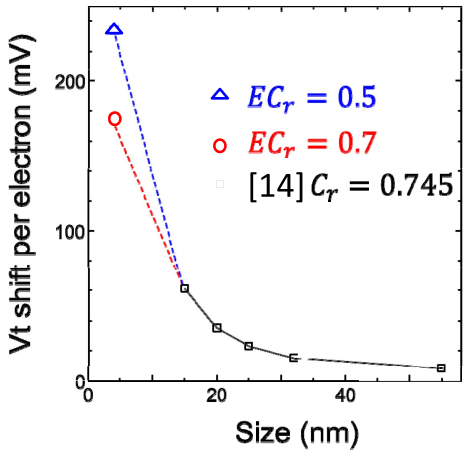

Fig. 6. Equivalent V_t shift per electron with regard to the size of floating island. From 55 to 15 nm is the data of cubic floating gate [14], while 4 nm is the data of this paper.

flash ($C_r = 0.745$) from 55- to 15-nm generations [14] (the small squares), as shown in Fig. 6. It is found that the EVT of $\mathrm{EC}_r = 0.7$ shows a reasonably smooth plot from $C_r = 0.745$. From the least square fit of $t_1/t_2 = 5$ nm/5 nm, it is found that the slope is $0.5000 \pm 0.04\%$ irregardless of N, while the y-intercept is 0.5973, 1×10^{-18}, and −0.5973 V at $N = -5$, $N = 0$, and $N = 5$, respectively. The obtained EC_r is thereby independent of the charge state of dot: programmed, neutral, and erased, respectively. On the other hand, the y-intercept is sensitive to the change of charge state, e.g., 0.5973 V to the change from $N = 0$ (neutral) to $N = -5$ (erased) and −0.5973 V to the change from $N = 0$ (neutral) to $N = 5$ (programmed). The y-intercept, accordingly, is −0.11946 V at $\Delta N = 1$ in this structure. Regarding that $\mathrm{EC}_r = 0.5$, the EVT is $0.11946V/0.5 \cong 0.239$ V, which is much higher than that of $\mathrm{EC}_r = 0.7$. This is also plotted by the triangle in Fig. 7 for the comparison. By this way, EC_r just coincides with $t_1/(t_1 + t_2)$. This implies that the capacitance of very small dot is consistent with those of parallel plates, in which the distances are t_1 and t_2, respectively.

Let us demonstrate the transient simulation with the initial condition that $V_g = 0$ V (fixed), $N = 10$ (initial), the diameter of dot is 6 nm (Ø = 6 nm), the center of dot is (5, 5, 5 nm), the size of the simulation structure is (10, 10, 10 nm), the top of this structure is covered by electrode-1 on which V_g is applied, and the bottom is covered by electrode-2, which is grounded. In Fig. 7, it is found that the number of electrons stored in dot is monotonically decreased from $N = 10$ to $N = 1$ during the first 1.8×10^{-10} s. At the same moment, the self-potential of dot is monotonically increased from $V_{\rm dot} = -0.397$ to $V_{\rm dot} = 0.0$ V with each step corresponding to about 40 meV, which is equivalent to thermal energy at room temperature. Since $\Delta V_{\rm dot}$ per electron is increased as the diameter of dot is decreased, 6 nm is the offset diameter on which single-electron phenomena can be observable at room temperature. Note here that 6 nm is quite small compared with 20 nm, which is estimated by assuming Coulomb blockade ($\Delta Q = \sqrt{2k_B \mathrm{TC}}$) [3]. On the other hand, it is consistent to 5 nm in [29].

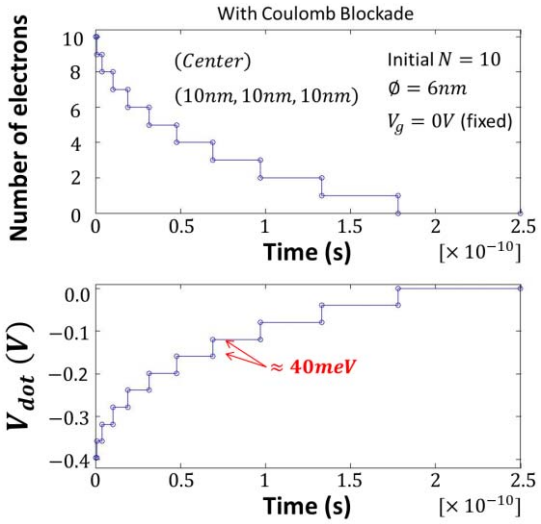

Fig. 7. Demonstration of transient simulation using dwell time as time to notch the next tunneling. The Coulomb blockade is considered. The diameter of dot is 6 nm and the gate voltage is zero.

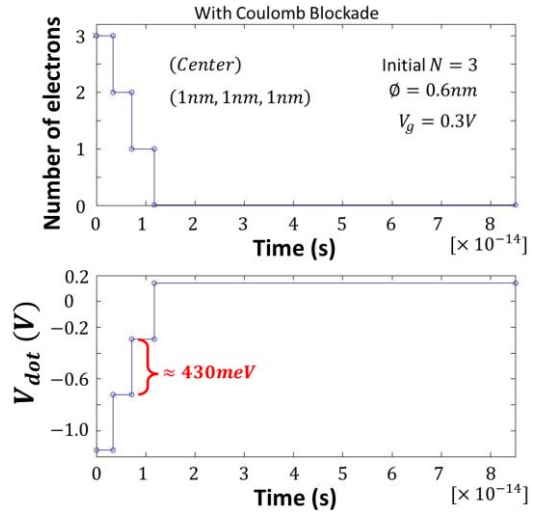

Fig. 8. Demonstration of transient simulation using dwell time as time to notch the next tunneling. The Coulomb blockade is considered. The diameter of dot is 0.6 nm and the gate voltage is low (0.3 V).

Next, we demonstrate much smaller floating island in single-electron box with the initial condition that $V_g = 0.3$ V (fixed), $N = 3$ (initial), the diameter of dot is 0.6 nm ($\emptyset = 0.6$ nm), the center of dot is (0.5, 0.5, 0.5 nm), the size of the simulation structure is (1, 1, 1 nm), the top of this structure is covered by electrode-1 on which V_g is applied, and the bottom is covered by electrode-2, which is grounded. In Fig. 8, it is found that the number of electrons stored in dot is monotonically decreased from $N = 3$ to $N = 0$ during the first 1.2×10^{-14} s. At the same moment, the self-potential of dot is monotonically increased from $V_{\rm dot} = -1.15$ to $V_{\rm dot} = 0.141$ V with each step corresponding to about 430 meV, which is ten times larger than thermal energy at room temperature. Note here that $V_{\rm dot}$ is changed from negative to positive, when N is changed from one to zero. It might appear that the positive

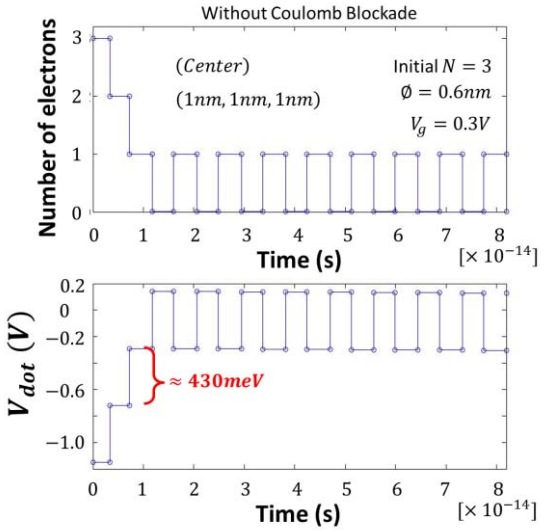

Fig. 9. Demonstration of transient simulation using dwell time as time to notch the next tunneling. The Coulomb blockade is ignored. The diameter of dot is 0.6 nm and the gate voltage is low (0.3 V).

$V_{\rm dot}$ causes electron to tunnel from bottom electrode to dot and then N is changed from zero to one. However, this does not occur in Fig. 8, since $V_{\rm dot}$ is negative when $N = 1$. This tunneling is prohibited by the idea of Coulomb blockade. To check the validity of the present modeling of Coulomb blockade, the simulation result without Coulomb blockade with the same condition with Fig. 8 is shown in Fig. 9. After 1.5×10^{-14} s, the oscillation occurs in $V_{\rm dot}$ and between $N = 0$ and $N = 1$. When $N = 1$, $V_{\rm dot}$ is shallow and then the emission rate from dot to electrode-1 is higher than the injection rate from electrode-2 to dot. When $N = 0$, $V_{\rm dot}$ is deep and then the injection rate from electrode-2 to dot is higher than the emission rate from dot to electrode-1. By this way, it is confirmed that the present simulation adequately detects Coulomb blockade, even though we do not use capacitance of dot. Finally, Fig. 10 shows the result with Coulomb blockade at high electric field. The $V_g = 3$ V (fixed), $N = 3$ (initial), the diameter of dot is 0.6 nm ($\emptyset = 0.6$ nm), the center of dot is (0.5, 0.5, 0.5 nm), the size of the simulation structure is (1, 1, 1 nm), the top of this structure is covered by electrode-1 on which V_g is applied, and the bottom is covered by electrode-2, which is grounded. The oscillation occurs between $N = 0$ and $N = 1$, even though Coulomb blockade is considered. This is because $V_{\rm dot}$ is positive in both cases of $N = 0$ and $N = 1$. As a result, $N = 0$ and $N = 1$ are alternatively repeated and then electron hops from electrode-2 to dot and subsequently from dot to electrode-1. This is the tandem (sequential) tunneling, which is similar to trap-assisted tunneling. Note here that 0.6 nm is much smaller than dot. It can be, therefore, regarded that trap-assisted tunneling occurs at high electric field and is prohibited at low electric field owing to Coulomb blockade.

IV. Discussion

The dwell time used here is the same idea with the electron capture time constant in [41]. We used the dwell time to notch

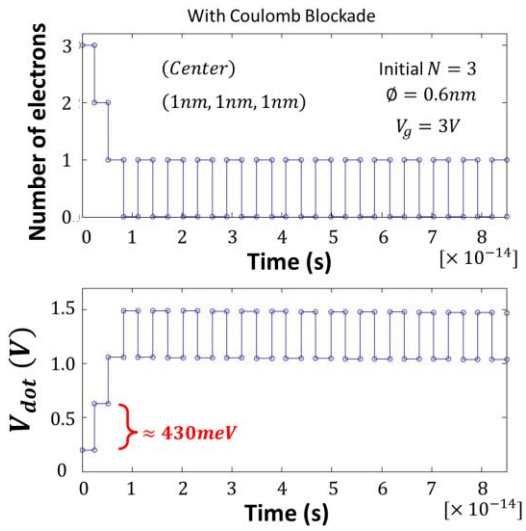

Fig. 10. Demonstration of transient simulation using dwell time as time to notch the next tunneling. The Coulomb blockade is considered. The diameter of dot is 0.6 nm. The gate voltage is high (3.0 V).

time progress and thereby simulated the discontinuous transport by hopping via floating dot. Note that the most possible tunnel path was selected at the obtained potential profile, via which an electron hops and then defined the dwell time. In the oscillation shown in Fig. 10, the obtained dwell times are constants (3.0×10^{-15} s in $N = 0$ and 2.9×10^{-15} s in $N = 1$). However, more precisely, a tunnel path should be probabilistically selected by taking into consideration the superiority and the inferiority in probability. In this event, the dwell time had to be quantum mechanically fluctuated, which was neglected in this paper.

We demonstrate the simulation of floating island with $\emptyset$ being from 6 to 0.6 nm, to emphasize that the kicking algorithm is useful to calculate the self-potential, irrespective of the size of floating island. However, as $\emptyset$ is decreased, the band structure and the permittivity inside floating island are gradually changed [37] and then giving rise to the molecular perturbation that was ignored in this paper. We can consider that this effect should be renormalized to dwell time, since it will change the tunneling flux. The quantum mechanical fluctuation and the molecular perturbation may result in the dispersion of dwell time.

The electrodes are regarded as plates (with thickness being zero), at which the voltage is applied, in the present form of this paper. The applied voltage defines the Dirichlet condition for solving the Poisson equation. Of course, this is a naïve simplification since the electrodes have more impact on tandem tunneling via smaller floating island. For example, electrons should be given by an electrode and absorbed by another electrode, in order for continuing the tandem tunneling. The Neumann condition is not suitable to model this phenomenon. We need to model the electrode in a more sophisticated fashion, but it is still not easy.

In the present demonstration, the estimation of $\hbar/(2|\delta E|)$ is less than the estimated dwell time. Therefore, it is regarded that the Coulomb blockade prohibits the tandem tunneling when the negative energy loss occurs. However, as mentioned above, the dwell time discussed here should be regarded as average. If quantum mechanical fluctuation causes the dwell time to be shorter than $\hbar/(2|\delta E|)$, then the tunneling electron can borrow the energy by δE.

The remaining issues mentioned earlier will be left for future investigations.

V. Conclusion

We successfully removed the ambiguous fitting parameter (capacitance of very small floating island) from the device modeling of very small floating island. This may stimulate a fruitful discussion about the device modeling of nanoscale electron devices. The present simulation method is composed of the kicking algorithm and the shortest dwell time (i.e., like a semiclassical approximation of tunnel path integral). As a result, Coulomb blockade of very small floating island is successfully simulated, even though the capacitance of the dot is not used. It is also found that the trap-assisted tunneling can occur at high electric field and is prohibited by Coulomb blockade at low electric field.

Acknowledgment

The authors would like to thank V. Lin and A. Lee for refining the tool of meshing the device structure. V. Lin also reviewed the manuscript.

References

[1] M. H. Devoret and H. Grabert, "Introduction to single charge tunneling," in *Single Charge Tunneling Coulomb Blockade Phenomena in Nanostructures*, vol. 294, H. Grabert and M. H. Devoret, Ed. Bergzabern, Germany: NATO, 1992, ch. 1.

[2] H. Park, J. Park, A. K. L. Lim, E. H. Anderson, A. P. Alivistatos, and P. L. McEuen, "Nanomechanical oscillations in a single-C60 transistor," *Nature*, vol. 407, pp. 57–60, Jun. 2000.

[3] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, "Room-temperature single-electron memory," *IEEE Trans. Electron Device*, vol. 41, no. 9, pp. 1628–1638, Sep. 1994.

[4] H. Watanabe, "Hopping transport of electrons via Si-dot," in *Simulation of Semiconductor Process and Devices*, vol. 12, T. Grasser and S. Selberherr, Eds. New York, NY, USA: Springer-Verlag, 2007, pp. 249–252.

[5] C. J. Gorter, "A possible explanation of the increase of the electrical resistance of thin metal films at low temperatures and small field strength," *Physica*, vol. 17, no. 8, pp. 777–780, 1951.

[6] T. A. Fulton and G. J. Dolan, "Observation of single-electron charging effects in small tunnel junctions," *Phys. Rev. Lett.*, vol. 59, no. 1, pp. 109–112, 1987.

[7] L. J. Geerlings, V. F. Anderegg, P. A. M. Holweg, and J. E. Mooij, "Frequency-locked turnstile device for single electrons," *Phys. Rev. Lett.*, vol. 64, pp. 2691–2694, May 1990.

[8] E. Leobandung, L. Guo, Y. Wang, and S. Y. Chou, "Observation of quantum effects and coulomb blockade in silicon quantum-dot transistors at temperatures over 100K," *Appl. Phys. Lett.*, vol. 67, pp. 938–940, Jun. 1995.

[9] N. M. Zimmerman, A. Fujiwara, H. Inokawa, and Y. Takahashi, "Electrostatistically gated Si devices: Coulomb blockade and barrier capacitance," *Appl. Phys. Lett.*, vol. 89, no. 1, pp. 052102-1–052102-2, 2006.

[10] K. Nakazato and H. Ahmed, "The multiple-tunnel junction and its application to single-electron memory and logic circuits," *Jpn. J. Appl. Phys.*, vol. 34, no. 2B, pp. 700–706, 1995.

[11] K. Uchida, J. Koga, R. Ohba, and A. Toriumi, "Programmable single-electron transistor logic for future low-power intelligent LSI: Proposal and room-temperature operation," *IEEE Trans. Electron Device*, vol. 50, no. 7, pp. 1623–1630, Jul. 2003.

[12] K. Naruke, S. Taguchi, and M. Wada, "Stress induced leakage current limiting to scale down EEPROM tunnel oxide thickness," in *IEDM Tech. Dig.*, 1988, pp. 424–427.
[13] D. Ielmini, A. Spinelli, M. A. Rigamonti, and A. L. Lacaita, "Modeling of SILC based on electron and hole tunneling—Part I: Transient effects," *IEEE Trans. Electron Devices*, vol. 47, no. 6, pp. 1258–1265, Jun. 2000.
[14] H. Watanabe, "Transient device simulation of floating gate non-volatile memory cell with a local trap," *IEEE Trans. Electron Device*, vol. 57, no. 8, pp. 1873–1882, Aug. 2010.
[15] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "Random telegraph noise of deep-submicrometer MOSFETs," *IEEE Electron Device Lett.*, vol. 11, no. 2, pp. 90–92, Feb. 1990.
[16] W. Kim, S. Choi, J. Sung, T. Lee, C. Park, H. Ko, *et al.*, "Multi-layered vertical gate NAND flash overcoming stacking limit for terabit density storage," in *Proc. VLSI Technology Symp.*, 2009, pp. 188–189.
[17] Y. Fukuzumi, R. Katsumata, M. Kito, M. Kido, M. Sato, H. Tanaka, *et al.*, "Optimal integration and characteristics of vertical array devices for ultra-high density, bit-cost scalable flash memory," in *Proc. IEDM*, Dec. 2007, pp. 449–452.
[18] H.-T. Lue, T.-H. Hsu, Y.-H. Hsiao, S. P. Hong, M. T. Wu, F. H. Hsu, *et al.*, "A highly scalable 8-layer 3D vertical-gate (VG) TFT NAND flash using junction-free buried channel BE-SONOS device," in *Proc. VLSI Technol. Symp.*, 2010, pp. 131–132.
[19] M. Kirihara, K. Nakazato, and M. Wagner, "Hybrid circuit simulator including a model for single electron tunneling devices," *Jpn. J. Appl. Phys.*, vol. 38, no. 4, pp. 2028–2032, 1999.
[20] Y. S. Yu, J. H. Oh, S. W. Hwang, and D. Ahn, "Equivalent circuit approach single electron transistor model for efficient circuit simulation by SPICE," *Electron. Lett.*, vol. 38, no. 16, pp. 850–852, 2002.
[21] Y. S. Yu, S. W. Hwang, and D. Ahn, "Transient modeling of single-electron transistors for efficient circuit simulation by SPICE," *IEE Proc. Circuits Devices Syst.*, vol. 1, no. 3, pp. 691–696, Dec. 2005.
[22] K. Miyaji, M. Saitoh, and T. Hiramoto, "Compact analytical model for room-temperature-operating silicon single-electron transistors with discrete quantum energy levels," *IEEE Trans. Nanotechnol.*, vol. 5, no. 3, pp. 167–173, May 2006.
[23] L.-W. Wang and A. Zunger, "Dielectric constants of silicon quantum dots," *Phys. Rev. Lett.*, vol. 73, no. 7, pp. 1039–1042, 1994.
[24] M. Macucci, K. Hess, and G. J. Iafrate, "Electronic energy spectrum and the concept of capacitance in quantum dots," *Phys. Rev. B*, vol. 48, no. 1, pp. 17354–17363, 1993.
[25] M. Macucci, K. Hess, and G. J. Iafrate, "Simulation of electronic properties and capacitance of quantum dots," *J. Appl. Phys.*, vol. 77, no. 7, pp. 3267–3276, 1995.
[26] M. Macucci and K. Hess, "Shell-filling effects in circular quantum dots," *VLSI Des.*, vol. 8, nos. 1–4, pp. 443–447, 1998.
[27] A. Kumar, S. E. Laux, and F. Stern, "Electron states in GaAs quantum dot in a magnetic field," *Phys. Rev. B*, vol. 42, no. 8, pp. 5166–5175, 1990.
[28] M. Madheswaran and K. R. Kavitha, "3D numerical modeling of quantum dot using Homotopy analysis," *J. Comput. Electron.*, vol. 12, no. 3, pp. 526–537, 2013.
[29] K. Nakazato, R. J. Blaikie, J. R. A. Cleaver, and H. Ahmed, "Single-electron memory," *Electron. Lett.*, vol. 29, no. 4, pp. 384–385, 1993.
[30] L. Guo, E. Leobandung, and S. Y. Chou, "A room-temperature silicon single-electron metal-oxide-semiconductor memory with nanoscale floating-gate and ultranarrow channel," *Appl. Phys. Lett.*, vol. 70, no. 7, pp. 850–852, 1997.
[31] L. Guo, E. Leobandung, and S. Y. Chou, "A silicon single-electron transistor memory operating at room temperature," *Science*, vol. 275, no. 1, pp. 694–651, 1997.
[32] A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, "Room temperature operation of Si single-electron memory with self-aligned floating dot gate," *Appl. Phys. Lett.*, vol. 70, no. 13, pp. 1742–1744, 1997.
[33] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee, "Room temperature operation of a quantum-dot flash memory," *IEEE Electron Device Lett.*, vol. 18, no. 6, pp. 278–280, Jun. 1997.
[34] G. Iannaccone, A. Trellakis, and U. Ravaioli, "Simulation of a quantum-dot flash memory," *J. Appl. Phys.*, vol. 84, no. 9, pp. 5032–5036, 1998.
[35] A. Thean and J. P. Leburton, "Three-dimensional self-consistent simulation of silicon quantum-dot floating-gate flash memory device," *IEEE Electron Device Lett.*, vol. 20, no. 6, pp. 286–288, Jun. 1999.
[36] D. Kahng and S. M. Sze, "A floating gate and its application to memory devices," *Bell. Syst. Tech. J.*, vol. 46, no. 6, pp. 1288–1295, 1967.
[37] H. Watanabe, K. Kawabata, and T. Ichikawa, "A tight-binding method study of optimized Si-SiO_2 system," *IEEE Trans. Electron Device*, vol. 57, no. 11, pp. 3084–3091, Nov. 2010.
[38] J. Robertson, "Defect mechanisms in a-SiO_2," *Phil. Mag. B*, vol. 52, no. 3, pp. 371–377, 1985.
[39] F. Giustino, P. Umari, and A. Pasquarello, "Dielectric discontinuity at interfaces in the atomic-scale limit: Permittivity of ultrathin oxide films on silicon," *Phys. Rev. Lett.*, vol. 91, no. 1, pp. 267601-1–267601-4, 2003.
[40] W. A. Harrison, "Tunneling from an independent-particle point of view," *Phys. Rev.*, vol. 123, no. 1, pp. 85–89, 1961.
[41] G. Molas, D. Deleruyelle, B. De Salvo, G. Ghibaudo, M. Gely, S. Jacob, *et al.*, "Impact of few electron phenomena on floating-gate memory reliability," in *IEDM Tech. Dig.*, 2004, pp. 877–880.

Hiroshi Watanabe (M'11–SM'12) was born in Gunnma, Japan. He received the B.Sc., M.Sc., and Ph.D. degrees in theoretical physics from the University of Tsukuba, Tsukuba, Japan, in 1989, 1991, and 1994, respectively.

He has been a Tenure-Track Faculty Full Professor with the Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, since 2010, and a Chair Professor with Phison Electronics Corporation, Miaoli, Taiwan, since 2011.

Kira (Chih-Wei) Yao was born in Taichung, Taiwan. He received the B.Sc. degree in electrical engineering from National Taiwan University, and the M.Sc. degree in communication engineering from National Chiao Tung University, in 2011 and 2013, respectively. He is currently pursuing the Ph.D. degree.

His current research interests include the physical simulation technique related to nanoscale electron devices. He is currently developing the General-Purpose Nano-Device Simulator.

Jerry (Po-Jui) Lin was born in Kaohsiung, Taiwan, in 1987. He received the B.Sc. degree in industrial technology education from National Taiwan Normal University, Taipei, Taiwan, and the M.Sc. degre in device physics from National Chiao Tung University, Hsinchu, Taiwan, in 2009 and 2012, respectively, where he is currently pursuing the Ph.D. degree with the Institute of Communications Engineering.

His research interests include the simulation of nanoscaled semiconductor devices.