Simulation and Investigation of Random Grain-Boundary-Induced Variabilities for Stackable NAND Flash Using 3-D Voronoi Grain Patterns

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***Abstract*— This brief investigates the random grain-boundary (GB)-induced variability in poly-crystalline silicon thin-film transistor for stackable NAND flash applications using 3-D Voronoi grain patterns. Compared with the 1-D and 2-D methods, the 3-D Voronoi grain can show a more realistic threshold-voltage variability when devices are downscaled along the channel height (H_{ch}) direction. Therefore, a full 3-D consideration is needed when modeling the random GB-induced variation.**

***Index Terms*— 3-D NAND, grain boundary (GB), variability, Voronoi.**

I. Introduction

TO ACHIEVE higher data storage density, NAND flash memories have been aggressively scaled down. Building 3-D array for NAND flash memories with multilayers and few critical process steps is one way to pursue higher bit density and lower bit cost simultaneously [1]. Various 3-D NAND flash array structures have been proposed recently [2]–[6]. However, these 3-D structures may suffer significant variability because most of them adopt poly-crystalline silicon (poly-Si) channel, which possesses random traps [7]. It has been reported that the random trap fluctuation has a noticeable influence on the threshold-voltage (V_T) distribution [8]. Therefore, an adequate modeling of the trap states in poly-Si is crucial to analyzing the device characteristics. To investigate the V_T fluctuations, poly-Si channel was modeled as Si material with traps introduced uniformly throughout the channel in the past [9]. This modeling method may be accurate for large devices possessing many grains in the active region. However, as the device size downscales, this model fails to capture the fact that the trap states are concentrated at the Si grain boundaries (GBs). In other words, more attention on the actual locations of GBs where the device variability stems from is needed.

There are several works [7], [10]–[13], [20]–[22] engaging in modeling and simulating the effects of randomly located GBs in poly-Si channel. In [11], devices with equally spaced GBs (namely, the grain size and the shape of grains are fixed) were simulated and analyzed. In [12], a 1-D rectangular method was used to consider the Si grain size variation by assuming a Gaussian distributed grain size with a given mean value and standard deviation. In the above two methods, the GBs have always been assumed to be perpendicular to the path where carriers flow. In other words, the shape of grain is constrained as rectangles and the GB is 1-D. This assumption, however, ignores the nature of arbitrary shape of grain patterns, and is unrealistic.

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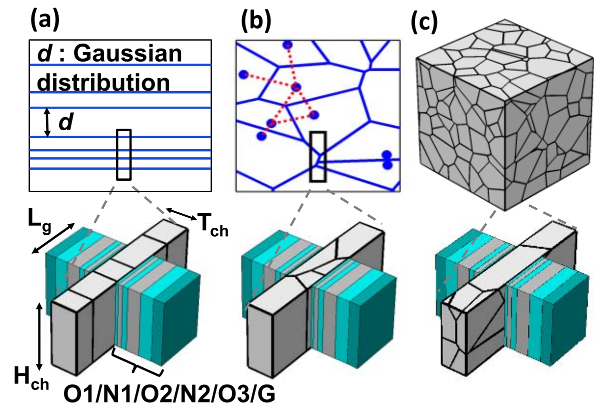

Fig. 1. Schematics for (a) 1-D rectangular [12], (b) 2-D Voronoi [13], and (c) 3-D Voronoi GBs.

In this brief, utilizing a novel 3-D Voronoi method, we investigate the GB-induced variability for 3-D NAND flash. This brief is organized as follows. In Section II, we describe our methodology to simulate random GB-induced variation. The V_T variation caused by random GBs is investigated in Section III. The conclusion is drawn in Section IV.

II. Simulation Methodology

Fig. 1 shows a summary of schematics and simulation methodologies employed in this brief. 1-D rectangular [12], 2-D Voronoi [13], [14], and 3-D Voronoi GB patterns are all performed for comparison. To reach a fair comparison, we perform 3-D simulations for both 1-D and 2-D grain patterns by extending the channel region along the width direction and redefine it as channel height (H_{ch}).

The flow chart for both 2-D and 3-D Voronoi approaches to simulate random GB-induced variation is shown in Fig. 2. The input parameter is the average grain size (d). For a given grain

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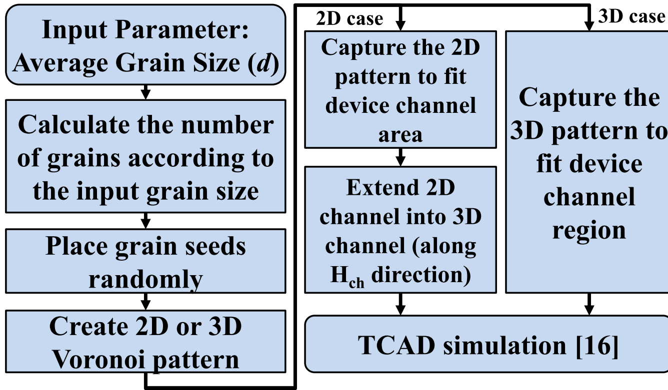

Fig. 2. Flow chart describing the 2-D and 3-D Voronoi methods for simulating poly-Si channels.

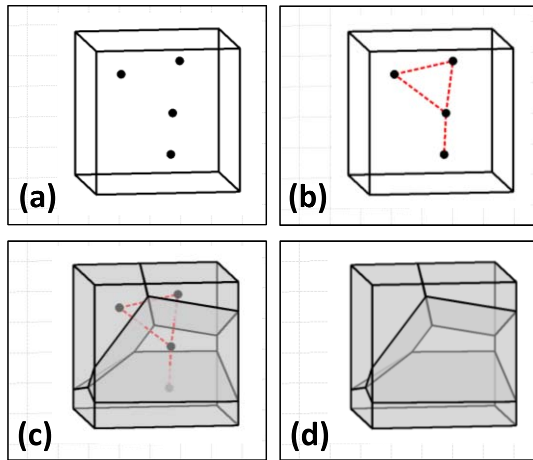

Fig. 3. Flow for constructing 3-D Voronoi patterns. (a) Randomly place grain seeds. (b) Connect every seed to its neighboring seeds (dash lines). (c) Draw perpendicular bisectors (gray planes). (d) Completed 3-D Voronoi diagram.

size, we can obtain various GB patterns by placing grain seeds randomly in a box. The number of grain seeds is determined by the following equation:

$$N = \frac{\text{box volume}}{\frac{4}{3}\pi\left(\frac{\text{grain size}}{2}\right)^3}.$$

Fig. 3 shows how the 3-D Voronoi patterns are generated. After the GB pattern is created, we capture a part of this pattern to fit in the device channel region. Finally, TCAD device simulations [16] are performed.

In our simulations, the device is designed as the junction-free BE-SONOS [6], as shown in Fig. 1. The gate-stack thicknesses for O1/N1/O2/N2/O3/G are 1.3/2/2.5/6/6/5 nm, respectively. Other pertinent parameters are listed in Table I.

A trap-concentrated GB may capture charges and form a potential barrier, which impedes free carriers [17]. Gate-induced grain barrier lowering [7] should be considered. To address the response of the current due to the lowering of energy barrier, we assume the thermionic emission transport behavior at the grain–grain interface [18]. Outside the grain–grain interface, the drift-diffusion transport is assumed. The Fermi-level pinning at GB, which has been addressed in [20] and [21], is not included in this brief.

TABLE I
DEVICE PARAMETERS USED IN THIS BRIEF

Parameter	Value
L_g	25 nm
T_{ch}	12 nm
H_{ch}	10 nm – 40 nm
grain size	100 nm
O1	1.3 nm
N1	2 nm
O2	2.5 nm
N2	6 nm
O3	6 nm
G	5 nm
channel doping, N_{ch}	n-type, 10^{16} cm^{-3}
gate doping, N_G	p-type, 10^{20} cm^{-3}

TABLE II
TRAP DENSITY PARAMETERS EXTRACTED FROM [18]

Parameter	Value
g_{TD}	8*10^{13} cm^{-2}eV^{-1}
g_{TA}	10^{14} cm^{-2}eV^{-1}
E_{TD}	60 meV
E_{TA}	90 meV

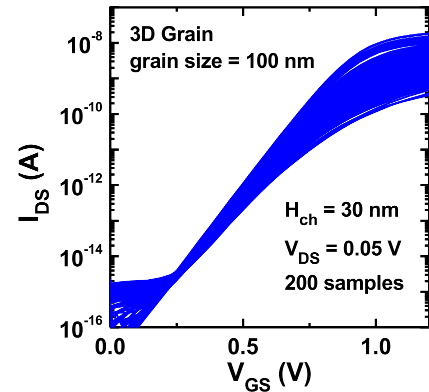

Fig. 4. Dispersion of I_{DS}–V_{GS} curves due to 3-D grain patterns.

In this brief, trap states are considered as interface traps at GBs, and no other traps are assumed outside these GBs. Besides, we assume that the trap concentrations are identical for all GBs. Trap states used in this brief are obtained from fitting the experimental data [19] with the following exponential functions:

$$g_D(E) = g_{\mathrm{TD}} \exp\left(\frac{E_V - E}{E_{\mathrm{TD}}}\right)$$
$$g_A(E) = g_{\mathrm{TA}} \exp\left(\frac{E - E_C}{E_{\mathrm{TA}}}\right)$$

where g_D and g_A are donor-like and acceptor-like densities of states, respectively. The extracted parameters for g_{TD}, g_{TA}, E_{TD}, and E_{TA} are listed in Table II.

III. THRESHOLD VOLTAGE VARIATION

Using our proposed 3-D Voronoi method, Fig. 4 shows the I_{DS}–V_{GS} dispersion with 200 random samples. In Fig. 5, the

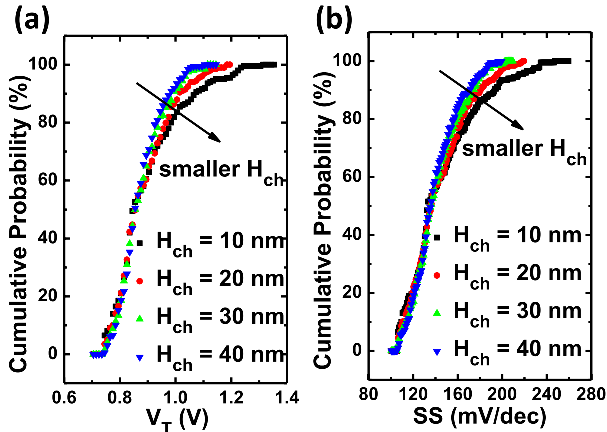

Fig. 5. Cumulative probability for (a) V_T and (b) SS for devices with various channel heights ($H_{\rm ch}$).

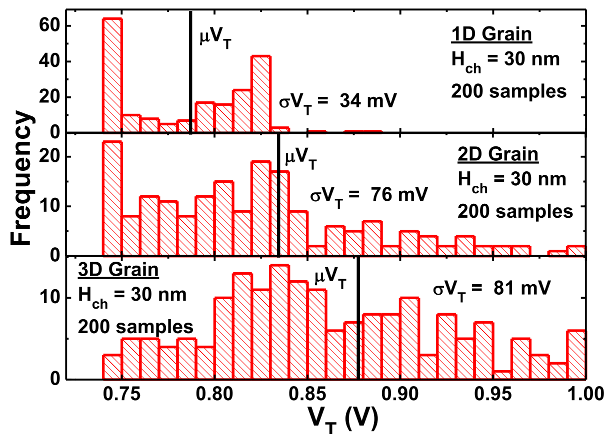

Fig. 6. V_T distributions for 1-D, 2-D, and 3-D GB patterns. The average grain size is 100 nm. Spikes are observed in both 1-D and 2-D patterns at $V_T \approx 0.75$ V.

cumulative probabilities for V_T and subthreshold swing (SS) for devices with various channel heights ($H_{\rm ch}$) are demonstrated. It can be seen that the distributions become wider as $H_{\rm ch}$ shrinks, which can be explained as follows. When the device is large, there are a large amount of GBs inside the active region and their impacts on the degree of randomness are averaged by each other. In this case, the variation only comes from the different number (number fluctuation) of GBs inside each device. However, for a given average grain size, there are less GBs inside the channel as the device shrinks. Therefore, when we consider the device variability, we should no longer ignore the impact of the actual positions and shapes of these GBs. In other words, the position and shape of GBs serve as additional variation sources in addition to the number fluctuation of GBs.

The V_T distributions from 1-D rectangular, 2-D Voronoi, and 3-D Voronoi methods are compared in Fig. 6 for devices with $H_{\rm ch} = 30$ nm. We can observe that there is an unusual spike at V_T around 0.75 V for the 1-D and 2-D grain cases. These spikes correspond to the devices that have no GBs in their channels. On the other hand, the spike disappears for the 3-D grain case because most devices possess GBs in their channel regions and hence the devices with the smallest V_T (i.e., no GB) become rare. Fig. 7 compares the $H_{\rm ch}$ dependence of V_T variations for the 1-D, 2-D, and 3-D methods. It can be seen that the 1-D and 2-D methods tend to underestimate the σV_T for devices with scaled $H_{\rm ch}$. Compared with the 1-D and 2-D grains, the 3-D grain has more freedom in varying the GB shapes, thus exhibiting a larger V_T variability. It indicates that a full 3-D GB pattern needs to be employed to accurately simulate the GB-induced variability.

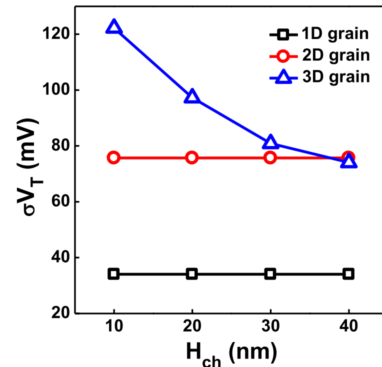

Fig. 7. Channel-height dependence of the V_T variability for 1-D, 2-D, and 3-D GB patterns.

IV. Conclusion

We have investigated the random GBs-induced variability in poly-Si thin-film transistor using 3-D Voronoi grain patterns. Compared with the 1-D and 2-D methods, the 3-D Voronoi grain can show a more realistic variability when devices are downscaled along the channel height ($H_{\rm ch}$) direction. This brief indicates that a full 3-D consideration is needed when modeling the random GB-induced threshold-voltage variation.

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