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Small-pixel TFT flaw detection and measurement using voltage imaging technique

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ABSTRACT

The paper proposed the characteristics of flaw measurement in small-pixel design mobile displays based on TFT array panel with respect to electrical-optic characterization. For advanced small-pixel and high-resolution mobile display applications, the display pixels on array process are smaller, detecting small-pixel defect played an important role than previously seen in non-small-pixel TFT array panels for managing process yield. The study resulted in small-pixel size TFT array show the flaw detection performance and preference approaches using the voltage imaging technique. It provides an initial insight into the high-resolution of small-pixel size designs for advanced mobile displays application.

1. Introduction

The general display, TFT array performance measurements include electrical characteristics tracking and flaw detection, they impact the in-process quality, manufacture cost and yield managing. Flaw detection plays a major role in mass production of quantitative visual tasks involving FPD cell testing [1].

In advanced mobile display technology have display high-resolution medical images in hand-held devices and provide healthcare enabled. However, it is necessary to determine the proper flaw detection methodology of these high-resolution displays and establish testing in-process yield requirements on the performance measures to ensure proper precision medical imaging interpretation and electrical characteristics tracking. In-process yield is an important display parameter as it affects the cost and quality seen at different positions on the display maker [2].

This measure characterizes the contamination from one pixel to neighboring pixels and defect detection for the quality of a display. This metric is particularly important when the task is to distinguish structures with subtle image [3,4]. Flaw detection is an important characteristic to measure in TFT array panels. Studies have shown that differences in-process positions relative to the testing method can severely change grayscale by the FPD testing. Thus, poor detection ability can lead to yield loss interpretation and difficult decrease controlling process accuracy especially in small-pixel flaw detection tasks [5,6].

However, because mobile displays are smaller in pixel size than normal displays. Resolution and sub-pixel structure differ greatly among display technologies. Measuring these characteristics provides information on how well the display, because current testing equipment supplier still cannot provide good solution and limit for small-pixel flaw detection in mobile display applications such as sub-pixel sized <40 μm [5–10]. The target of this paper was proposed the small-pixel flaw detection enhancement by using voltage imaging technique and corrected.

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2. Materials and methods

2.1. Flaws classification of TFT array

There are many types of flaws in a thin-film-transistor (TFT) array. All flaws can be classification into two groups, one is line defect and the other one is pixel defect. Line defect is classified according to which line is short or open. Few types of line defects are widely referred; gate open, data open, gate-to-gate short, data-to-data short, gate-to-data short, and data-to-com short. Pixel defect is conventionally classified by its defected feature; TFT gate open, TFT data open, TFT pixel open, low TFT on-current, high TFT off-current, TFT via hole missing, pixel-to-data line short, pixel-to-gate line short, storage capacitor short, pixel-to-pixel short across data line or across gate line, data line residue under pixel, and amorphous silicon residue under pixel. For better flaw detection with different configuration of TFT array panel designed, it requests a good solution each pixel design on TFT array panel.

2.2. TFT array testing

The testing operation theory is the voltage imaging technique. The measurement methodology proposed in this study is for detecting TFT array flaws. In Fig. 1, it has shown the measurement of opto-electrical transformation with TFT characterizing. The modulator will sense the induced voltage by pixels' E-fields and showed the measurement pixel voltage by opto-electrical transformation with TFT characterizing; the voltage imaging for green is good pixel and dark for bad pixel.

The bad pixels getting electrical leakage, induced pixel voltage drop caused by capacitive coupling due to data voltage drop be ΔV_{data}, and the pixel voltage drop, ΔV_{pixel} is expressed as follow Eq. (1), where C_{dp} denotes the equivalent capacitance of bad pixels getting electrical leakage, C_{st} is the capacitance of storage capacitor, and C_{gd} is the capacitance of TFT parasitic capacitor. C_{dp} is an equivalent capacitor between pixel electrode and data line through the passivation layer.

$$\Delta V_{\text{pixel}} = \frac{C_{dp}}{C_{dp} + C_{st} + C_{gd}} \cdot \Delta V_{\text{data}} \tag{1}$$

In order to reduce the measurement noise, the Voltage Imaging technology uses four image acquisition frames, a, b, c, and d, to get the pixel voltage V_{pixel}, and V_{pixel} can be calculated as follow Eq. (2), where V_a is voltage denotes the frame a of voltage image acquisition, V_b is voltage denotes the frame b of voltage image acquisition, V_c is voltage denotes the frame c of voltage image acquisition, V_d is voltage denotes the frame d of voltage image acquisition, V_{pixel} is voltage denotes the pixel voltage.

$$V_{\text{pixel}} = (V_a - V_b - V_c + V_d)/2 \tag{2}$$

With the comparison of normal and defective pixel under the driving pattern caused results. Here, the pixel voltage drop ΔV_p is induced at the defective pixel with the overlap of the pixel and data line due to the data voltage drop ΔV_d. In this case, the measured voltage of the normal pixel (V_{Normal}), the defective pixel with electrode and data line overlap (V_{Defect1}), and the leakage short with data-to-data (V_{Defect2}) are calculated as follows Eqs. (3)–(5):

$$V_{\text{Normal}} = (V_{a0} - V_{b0} - V_{c0} + V_{d0})/2 \tag{3}$$

$$V_{\text{Defect1}} = (V_{a1} - V_{b1} - V_{c1} + V_{d1})/2 \tag{4}$$

$$V_{\text{Defect2}} = (V_{a2} - V_{b2} - V_{c2} + V_{d2})/2 \tag{5}$$

Therefore, the voltage difference between the normal pixel and the defective pixel is enough large to differentiate them. The overlap capacitance is assumed for pixel electrode and data line overlap; also for the leakage short with data-to-data. It is not considered the line delay of both gate line and data line; the real whole plate might

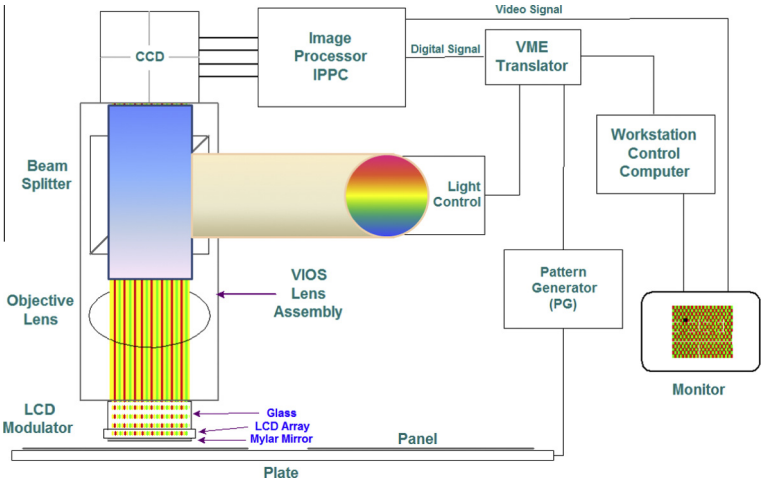

Fig. 1. Measurement system of opto-electrical transformation with TFT characterizing and pixel voltage measured by opto-electrical transformation with TFT characterizing shown on monitor.

be different from these data of the measured voltage. It might induce larger voltage drop because of larger overlap capacitance.

3. Results

Fig. 2 has shown the (a) plate, (b) TFT array panel and (c) pixel layout of the mobile display. Under a common pattern, the voltage of every pixel is same as even a pixel-to-pixel short defect has the same voltage with a normal pixel. A data line residue under pixel and an amorphous silicon residue under pixel are detected. The overlap area between the residues form a capacitor and a small voltage variation is generated in these types of defects due to this overlap capacitance. Depending on the overlap area, the variation may result in a shift of a few gray levels under a conventional 64 gray level driving scheme. The voltage step between two consecutive gray levels is around 50 mV. It should be drop down larger particle in order to detect a single defect. In order to enable detecting a pixel-to-pixel short defect and improve the small-pixel-sized defect detection capability, two adjacent pixels need to have an opposite polarity of voltage that makes the voltage of the defect to be 0 V. This is small to differentiate a defect from a small-pixel sized of sub-pixel (~39 μm). The detected natural critical small-pixel sized point defects are shown in Fig. 3. Fig. 3 shows the artificial line defect as (a) gate line open and (b) data line open were detected. Fig. 4 shows the artificial line defect as (a) data-to-common short and (b) gate-to-data short were detected. Fig. 5 shows the artificial defects were detected (a) pixel to pixel and (b) pixel point.

To detect the line defects such as gate line open, data line open and data line to common line short. It feature checks out the current between each shorting bar and finds out if any short exists between the lines. Thus, this feature reports the location of line open and short. It shows the difficult artificial line defect as gate line open, data line open, and also shows that the data line to common line short

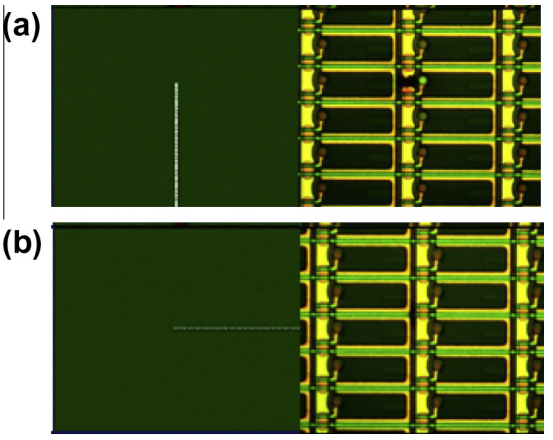

Fig. 3. The artificial line defects: (a) gate line open and (b) data line open.

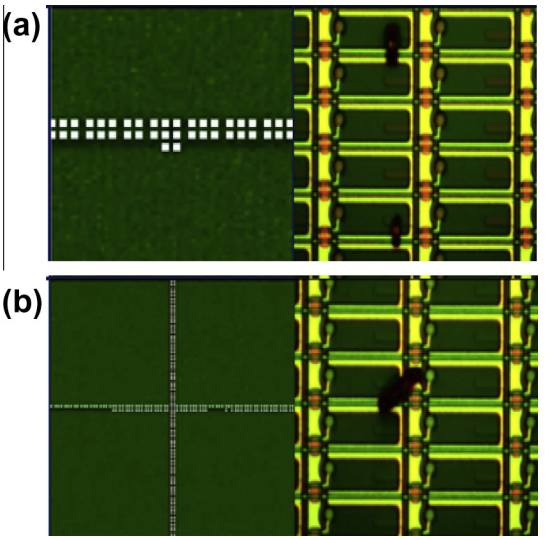

Fig. 4. The artificial line defects: (a) data-to-common short and (b) gate-to-data short.

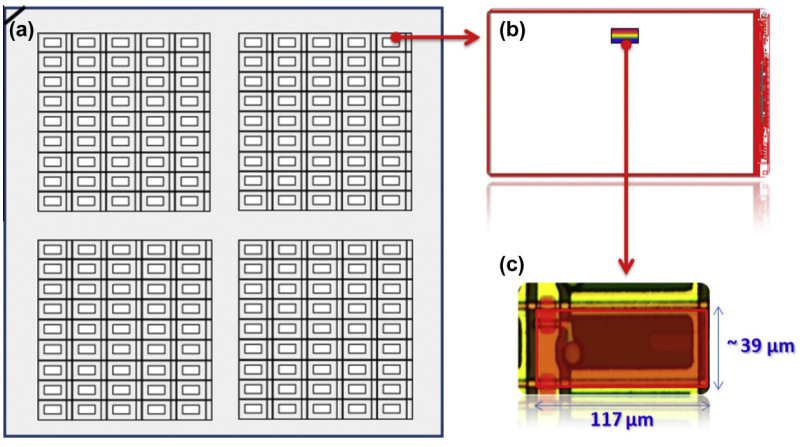

Fig. 2. (a) Plate, (b) TFT array panel and (c) pixel layout of the mobile display.

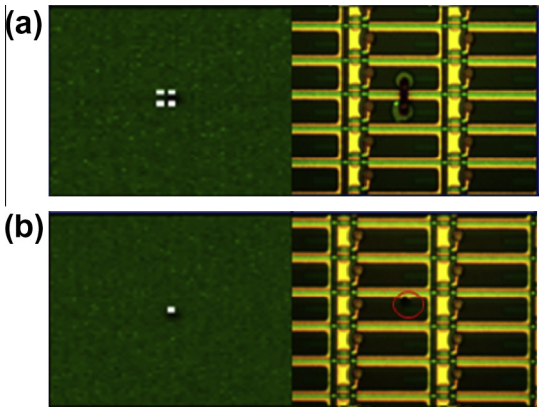

Fig. 5. The artificial point defects: (a) pixel to pixel and (b) pixel point.

were detected. Comparison with past data for small-pixel sized of TFT array flaw detection, it estimates to improve better than 30% flaw reporting that including point and line defects [5–14]. Voltage imaging also has difficulty in locating the position of the line short and open. This difficulty arises from the fact that this type of defects does not generate a sharp voltage drop and the defect location is hidden in a form of a line defect.

4. Discussion

The defect detection capability for voltage imaging technique, it depends on the panel design as well as the driving pattern. The designed shorting bar configuration provides the highest defect detection capability. The driving voltage presented in this report is just an example. It should be modified for each customer's use, because each customer has his own design parameters such as a storage capacitor capacitance, shorting bar resistance, TFT on/off current, TFT parasitic capacitance, and so on. The defect type of TFT array was reviewed and new application was developed to detect small-pixel defects. The defect detection capability was compared with various shorting bar configurations and driving schemes. Some restrictions may have TFT manufactures fabricate and design many kinds of array panel. It is very difficult to have good defect detection in a storage-on-gate mode with only one gate line and one data line panel configuration. In this case, designing a panel as a storage-on-common mode may be a better solution for defect detection than doing it as a storage-on-gate mode.

In the past, they suffer the limitation of detecting the critical defect in small-pixel sized TFT array and facing an unstable charge density and array structure with optical-sensing sensitivity issue [5,10]. The electron beam schemes only can inspect a few kinds of flaws and detected, and it also demands of high stability of the instruments and long working time for them [7]. For the electrical testing scheme requires a large number of contact pins for direct contact and measurement, it should be take higher cost, longer working-time for product-line [8]. Table 1 shown the simple comparison of small-pixel sized detection ability and performance on the in-process testing for TFT array defects. The voltage step between two consecutive gray levels is around 40 mV. This is difficult to differentiate a defect from a small-pixel-sized of sub pixel ($\sim$39 μm × 117 μm) [12–14]. Future work, it is our goal for smaller pixel sized of sub pixel flaw detection. It should be helpful reduce the manufacture cost and managing in-process yield for the medical display and advanced mobile display panel.

5. Conclusions

The proposed testing scheme can be performed without any hard contact and panel damage during in-process detection, and the in situ measurement can be taken in real time with high stability and capacity. The results presented here is including critical pixel electrical leakage defect, and is useful in identifying the causes of array defects on the in-process small pixel panels testing. Furthermore, the TFT array testing can be applied into the in-line testing of TFT array process for IGZO-based with TFT-LCD and AMOLED. It's enhancing the testability of small sized pixel TFT array and high-resolution mobile display panels' inspection. An effective electrical testing scheme depends on the configuration of pixel circuit and panel design by using this proposed testing, the function of all devices such as TFT and Array can be examined defects with fully test before the back end of process is performed.

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Table 1
The comparison of small-pixel sized detection ability and performance.

TFT-Array-Testing	Optical sensing	Electron beam	Electrical testing	Voltage imaging
Small-pixel sized (32 μm < x < 55 μm)	△	○	△	◎
Low tooling cost	△	○	△	○
High detection rate	○	○	○	◎
Stable measurement	△	△	◎	◎
Short working time	○	△	△	◎

◎: Good, ○: Normal, △: Poor

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