A Switchable Digital–Analog Low-Dropout Regulator for Analog Dynamic Voltage Scaling Technique

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***Abstract*—Dual dynamic voltage scaling (DVS) techniques employed in single-inductor dual-output (SIDO) converters are used to improve the efficiency of the system-on-a-chip (SoC). One DVS technique for digital circuits is controlled by the SoC processor. This paper presents the analog DVS (ADVS) technique for analog circuits to scale voltage across the power MOSFET of the switchable digital–analog (D/A) low-dropout (LDO) regulator which is the post-regulator cascaded in series with the SIDO converter. The ADVS determines the tradeoff between voltage suppression and efficiency. Furthermore, because of the digital operation of the D/A LDO regulator, the quiescent current is further reduced at light loads while the load current requirement is minimized. In addition, the limitation of the capacitor-free LDO is significantly reduced by a few microamperes. The test chip was fabricated using a 40-nm CMOS process. Experimental results demonstrated switchable D/A LDO regulator operation with peak efficiency at 96.7% in analog operation and a 5-mV output voltage ripple at 120-mA load resulting from the advantage of ripple suppression. The power efficiency could be sustained at a value over 92.57% even when the load current decreased to 1 μA.**

***Index Terms*—Asynchronous digital low-dropout (LDO) regulator, bidirectional asynchronous signal pipeline, dynamic voltage scaling (DVS), hybrid operation, million instructions per second performance, power conversion efficiency, power module, ripple-based control, switching regulator.**

I. Introduction

POWER management is an essential system-on-a-chip (SoC) design issue that requires distributive voltage and current levels for distinct subcircuits. SoC power management requires area efficiency. The single-inductor dual-output (SIDO) converter shown in Fig. 1(a) can power both analog and digital circuits in the SoC by employing two distinct output voltages with only one off-chip inductor [1]–[3] to effectively reduce the print circuit board (PCB) area. Specifically, the volume and cost of manufacturing portable electronics can be reduced.

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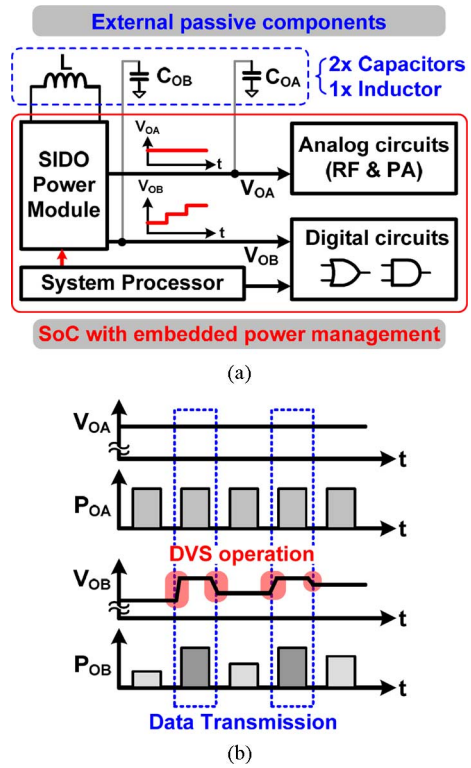

Fig. 1. (a) The SoC merges with the integration of SIDO power module, which provides two distinct supply voltages, V_{OA} and V_{OB}, to digital and analog circuits, respectively. (b) Scalable voltage at the V_{OB} corresponding to the SoC operation compared with the fix voltage at the V_{OA}.

Power reduction ability is another necessary feature of power management. Dynamic voltage scaling (DVS) is the most efficient technique for power reduction. Moreover, the system processor can send the voltage indication signal to the SIDO converter to adjust one of two output voltages as one DVS-based power management. The DVS function is generally implemented in digital blocks because digital circuit power consumption is also optimized by the different operation instructions or tasks in SoC [4]–[9].

As shown in Fig. 1(b), if the SoC enters into the data transmission operation, the increase of V_{OB} meets the SoC speed requirement. The decrease of V_{OB} also conserves power when the data transmission ends. Comparatively, analog circuits cannot use the similar DVS technique in digital circuits because the supplying voltage for analog circuits should be kept

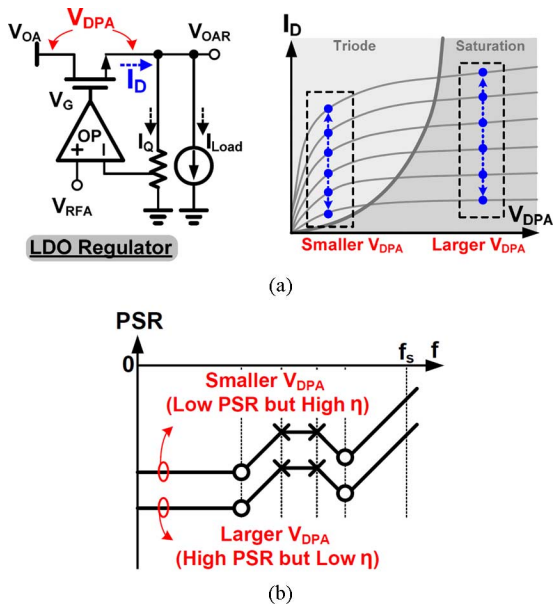

Fig. 2. (a) The dropout voltage V_{DPA} of the LDO regulator. (b) The relationship between the dropout voltage V_{DPA} and the PSRR.

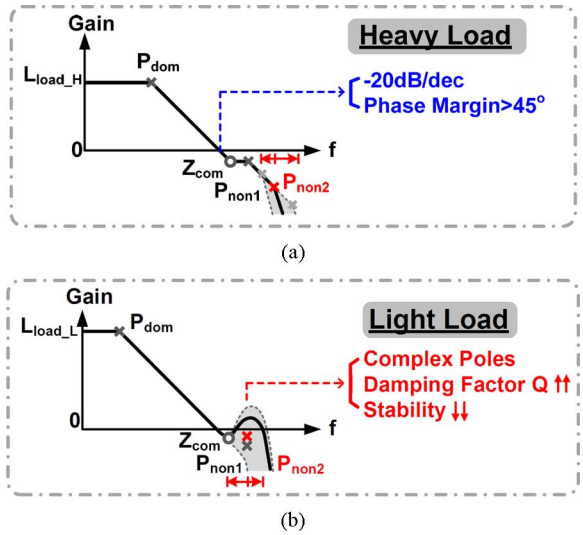

Fig. 3. Analysis of capacitor-free LDO regulator. (a) Frequency response at heavy loads. (b) Frequency response at light loads.

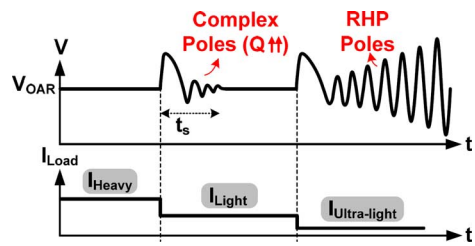

Fig. 4. Unstable phenomena of LDO regulator caused by load current limitation in case of heavy-to-light load change of capacitor-free design.

constant to maintain some important performance. In addition, the switching voltage ripple at the V_{OA} will degrade accuracy and power supply rejection ratio (PSRR). Consequently, one low-dropout (LDO) regulator cascaded in series with the SIDO converter is needed to supply voltage to analog circuits with voltage ripples smaller than those at the V_{OA}. Moreover, the improved voltage ripple suppression results in a larger dropout voltage across the pass transistor of the analog LDO regulator because the dropout voltage is considered as a buffer between input supply voltage and output voltage. Fig. 2 illustrates the relationship between dropout voltage V_{DPA} and the current across and through the power MOSFET of the analog LDO regulator, respectively.

When the analog LDO regulator operates with smaller dropout voltage, power supply rejection (PSR) negatively escalates alongside the acquisition of higher power efficiency. This condition occurs because the power MOSFET in the triode region rather than the voltage control current source in the deep saturation region exhibits a resistive characteristic. By contrast, larger dropout voltage across the power MOSFET can help improve PSR while simultaneously deteriorating power efficiency. The power MOSDET dissipates large power loss. The new definition of analog-DVS (ADVS) technique for analog circuits is to dynamically scale the dropout voltage V_{DPA} according to the loading condition and to maintain constant V_{OAR} for analog circuits. In other words, the proposed ADVS technique determines the tradeoff between efficiency and output voltage ripple without affecting the performance of analog circuits in the SoC [10].

Moreover, the LDO regulator design that meets the area efficiency demand as a cascading regulator in series with the SIDO converter may require capacitor-free architecture. Thus, similar to the illustration in Fig. 1, three external passive components, two capacitors and one inductor, are retained. The embedded capacitor-less LDO regulator in the SoC has the advantage of removing the external output capacitor. However, the high quiescent current drastically deteriorates power efficiency compared with the LDO design with the dominant pole compensation. The capacitor-free LDO regulator also encounters obstacles in stability and restrictions in driving capability. In response to the disadvantages in the capacitor-free LDO design, the system should dissipate a minimum load current to ensure the stability of light load condition. Generally, 50 to 100 μA are required at light loads and further decrease power efficiency.

In this paper, the LDO regulator is cascaded in series with one of the two SIDO converter outputs and designed as a switchable digital–analog (D/A) LDO regulator that supplies analog circuits in the SoC. The advantages are as follows. In the analog operation of the D/A LDO regulator, adjusting the dropout voltage corresponding to the loading condition provides the function of ADVS. Proper dropout voltage is obtained to achieve a regulated output voltage with ripple suppression and power loss reduction. By contrast, digital operation of the D/A LDO regulator reduces the minimum load current requirement to a value near zero [11]. Meanwhile, the dropout voltage is continuously minimized for power optimization. Therefore, the proposed switchable D/A LDO regulator ensures high efficiency over a wide load range and employs the ADVS technique to supply analog circuits.

In this paper, power management using the dual DVS functions for the SoC improves performance in both digital and

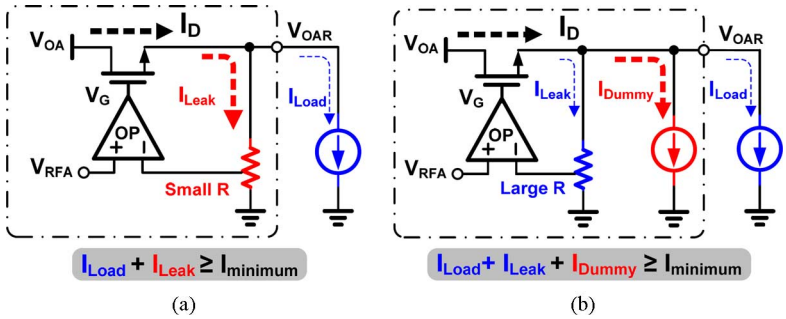

Fig. 5. Conventional solution for alleviating minimum load limitation in the capacitor-free LDO regulator. (a) With an increased quiescent current. (b) With an extra dummy load current.

analog blocks. This paper is organized as follows. The analysis of the analog capacitor-free LDO regulator is discussed in Section II. ADVS function operations with the switchable D/A LDO regulator are examined in Section III. Circuit implementations are presented in Section IV. Experimental results are reported in Section V. Finally, conclusions are given in Section VI.

II. Analysis of Analog Capacitor-Free LDO Regulator

The analog LDO regulator with Miller compensation is called capacitor-less design. This design has only one small output capacitor to prevent large dip voltage in case of load changes. Thus, the capacitor-less design is more suitable for SoC integration because of the absence of a large output capacitor [12]–[17]. A small integrated output capacitor removes the need for an extra pin for the output capacitor and, thus, has the advantage of reducing volume and cost. However, the bottleneck of the capacitor-free LDO regulator refers to the minimum load current ($I_{\rm minimum}$) requirement used to avoid unstable occurrences at light loads. The minimum load current requirement seriously degrades power conversion efficiency at light loads or no load condition.

As shown in Fig. 3, the bandwidth (BW) of the capacitor-free LDO regulator is almost constant over a wide load current range. On-chip Miller compensation generates low-frequency pole and zero, $P_{\rm dom}$ and $Z_{\rm com}$, respectively. In addition, the high-frequency nondominant poles $P_{\rm non1}$ and $P_{\rm non2}$ are located at the gate of the power MOSFET and the output node, respectively. The $P_{\rm non2}$ is dependent on the load current. More specifically, the $P_{\rm non2}$ moves toward lower frequencies because of increased equivalent output resistance resulting from the decreased load current. Once the $P_{\rm non2}$ approaches the $P_{\rm non1}$, the increasing damping factor Q seriously deteriorates system stability. From the perspective of the S-domain, the complex poles generate when two non-dominant poles collide with each other and split out of real axis. Even at ultralight loads, the complex poles move to the right half plane (RHP) and cause an unstable oscillation. As shown in Fig. 4, an unexpected phenomenon occurs in cases of different load transient step variations. Output voltage ringing and long settling time (t_s) during the transient period are caused by insufficient PM, which result from the complex poles in the capacitor-free LDO regulator.

Even though several techniques in previous literatures propose a decrease in the minimum load current, the minimum load current retains tens or hundreds of microamperes [13], [18]. Therefore, efficiency is restricted because of increased leakage current (I_{Leak}) or dummy load current ($I_{\rm Dummy}$) payments to meet minimum load current requirements, as shown in Fig. 5 [19]–[22]. Although the ultralight load demands when the SoC system enters into standby mode, the squandered current through power MOSFET remains large and results in substantial power loss, as indicated in Fig. 5. The situation shortens the battery usage time for portable devices. Furthermore, without the assistance of an output capacitor in case of load transient periods, good transient response requires a large amount of quiescent current to achieve low impedance and a high slew rate (SR). Thus, current efficiency is poor at light loads if the minimum load current requirement does not decrease.

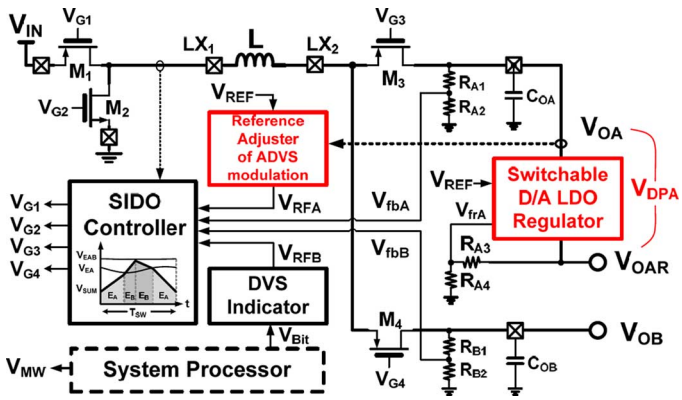

Fig. 6. Structure of the proposed SIDO power module for dual DVS functions.

In order to extend load current to be lower than the minimum load current defined by conventional capacitor-free LDO regulator, the D/A LDO regulator is switched from the analog operation to the digital operation. Thus, the digitally operating LDO regulator confirms stability under a no-load condition while consuming only 50 nA of quiescent current on the controller and only 0.5 μA of current on the resistor divider. By contrast, the current flowing through the resistor divider and quiescent current are equal to tens or hundreds of microamperes in the prior arts. In other words, the digital operation in the D/A switchable LDO regulator breaks through the limitations of the minimum load current. In turn, high current efficiency is achieved over a wide load current range with a compact-size solution for SoC power management.

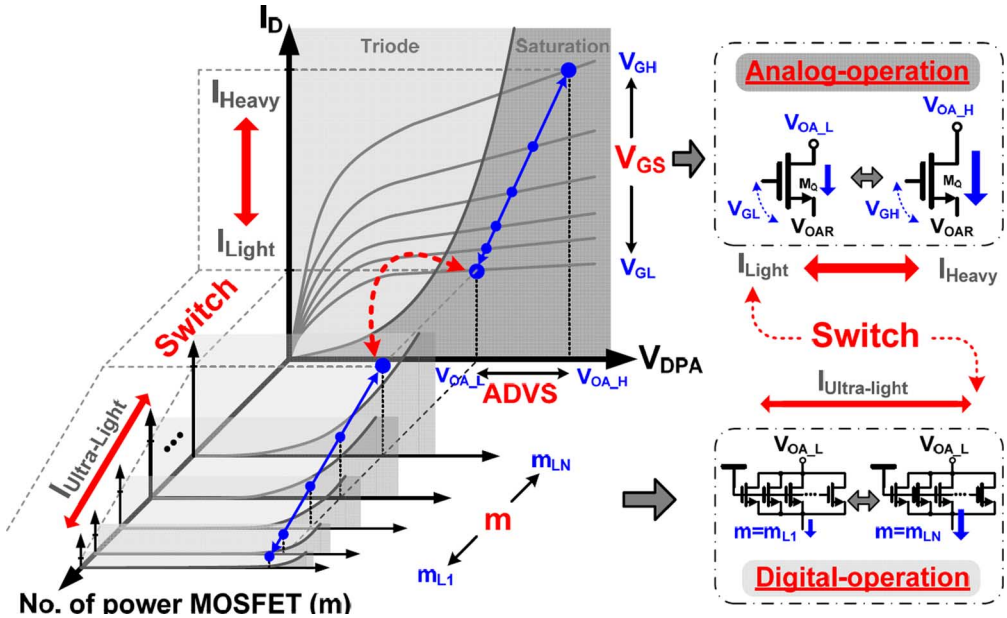

Fig. 7. I–V characteristic of the switchable function in analog operation and digital operation.

III. Operation of the ADVS Function With the Switchable D/A LDO Regulator

With regard to power management using the dual DVS technique in the SoC, the proposed SIDO power module shown in Fig. 6 has two outputs. One output is for digital circuits and the other, with the switchable D/A LDO regulator, is for analog circuits in the SoC. With only one off-chip inductor, the power stage of the SIDO converter is composed of four power switches from M_1 to M_4. These switches transfer the energy from the input battery to both outputs V_{OA} and V_{OB}. The V_{OB} directly supplies digital circuits in the SoC. In DVS operation, the DVS indicator receives the control signal $V_{\rm Bit}$ from the system processor to generate the reference voltage V_{RFB} for the V_{OB}. By contrast, the switchable D/A LDO regulator is cascaded in series with the V_{OA} of the SIDO converter to guarantee the supply quality for the analog circuits.

When the D/A LDO regulator is operated using the analog function, the load current condition at the V_{OA} is reflected to the reference adjuster of ADVS modulation to dynamically adjust the dropout voltage, which subsequently leads to voltage ripple suppression or power conservation. If the output load condition at the V_{OA} continuously decreases to an ultralight condition, the switchable D/A LDO regulator is switched to digital operation. Thus, quiescent current decreases because of digital controller and dropout voltage is minimized to further enhance the power efficiency. The load-dependent technique indicates the switching procedure between analog and digital operations in the switchable D/A LDO regulator. Therefore, with the feedback control loop in the SIDO power module, the ADVS and DVS functions are achieved at the V_{OA} and the V_{OB}, respectively. The SIDO controller uses the current-programmed control scheme [3] to realize the energy delivery function at the power stage and ensure high power efficiency.

The concept of a switchable D/A LDO regulator is illustrated by the I–V characteristic in Fig. 7. According to the load current from the SoC power demand, the analog or the digital operation is activated to ensure voltage regulation and to achieve high power efficiency. Analog operation uses the ADVS function that adjusts the adaptive dropout voltage through cooperation with the SIDO converter.

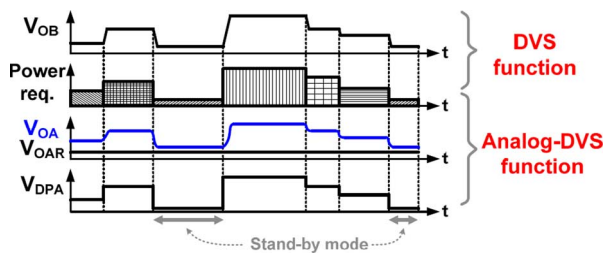

Fig. 8. Operations of both the DVS function for digital circuits and the ADVS function for analog circuits in the proposed SIDO converter.

The I–V characteristic of power MOSFET is controlled by an error amplifier and shows the parabolic curve between the triode region and the saturation region according to

$$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right){V_{OV}}^2(1+\lambda V_{\rm DS}),\ V_{\rm DS} \geq V_{OV}. \quad (1)$$

Under the critical condition in which $V_{\rm DS}$ is equal to V_{OV}, the following equation shows that $V_{\rm DS}$ is proportional to the square of the drain current I_D while neglecting channel length modulation parameter λ:

$$V_{\rm DS} = V_{OV} \propto \sqrt{I_D}. \quad (2)$$

Consequently, as the load decreases, a smaller dropout voltage is required to ensure proper functioning of the power MOSFET in the saturation region for good voltage ripple suppression. Therefore, small dropout voltage eliminates the superfluous conduction loss on the power MOSFET and enhances conversion.

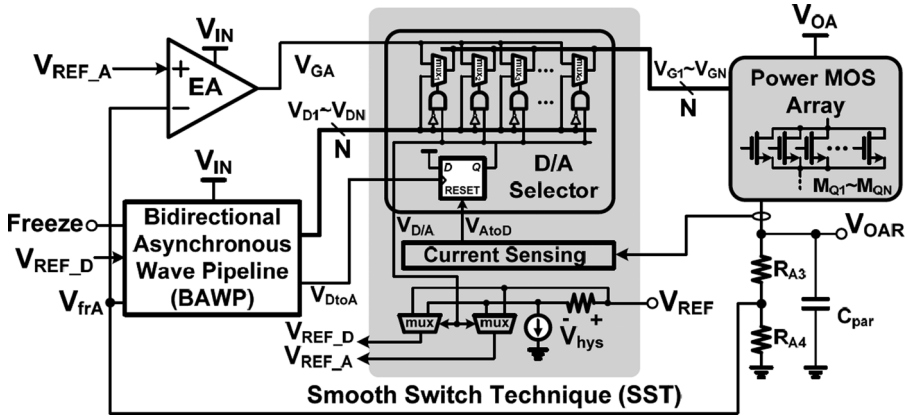

Fig. 9. Schematic of the switchable D/A LDO regulator.

At ultralight loads, the pole at the output moves toward the origin and stability decreases drastically. Without the help of the dummy load current, the power MOSFET is modulated by the digital controller rather than the analog controller (the error amplifier) to significantly decrease the quiescent current. Thus, the digital operation of the D/A LDO regulator breaks through the limitations of minimum load current for the capacitor-free LDO regulator. An advantage is that the digital controller features low quiescent current and further enhances power conversion efficiency.

The right-hand side of Fig. 7 illustrates the operating behavior of the power MOSFET M_Q in either analog or digital operation. In particular, the error amplifier controls M_Q to determine an adequate gate voltage level that corresponds to the load current condition. Moreover, because of the regulated output voltage V_{OAR} of the D/A LDO regulator, the load current adjusts the dropout voltage to determine the adequate output voltage V_{OA} of the SIDO converter. When the load condition changes from heavy to light, the V_{OA} changes from V_{OA_H} to V_{OA_L} and obtains a smaller dropout voltage while simultaneously decreasing the gate voltage level from V_{GH} to V_{GL} for appropriate driving capability. If the load current decreases under certain value, the analog operation switches to digital operation.

During the digital operation, the transistor M_Q is divided into several parallel sub-MOSFET units (SMUs). Portions of SMUs are turned on and off by the digital controller according to load current. The number of turn-on SMUs is denoted as m. When the load current decreases continuously, the value of m shrinks ($m_{L1} < m_{L2} < m_{L3} \cdots < m_{LN}$ in Fig. 7). Thus, the switchable D/A LDO regulator uses both analog and digital operation suitable to the demand for analog circuits in the SoC.

Fig. 8 illustrates the operations of both the DVS function for digital circuits and the ADVS function for analog circuits achieved via the switchable D/A LDO regulator. When the SoC enter into operating mode, the DVS function indicated by the system processor is activated to optimize the power consumption. The ADVS function also enables the dynamic adjustment of the dropout voltage of the LDO regulator to guarantee high power conversion efficiency. More specifically, the output voltage level of SIDO power module V_{OA} is adjusted according to the load current condition at the V_{OAR}. Moreover, the switchable D/A LDO regulator using the digital operation

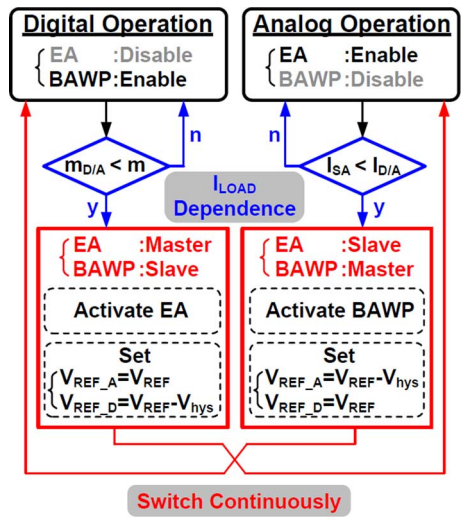

Fig. 10. Flowchart of the switchable technique.

once the SoC enters into silent or standby mode. Although the capability of ripple suppression decreases, dropout voltage is reduced to a relatively small value for energy-efficient operation.

IV. Circuit Implementation

A. Switchable Digital-or-Analog LDO Regulator

A schematic of the proposed switchable D/A LDO regulator is depicted in Fig. 9 and exhibits the digital and analog operations. These two operations indicate that SMUs are controlled by the bidirectional asynchronous wave pipeline (BAWP) [23] and the error amplifier (EA) [24], respectively. In this case, the smooth switch technique (SST) decides whether digital or analog operation is to be used with respect to load current condition. This technique also ensures the continuous and smooth switching procedure between the digital and analog operations. The D/A selector is structured by an array of multiplexers and controlled by the load-dependent signals V_{AtoD} and V_{DtoA}. Pass transistors M_{Q1} to M_{QN} are controlled by the gate control signals V_{D1} to V_{DN} of the digital controller or the analog signal V_{GA} of the analog controller.

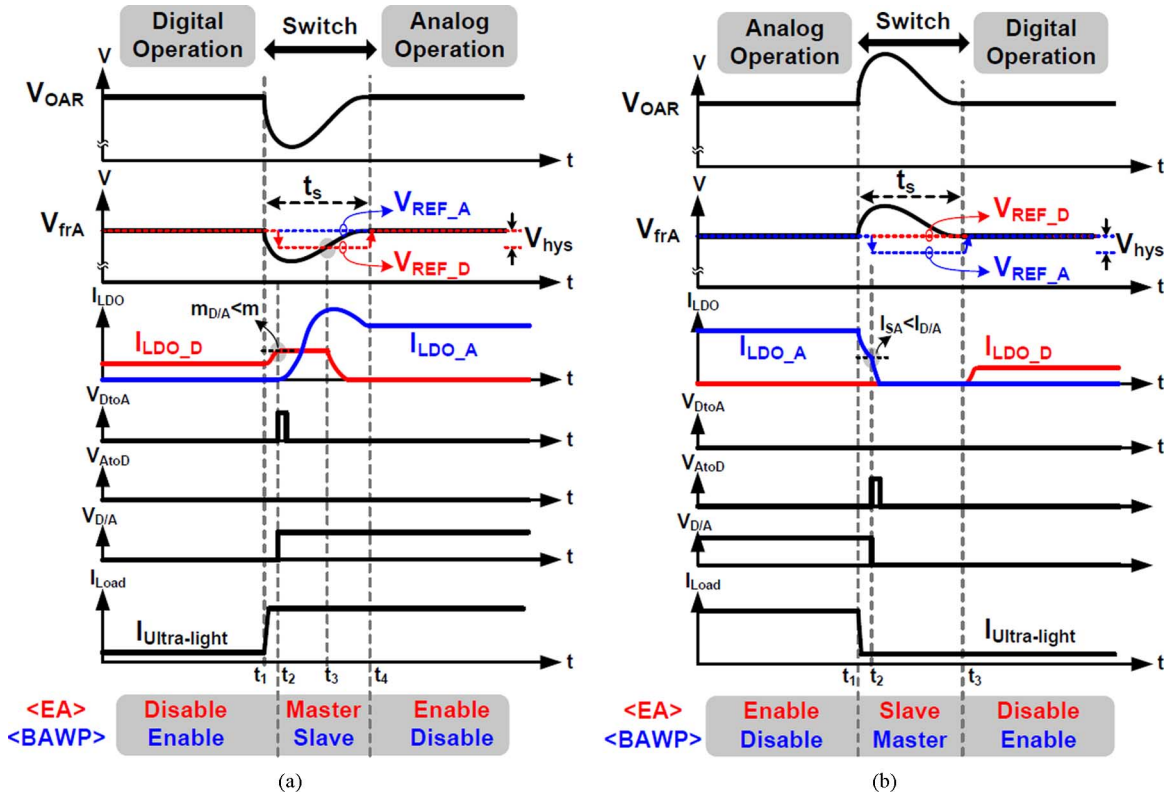

Fig. 11. Control mechanism of switchable technique between digital operation and analog operation. (a) Switch from digital operation to analog operation. (b) Switch from analog operation to digital operation.

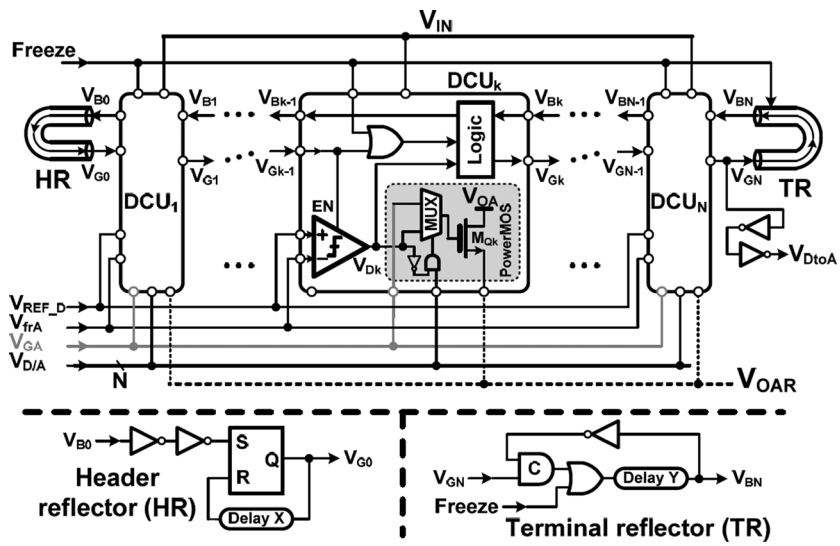

Fig. 12. Schematic of the BAWP circuit in switchable D/A LDO regulator.

Once the analog operation is taken place, the EA generates the error signal V_{GA} that in turn guarantees the output voltage V_{OAR} under different output load current conditions. Each gate voltage, from V_{G1} to V_{GN}, of the pass transistors are connected to the error signal V_{GA} when the switchable LDO regulator is in the analog operation. By contrast, the digital operation activates when the SoC enters into silent mode. At this period, the BAWP circuit generates thermometer control codes for each of the pass transistors. The digital control method releases the minimum load limitations at only several microamperes for the system to effectively conserve power. Moreover, the freeze operation in the BAWP circuit reduces quiescent current to an ultra-low value for high efficiency. Consequently, the proposed switchable D/A LDO regulator achieves ripple suppression and energy-efficient operation in a distinct mode for high efficiency.

B. Smooth Switch Technique

The proposed switchable D/A LDO regulator indicates only one of two operations that can be enabled in case of load current change. The SST also ensures the continuous and smooth

takeover procedure between analog and digital operations to prevent undesirable oscillation that induces large output voltage ripples. The hysteresis window $V_{\rm hys}$ adjusts the reference voltages of the D/A LDO regulator during the switching procedure. The flowchart in Fig. 10 describes the operation procedure during switching. When the LDO regulator switches from digital to analog operation during load current increases, the increasing value of m becomes larger than the pre-defined $m_{\rm D/A}$ and triggers the operation procedure by pulse signal $V_{\rm DtoA}$. Thus, the EA is activated and the reference voltage of BAWP, $V_{\rm REF\_D}$, also changes from $V_{\rm REF}$ to the value of '$V_{\rm REF}$-$V_{\rm hys}$'. The EA and the BAWP temporarily operate simultaneously. Meanwhile, the EA gradually dominates the control of SMUs when the feedback voltage V_{frA} is larger than $V_{\rm REF\_D}$. The EA and the BAWP represent the master and the slave, respectively. Finally, the switching procedure is complete when the EA leads the operation and disables the BAWP automatically with regulated output voltage. By contrast, when the LDO regulator switches from analog to digital operation during load current decreases, the decreasing sensing current I_{SA} becomes smaller than the predefined $I_{\rm D/A}$ and triggers the switching procedure by the pulse signal $V_{\rm AtoD}$, as shown in Fig. 9. The following switching procedure is completed by the aforementioned opposite procedure.

The operation waveforms of the SST are shown in Fig. 11. The currents $I_{\rm LDO\_D}$ and $I_{\rm LDO\_A}$ flow through the SMUs and are controlled by the BAWP and EA, respectively. In cases of increasing load current, the digital operation switches to analog operation as illustrated in Fig. 11(a). At $t = t_1$, the I_{LDO_D} increases with the rising number of turned-on sub-MOSFET units. At $t = t_2$, if m is larger than $m_{\rm D/A}$, the EA is enabled and the reference voltage of the BAWP, $V_{\rm REF\_D}$, changes from $V_{\rm REF}$ to the value of V_{REF}-$V_{\rm hys}$. As a result, the EA and the BAWP function in a master–slave relationship. During this period, the EA controls the remaining switched-off SMUs and the $I_{\rm LDO\_A}$ subsequently increases to regulate the output voltage V_{OAR}. Once the feedback voltage V_{frA} increases to a value higher than the $V_{\rm REF\_D}$ at $t = t_3$, the $I_{\rm LDO\_D}$ is reduced to zero and the BAWP is automatically disabled. Finally, after the V_{OAR} recovers at $t = t_4$, the switching procedure is complete. The analog operation takes over and enables only the EA. The BAWP shuts down to work in a single loop control.

The analog operation can be switched back to the digital operation if the load current decreases to a low enough value, as shown in Fig. 11(b). At $t = t_1$, the $I_{\rm LDO\_A}$ continuously decreases and is controlled by the EA. At $t = t_2$, once the condition of I_{SA} is smaller than $I_{\rm D/A}$, the BAWP is enabled and the reference voltage of EA, $V_{\rm REF\_A}$, changes from $V_{\rm REF}$ to the value of '$V_{\rm REF}$-$V_{\rm hys}$'. Thus, the $I_{\rm LDO\_D}$ gradually increases while the $I_{\rm LDO\_A}$ is reduced to zero. The switching procedure is complete when the V_{OAR} recovers at $t = t_3$.

According to the load condition, SMUs are controlled by the analog or digital controller determined by the SST. Ten percent of SMUs are driven by the digital controller at light loads. Ninety percent of SMUs are turned off. During the D/A switching procedure in case of light-to-heavy load changing, the analog controller controls a portion of the power MOS units while the digital controller controls other portions. The analog

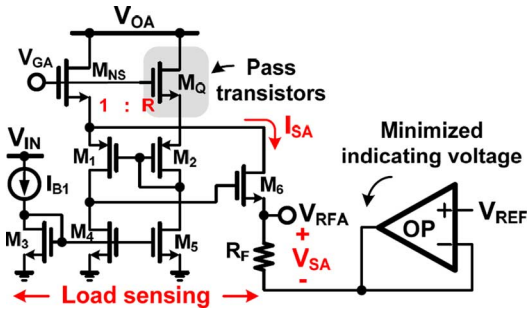

Fig. 13. Reference adjuster of ADVS modulation.

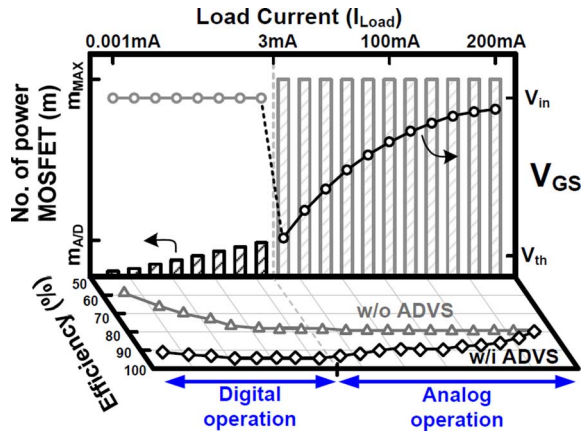

Fig. 14. Simulated performance of the switchable D/A LDO regulator.

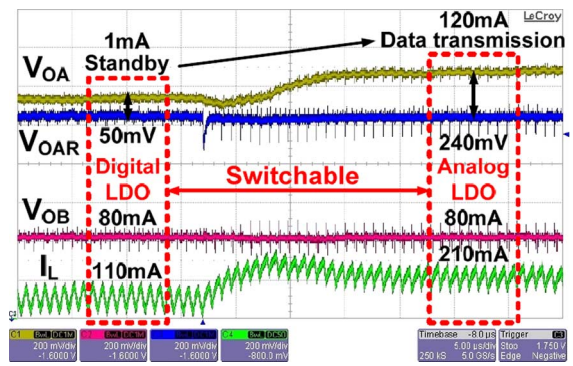

Fig. 15. Measured load transient with the distinct operation modes in SoC.

controller controls all power MOSFET units at the end of the load change. Finally, none of SMUs are controlled by the digital controller. Consequently, the energy delivered to the output is continuous to retain low output voltage variation. By reflecting the variation of output voltage through the feedback network, the condition of $m_{\rm D/A} < m$ or $I_{SA} < I_{\rm D/A}$ implies which controller is suitable for use. Thus, SMUs are adequately controlled even if the loading condition changes faster than the switching time. Upon setting the reference voltage to $V_{\rm REF}$–$V_{\rm hys}$, the stability is confirmed if a moderate or long period is used as the hysteresis window.

C. Bidirectional Asynchronous Wave Pipeline

The BAWP circuit, as illustrated in Fig. 12, generates the control signals for the pass transistors to guarantee the digital operation in the switchable D/A LDO regulator. The digital

TABLE I
DESIGN SPECIFICATIONS OF PROPOSED POWER MODULE

Topology	Switchable D/A LDO regulator		SIDO
Fabricated process	40 nm CMOS		40 nm CMOS
Input voltage	1.85 V – 2.2 V		2.7 V – 4.2V
Output voltage	1.8 V		V_{OA}: 1.85V ~ 2.20V V_{OB}: 1.00V ~ 1.30V
Quiescent current I_Q	Analog operation Digital operation	30 µA 0.05 µA	260 µA (w/o driver)
Leakage current on resistor divider I_{Leak}	0.8µA		10µA
Inductor	N/A		4.7 µH
Output capacitance	< 100pF		4.7 µF
Load range	0~200mA		< 400mA
Output ripple	Analog operation Digital operation	5mV @I_{Load}=120mA 12mV @I_{Load} =1mA	12mV
Power efficiency P_{OUT}/P_{IN}	Analog operation Digital operation	96.7%~81.2% 97.2%~92.57%	91% (Peak)
Current efficiency $I_{Load}/(I_{Load}+I_Q)$	Analog operation Digital operation	99.9%~99.0% 99.9%~95.0%	N/A
Active area	2 mm^2		

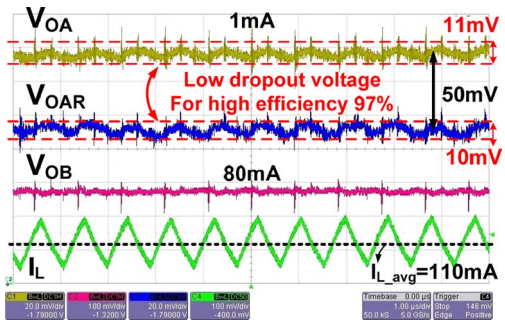

Fig. 16. Measured digital operation in the switchable D/A LDO regulator.

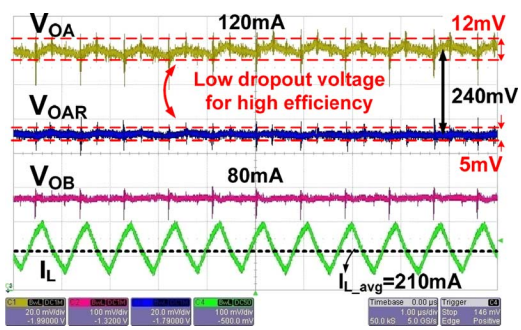

Fig. 17. Measured analog operation in the switchable D/A LDO regulator.

control unit (DCU) is used to realize the asynchronous operation. The advantage of this condition lies in clock-free operation and the reduction of power loss caused by periodical switching. In addition, the header reflector (HR) and the terminal reflector (TR) are adopted to ensure correct function in light of the asynchronous operation scheme. The freeze signal interrupts the asynchronous operation once the digital LDO enters into static operation. Therefore, current consumption is also minimized and power efficiency is enhanced.

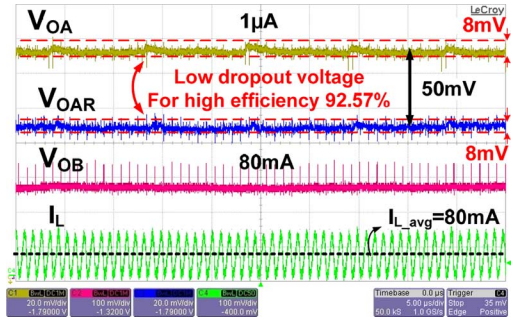

Fig. 18. Measured digital operation in the switchable D/A LDO regulator at ultralight loads.

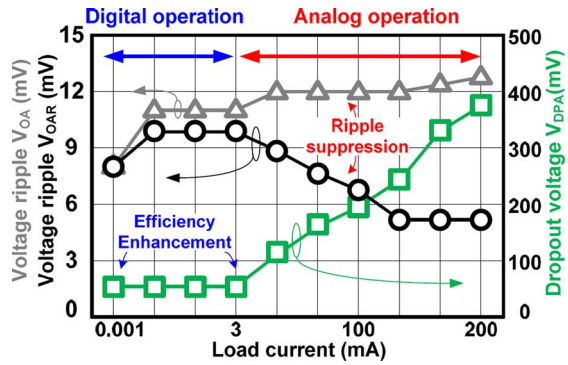

Fig. 19. Measured voltage ripple on the V_{OAR} for analog subcircuits in SoC.

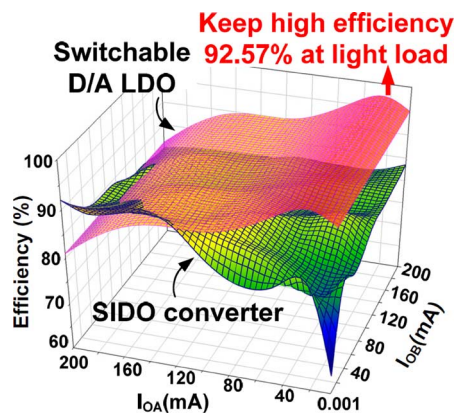

Fig. 20. Measured power efficiency.

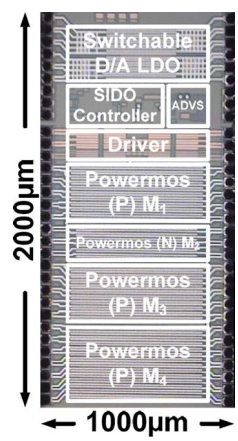

Fig. 21. Chip micrograph.

TABLE II
COMPARISON TABLE

Topology	[19]	[13]	[20]	[21]	[22]	Proposed Switchable D/A LDO regulator	
Fabricated process (μm)	0.35	0.35	0.35	0.09	0.065	40 nm CMOS	
Output voltage (V)	1.5	2.8	0.5	0.9	1	1.8 V	
Dropout voltage (mV)	142	200	400	300	200	50mV~400mV	
Output capacitor (pF)	0-100	0-100	0	600	0-100	0-100	
$I_{Load(max)}$ (mA)	100	50	50	100	10	200mA	
$I_{Load(min)}$ (mA)	0	0	0	0	0	0	
Quiescent current I_Q (μA)	27	65	0.103	6000	0.9~82.4	Analog operation Digital operation	30 μA 0.05 μA (★)
Leakage current on resistor divider I_{Leak} (μA)	N/A	N/A	N/A	N/A	N/A	0.5 μA	
Line regulation (mV/V)	1.046	23	21.76	N/A	4.7	1.9	
Load regulation (mV/mA)	0.0752	0.56	0.324	1.8	0.3	0.036	
Step-load ΔI_{Load} (mA)	100	50	50	100	100	119	
Edge time Δt (μs)	1	1	N/A	0.0001	0.3	1	
Settling time (μs)	N/A	15	400	N/A	6	3	
Undershoot voltage ΔV_{OUT} (mV)	25	90	320	90	68.8	50	
Current efficiency $I_{Load}/(I_{Load}+I_Q)$ @ I_{Load}=100mA	99.97%	99.93%	99.99%	94.33%	99.91%	99.97%	
Current efficiency $I_{Load}/(I_{Load}+I_Q)$ @ I_{Load}=1μA	35%	15%	90.6%	0.1%	52.6%	95.2% (★)	
Power efficiency P_{OUT}/P_{IN}	<91.3%	<93.3%	<92.5%	<96%	<83.3%	Analog operation Digital operation	96.7%~81.2% 97.2%~92.57%
Power efficiency P_{OUT}/P_{IN} @ I_{Load}=1μA	31.95%	13.99%	83%	9.6%	43.65%	92.57% (★)	

D. Reference Adjuster of Analog Dynamic Voltage Scaling Modulation

A schematic of the reference adjuster of ADVS modulation is presented in Fig. 13. The current flowing through the pass transistors must be monitored to dynamically adjust the dropout voltage for the analog LDO regulator. The load sensing implementation obtains the supply current information through the load sensing circuit. The load current is replicated to the sensed current I_{SA}, to generate the reference voltage V_{RFA} by the resistor R_F. Therefore, the load current condition properly modulates the output voltage level of V_{OA} in the SIDO converter to guarantee the optimal dropout voltage in the switchable D/A LDO regulator with an analog operation. Furthermore, the minimized indicating voltage also ensures the smallest dropout voltage in the analog LDO regulator.

V. EXPERIMENTAL RESULTS

The proposed SIDO converter with the switchable D/A LDO regulator was fabricated using a 40-nm CMOS process. The off-chip inductor for the SIDO power module has a value of 4.7 μH and the output capacitors at both V_{OA} and V_{OB} have a value of 4.7 μF. The input voltage ranges from 2.7 to 4.2 V. The nominal voltage at the output of the switchable D/A LDO regulator is 1.8 V. Fig. 14 illustrates the simulation performance of the switchable D/A LDO regulator. The ADVS works in analog operation at heavy loads and in digital operation at light loads. Thus, the switchable D/A LDO regulator enhances power conversion efficiency compared with the performance of converters without the ADVS.

Fig. 15 shows the measured load transient response with distinct SoC operation modes. The switchable D/A LDO regulator operates by the digital controller during standby with 1-mA load current. The regulator also operates by the analog controller to suppress the voltage ripple during data transmission operations with 120-mA load current. The detailed design specifications are listed in Table I. If the maximum output capacitance at V_{OAR} is 100 pF during the analog operation, the load current can be decreased to 100 μA. For safety operation, the operation is switched to digital control when the load current is less than 500 μA. Thus, the system is stable even when the load decreases to 10 μA. Fig. 16 presents the measured digital operation in the switchable D/A LDO regulator. The dropout voltage is reduced to 50 mV to minimize energy consumption on the pass transistors. Fig. 17 shows the measured analog operation in switchable D/A LDO regulator with dropout voltage of 240 mV to suppress switching voltage ripples. This condition enhances the supply quality and ensures the operation for noise-sensitive analog subcircuits in the SoC.

Fig. 18 demonstrates the stable system in digital operation even at an ultralight load current of 1 μA. Meanwhile, the SIDO converter operates in skip mode to conserve power. Fig. 19 shows the measured the dropout voltage and output voltage ripples on the V_{OAR}. A 5-mV output voltage ripple is achieved from a 120-mA load current because of the advantage of ripple

suppression by the analog operation while LDO voltage is also achieved at ultralight loads for power conservation. The measured power efficiency of switchable D/A LDO is shown in Fig. 20 and indicates the peak efficiency at 96.7% during analog operation. A value higher than 92.57% is retained even when the load current is reduced to 1 μA because of digital operation. Fig. 21 shows a chip micrograph with an active silicon area of 2 mm^2.

Even though prior literature largely emphasized no-load operation and adequate performance via high LDO current efficiency, as defined by $I_{\rm Load}/(I_{\rm Load} + I_Q)$, at values close to 99.9% during heavy loads. There was a need to adequately prolong battery usage time because portable devices spend much more time in standby mode than in active mode. For complete analysis, power efficiency, defined as $P_{\rm OUT}/P_{\rm IN}$ and related to quiescent current and dropout voltage at ultralight loads, is evaluated in comparison with efficiency performance. The comparison results on the performance of different LDOs are summarized in Table II. Other works consume extra power to increase system stability thereby causing poor power and current efficiency at ultralight loads, although they can perform good power and current efficiency at heavy loads. With the D/A switchable technique, the proposed design effectively conserves power at ultralight loads to further extend the battery usage time.

VI. Conclusion

This paper presents a SIDO converter with a switchable D/A LDO regulator for improving supply quality. The proposed ADVS function dynamically adjusts the dropout voltage to achieve the tradeoff of ripple suppression function and high efficiency operation. The regulator can switch to digital operation once an ultralight load condition occurs. Specifically, the limitations of the minimum load current requirement for the capacitor-free LDO are significantly reduced to several microamperes, and the quiescent current is further reduced to nanoamperes at light loads for power conservation. Furthermore, the proposed SST decides a digital or analog operation with respect to the load current condition. The SST ensures the continuous and smooth switching procedure between digital and analog operations. Experimental results demonstrate that the switchable LDO regulator operation exhibits a peak efficiency of 96.7% in analog operation and 5-mV output voltage ripple at a load of 120 mA. The efficiency can be maintained at a value over 92.57% even when the load current is at 1 μA.

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