High-quality planar light emitting diode formed by induced two-dimensional electron and hole gases

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Abstract: A high-quality planar two-dimensional p-i-n light emitting diode in an entirely undoped GaAs/AlGaAs quantum well has been fabricated by using conventional lithography process. With twin gate design, two-dimensional electron and hold gases can be placed closely on demand. The electroluminescence of the device exhibit high stability and clear transition peaks so it is promising for applications on electrically-driven single photon sources.

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OCIS codes: (230.3670) Light-emitting diodes; (230.5590) Quantum-well, -wire and -dot devices.

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#200571 - $15.00 USD Received 4 Nov 2013; revised 19 Dec 2013; accepted 8 Jan 2014; published 11 Feb 2014

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1. Introduction

Most of the III-V optoelectronic devices rely on junctions formed by stacks of epilayers, where the electrical current flows across the junction vertical to the sample surface. The lateral p-n junctions that are and difficult to fabricate, however, are often desirable for many device applications. For example, because of their coplanar geometry, they are suitable for optoelectronic integration. Since the cross section of the lateral junction is determined by the thickness of the epilayer, the capacitance of the junction can also be much smaller than that of conventional vertical ones. Thus, the 2-D lateral junctions could lead to a new family of high-frequency and optoelectronic devices [1–6]. Furthermore, lateral 2-D p-n junctions are potential candidates for investigating the properties of electron spins in low-dimensional systems by optical methods [7]. On the other hand, there has been an increasing interest in the surface acoustic wave (SAW)-driven single-photon sources owing to their potential applications in high-speed quantum communications [8–10]. In [8], Foden *et al* proposed that when a SAW propagates through a two-dimensional (2D) p-i-n junction, a series of traveling quantum dots are formed in the i-region of the junction. Consequently, a constant stream of electron packets, which can be manipulated by a controlled gate voltage, flows from a two-dimensional electron gas (2DEG) channel into a two-dimensional hole gas (2DHG) channel, where electrons and holes are recombined to create bursts of optical pulses. By controlling the split gate voltage, one can obtain a stream of single electrons to generate single photons. In SAW-driven single-photon source devices, the key component is a high-quality 2-D p-i-n junction.

With the aim of reliably fabricating 2-D lateral p-n junctions, several methods have been developed over the past years [3–5, 7, 9–15]. The authors in [2,12,13] fabricated lateral p-n junctions by molecular beam epitaxy (MBE) growth on a patterned GaAs substrate by employing the amphoteric nature of the Si dopants to simultaneously form 2DEG on the (001) planes and 2DHG on (113)A planes. Kaestner *et al.* used a partially etched GaAs/AlGaAs heterostructure to define 2DEG and 2DHG regions [15]. In [14], Hosey *et al.* integrated MBE growth with a focused ion beam to fabricate a lateral p-n junction. All above methods used complex technique and based on doped heterostructures. Introducing impurities affects luminescence efficiency by presenting non-radiative recombination channels. Thus, it will affect further application for single-photon devices.

In this paper, we demonstrate a novel structure utilizing induced 2DEG and 2DHG channels in an undoped GaAs quantum well to form the lateral p-i-n junction. The two different types of channels are induced via surface Schottky gates and metal-insulator-semiconductor (MIS) gates. The device created is not just a diode but also a transistor, as suggested by [16]. The amount of current and the resulting light emitting intensity of the lateral diode are controllable by the bias voltages applied to the gates and the source and the drain. The device has a planar structure and can be easily fabricated by conventional metallization and lithography processes.

#200571 - $15.00 USD Received 4 Nov 2013; revised 19 Dec 2013; accepted 8 Jan 2014; published 11 Feb 2014

2. Sample design and process

The layer structure used for lateral junction fabrication is that of a GaAs/AlGaAs quantum well shown in Fig. 1(a). The sample was grown on a semi-insulating (100) GaAs substrate by using a solid-source MBE system. A 400-nm $Al_{0.33}Ga_{0.67}As$ was grown on top of a 100-nm GaAs buffer layer, followed by a 10-period GaAs/$Al_{0.33}Ga_{0.67}As$ (3 nm/3 nm) superlattice. A 20-nm GaAs quantum well between two $Al_{0.33}Ga_{0.67}As$ barriers was grown as the 2-D channel of the device. Finally, the sample was capped with a 3-nm GaAs layer. All layers are intentionally undoped.

The device processing starts with a mesa etching step to define the channel region. The n-type ohmic contact region was then defined and recessed down to the GaAs channel. All metal depositions were done by an e-gun evaporator. The n and p Ohmic contacts are formed by Ni/Ge/Au/Ni (5 nm/70 nm/70 nm/35 nm) and Pd/AuZn (40 nm/100 nm) then annealed at 450 °C and 420 °C for 2 mins, respectively. After the gate recess using $H_2O:H_3PO_4:H_2O_2$ (1:3:50) to a depth of 150 nm, the Schottky gate metal of Ti/Au (20 nm/80 nm) for both n and p channels was deposited to form the surface gate (SG). A 350-nm photosensitive polyimide, serving as an insulator layer, was then coated and patterned. Finally, the metal Ti/Au (20 nm/200 nm) was deposited on top of the polyimide layer to form the top gate (TG). The top view of a finished device is shown in Fig. 1(b). The upper half is the p-channel device and the lower half is the n-channel device. The devices are normally off because the epitaxy layers are totally undoped.

In our device layout, the n-SG and the p-SG are placed side by side with 2 μm spacing; see Fig. 1(b). With a negative voltage applied on the p-gates (SG and TG) and a positive voltage applied on the n-gates (SG and TG), both 2DHG and 2DEG channels can be induced in the GaAs quantum well, so a lateral 2-D p-i-n diode is formed. The schematic cross-section of the device is shown in Fig. 1(c). 2DEG and 2DHG are induced in the left and the right side of the quantum well, respectively. Previously we reported a lateral p-i-n diode using a single-gated MIS structure [17]. But the gate control of the carriers in the quantum well is not very efficient because of the distant gate from the channel. As a result, the two top gates on the insulator could not be put too close to each other. This directly affects the carrier recombination in the i region. To solve this problem, we developed the present twin gate structure, which was first introduced by Harrell et al. [18]. The surface gates provide a very good control for the carriers in the channel and at the same time can be put very close to each other. The top gates, which overlap the source and the drain through the insulator spacer, control the carriers in the channel regions next to the source and the drain without having a leakage path between the gates and the ohmic contacts. The fabricated device, Fig. 1(b), has a length of 10 μm and a width of 7.5 μm for both 2DEG and 2DHG channels. The distance between the n-SG and the p-SG, that is the length of I region, is 2 μm. Electrical and optical characteristics of the devices were measured at 4K.

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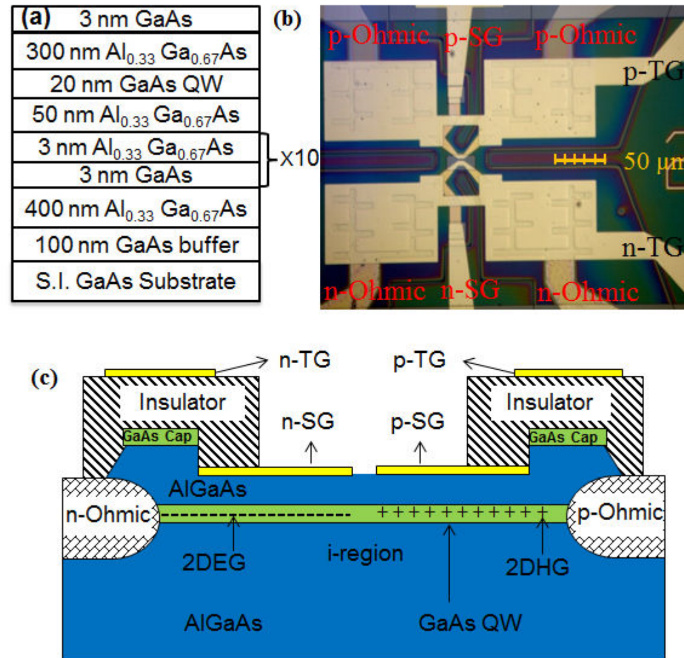

Fig. 1. (a) Sample structure grown by MBE. (b) Optical microscopy image of the finished device. (c) Schematic cross-section of the devices.

3. Results and discussion

Figure 2(a) shows the drain current versus p-TG voltage (denoted as V^p_{tg}) curve for the p-channel with the drain-source (two p-type Ohmic contacts) voltage, V_{ds}, set at 500 mV. The two different curves correspond to two different p-SG voltages of −0.4 V and −0.6 V. The p-TG threshold voltage is −0.8 V, which stays constant for the two p-SG voltages. The transconductance is higher for $V^p_{sg} = -0.6$V as expected because more carriers are induced in the channel. The same measurements were performed for n-channel of the devices. The inset of Fig. 2(a) shows the drain current versus n-TG voltage curve of the n-channel with n-SG voltage V^n_{sg} = 0.9 V and the drain-source (two n-type Ohmic contacts) voltage V_{ds} of 500 mV. The threshold voltage of the n-TG is 3.2 V. The higher threshold voltage of the n-channel is probably due to the surface state pinning at the insulator/semiconductor interface [18]. Figure 2(b) shows the drain current versus p-SG voltage V^p_{sg} for the p-channel at V_{ds} = 500 mV. Different curves correspond to different p-TG voltages. The p-SG threshold voltage is −0.2 V. The saturation current is higher for higher V^p_{tg}, because the series resistance between the channel and the source Ohmic contact is reduced when V^p_{tg} increases. The I_{ds}-V^n_{sg} curve for the n-channel with V^n_{tg} = 6 V and V_{ds} = 500 mV is shown in the inset of Fig. 2(b). The threshold voltage of the n-SG is 0.5 V. Leakage currents to gates were negligible so the stability of the induced carriers is pretty good.

By biasing the n- and p-channel devices above their threshold voltages, the electrical characteristics of the p-i-n device were then measured. The measurement configuration is shown in the inset of Fig. 3. The p-TG bias V^p_{tg} and p-SG bias V^p_{sg} of the p-channel device were set at −3 V and −0.6 V respectively and those of the n-channel device were V^n_{tg} = + 6 V and V^n_{sg} = + 0.9 V. The current flow between the p-channel and the n-channel, denoted as I_{pn}, was measured as a function of the voltage applied between the p and n ohmic contacts V_{pn}; see inset of Fig. 3. In the measurement setup, the gate voltages for the N channel were measured relative to the source (the ohmic contact on the left), and the voltage of the P gates were measured relative to the drain (the ohmic contact on the right). So with this setup, the

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channel condition for both the N channel and the P channel remains the same when V_{pn} is changed. The current I_{pn} in Fig. 3 is plotted both in the linear and logarithmic scales for clarity. One can see clearly the rectifying behavior with turn-on voltages of 1.73 V. Very good exponential behavior was observed all the way down to the measurement limit. The current of the diode can go up to hundreds of microamperes. Two kinks occur in the I-V curve at V_{pn} = 1.48 and 1.70 V. The kink position slightly changes with the surface gate bias. Thus, they could be attributed to the potential barriers for hole at p-i junction and for electron at the n-i junction. However, further investigations are needed to address this issue.

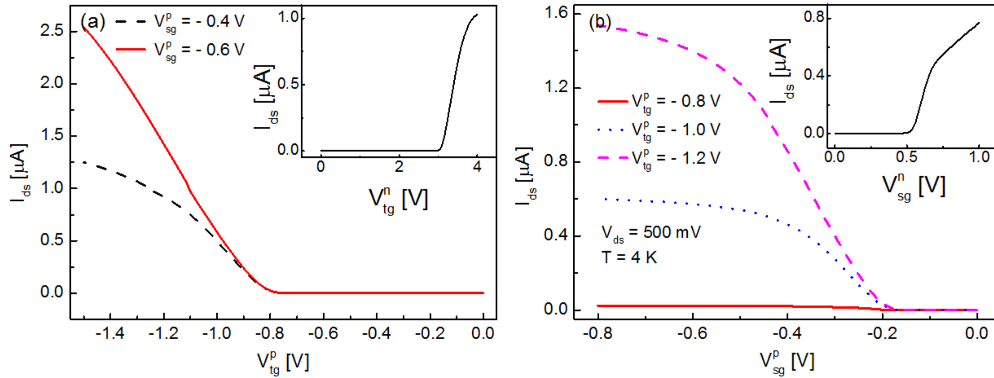

Fig. 2. Current – voltage characteristics of 2DEG and 2DHG with bias between two Ohmic V_{ds} = 500 mV at temperature of 4 K. (a) Current – TG voltage characteristics of 2DHG with different SG voltages, −0.4 V (dashed line)and −0.6 V (solid line). The inset shows current – TG voltage characteristics of 2DEG. (b) Current – SG voltage characteristics of 2DHG with different TG voltages, −0.8 V (solid line), −1.0 V (dot line), and −1.2 V (dashed line). The inset shows current – SG voltage characteristics of 2DEG channel.

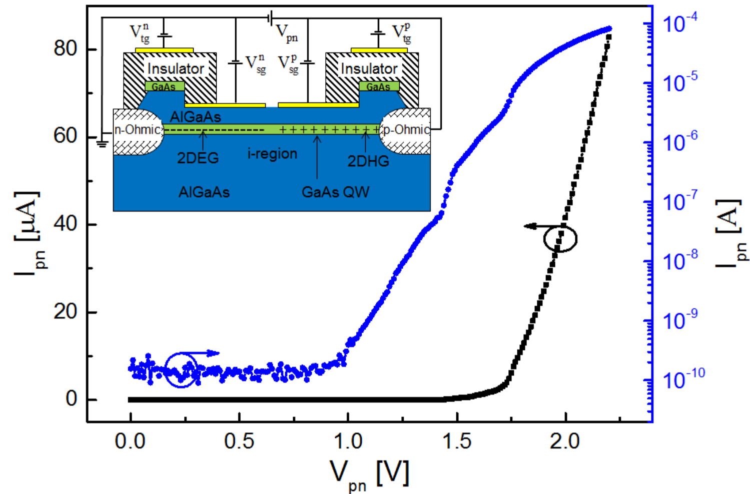

Fig. 3. Linear and logarithmic current – voltage characteristics of the lateral 2-D p-i-n diode at temperature of 4 K with p-TG and n-TG biased at V^p_{tg} = −3 V and V^n_{tg} = + 6 V, respectively, and p-SG and n-SG biased at V^p_{sg} = −0.6 V and V^n_{sg} = + 0.9 V, respectively. V_{pn} is the operation voltage of the diode. The inset shows measurement configuration.

The electroluminescence (EL) emission of the p-i-n diode measured at 4 K is shown in Fig. 4(a). The device was measured under the surface gate voltages of V^n_{sg} = + 0.9 V and V^p_{sg} = −0.6 V, and the top gate voltages of V^n_{tg} = 6 V and V^p_{tg} = −3 V, and the junction voltage from V_{pn} = 1.6 V to 2.0 V with step of 0.05 V. The inset of Fig. 4(a) shows the

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measure photoluminescence (PL) of the sample. We clearly observe two peaks in the PL spectra at 1.5205 eV (815.5 nm) and 1.5239 eV (813.7 nm). The intensity ratio of the two PL peaks remains constant when the excitation power changes. Thus, the two peaks observed here are most likely due to the roughness of the quantum well interfaces [19]. There are also two peaks at 1.5174 eV (817.5 nm) and 1.5207 eV (815.4 nm) in the EL spectra. The peaks have a 0.4 meV redshift when the junction bias V_{pn} increases from 1.6 V to 2.0 V. Full width at half maximum of the 1.5205 eV peak changes from 1.2 to 2.2 meV, and that of the other peak from 1.2 to 3 meV when V_{pn} increases from 1.6 V to 2.0 V. The narrow linewidths of the peaks demonstrate that the 2-D channel is of high-quality, which is essential for further applications such as electrically-driven single photon sources.

Figure 4(b) shows the integrated intensity of the EL spectra (black curve with square symbol) against the junction bias V_{pn}. Light intensity increases linearly with diode voltage V_{pn}. Inset of Fig. 4(b) shows the integrated intensity of the EL spectra (black curve with triangle symbol) and external efficiency (blue curve with round symbol) versus the diode current I_{pn}. At low currents, $I_{pn} < 5.0$ µA, after an initial set back, the light intensity rises sharply with current. At higher currents, $I_{pn} > 5.0$ µA (after the diode turns on, $V_{pn} > 1.73$ V), the light intensity increases with current at a constant rate. However, the slope of L-I curve is much smaller in comparison to low injection currents. The result can be explained as follows. At low currents, radiative recombination mostly happens in the i-region. But at high currents, electrons are injected into the p-region under p-SG and holes are injected into the n-region under n-SG. So, as a result, part of the radiation is blocked by the gate metal. Consequently, light collection efficiency decreases. This can be seen in the external efficiency curve in inset of Fig. 4(b). With the increasing forward current I_{pn} from 0.0 µA to 5.0 µA, the external quantum efficiency increases to a maximum of 0.003%, then it drops dramatically for I_{pn} > 5.0 µA (after the diode turn on, $V_{pn} > 1.73$ V). This problem could be avoided by using semi-transparent metal gate.

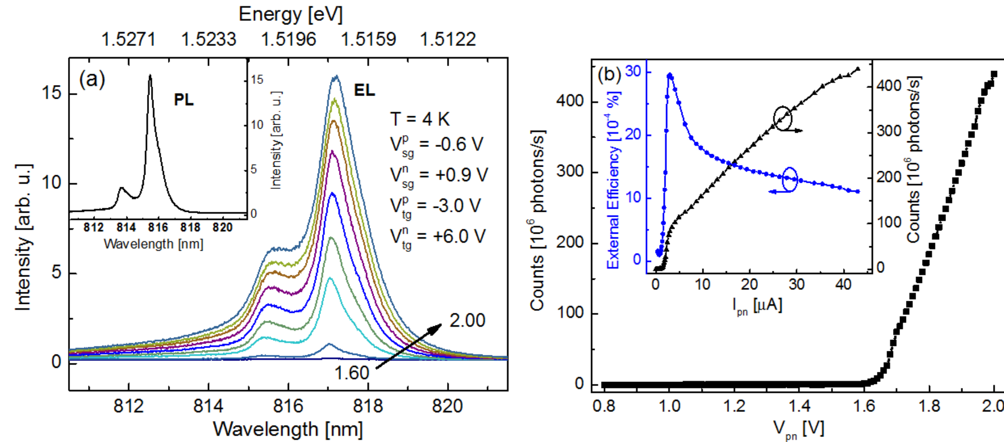

Fig. 4. (a) Electroluminescence spectra of the lateral 2D p-i-n diode at temperature of 4 K with with p-TG and n-TG biasing at $V^p_{tg} = -3$ V and $V^n_{tg} = +6$ V, respectively and p-SG and n-SG biasing at $V^p_{sg} = -0.6$ V and $V^n_{sg} = +0.9$ V, respectively and V_{pn} from 1.6 V to 2.0 V with step 0.05 V. Inset shows photoluminescent spectrum at 4 K. (b) Light integrated intensity versus forward bias voltage of the lateral 2D p-i-n diode measured at the same condition. Inset shows the light integrated intensity (black curve with triangle symbol) and external efficiency (blue curve with round symbol) versus the diode current.

The electroluminescence emission spectra of our devices are stable and much cleaner than those of previously reported lateral 2-D junctions [5, 7, 9, 14]. This is important for using the device for further studies and applications. For example, Kim et al. used simultaneous Coulomb blockade for electrons and holes in a mesoscopic double barrier p-n junction to fabricate a single-photon turnstile [20]. And recently, Kaestner et al. [21] and Fletcher et al.

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[22] have successfully fabricated a stable single-electron pump on a 2DEG GaAs/AlGaAs heterostructure, we can make a single-photon source device by fabrication a single-electron pump on the i-region of the lateral p-i-n junction device. Thus, single hot electron can be pumped into 2DHG region and then single photon emitted as electron-hole recombination occurs. In this aspect, high repetition-rate and electrically-driven single photon source could be realized in coming years.

4. Conclusion

In conclusion, we have developed a relatively simple method to fabricate high-quality planar light emitting diode. By using the surface gate and top gate design, 2DEG and 2DHG can be induced side by side in a completely undoped GaAs/AlGaAs quantum well. The electrical and optical properties of the device show that the 2-D channel is of high quality. Our results demonstrate that the device is promising for applications in the single-photon devices.

Acknowledgments

We would like to acknowledge the Center of Nano Science and Technology at National Chiao Tung University for their equipment support. This work was financially supported by the National Science Council and ATU program of Ministry of Education in Taiwan.

#200571 - $15.00 USD Received 4 Nov 2013; revised 19 Dec 2013; accepted 8 Jan 2014; published 11 Feb 2014
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