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Effects of N_2O-Plasma Treatment of a-SiO_xN_y/a-SiN_x Gate Insulators on Electrical Stability of a-Si:H Thin-Film Transistors

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N_2O-plasma was used to treat the as-deposited a-SiO_xN_y/a-SiN_x gate insulators of inverted-staggered a-Si:H thin-film transistors (TFTs), and its effects on electrical properties of TFTs were investigated. The TFTs with N_2O-plasma-treated gate insulators tended to have a smaller threshold voltage (V_{th}), V_{th} shift and hysteresis width (W_{FB}) of the forward and backward transfer characteristics. In addition, the results of a bias-temperature stress (BTS) experiment showed that the N_2O-plasma-treated devices had a smaller decay of drain current with time. These phenomena demonstrated that the N_2O-plasma treatment could be used to improve the electrical stability of a-Si:H TFTs.

KEYWORDS: thin-film transistor, electrical stability, N_2O-plasma treatment

1. Introduction

Exposure to light or gate-bias stress can cause a reduction of on-conductance and a V_{th} shift to a conventional a-Si:H thin-film transistor (TFT) with an a-SiN_x gate insulator.[1,2] Alternately, an a-SiO_xN_y gate insulator, which possesses a lower mechanical stress and a larger optical gap than those of the a-SiN_x film, is more water-resistant than the a-SiO_x film.[3] Also, a thin a-SiN_x layer inserted between the a-Si:H channel and a-SiO_xN_y gate insulator can be used to reduce the density of trapped charges in the a-SiO_xN_y gate insulator without degrading the switching characteristics of an a-Si:H TFT.[4] Therefore, the structure of a-SiO_xN_y/a-SiN_x gate insulators may result in good performance of a-Si:H TFT.

Exposing the gate nitride to an O_2 plasma prior to the a-Si:H deposition results in a reduction of defects in the interface region and especially an improvement of the p-channel a-Si:H TFT characteristics.[5] Also, the surface oxidation of a-Si:H caused by the N_2O-plasma treatment of a fabricated a-Si:H TFT increases its drain current under negative gate bias.[6] On the other hand, although the NH_3-plasma treatment of the gate nitride causes a general increase in the subthreshold slope, S, and V_{th} of the a-Si:H TFT, the TFT stability can be improved, since the NH_3-plasma-treated TFT has a smaller W_{FB} and a higher resistance against the prolonged positive gate bias.[7] In addition, an H_2-plasma treatment of thermally grown SiO_2 gate insulator of a-Si:H TFT results in degradation of its electrical stability, and this phenomenon is ascribed to the increased defect density in SiO_2 caused by H_2-plasma treatment.[8]

We previously reported a N_2O-plasma treatment of a-SiO_xN_y/a-SiN_x gate insulators which showed an electrical stability improvement of the a-Si:H TFT.[9] Unfortunately, it also caused degradation of device field-effect mobility μ_{eff}. The Si source gas previously used during depositions of the gate insulators and channel was 4% SiH_4 in H_2.[9] Since a N-rich a-SiN_x layer can be used to improve the TFT performance,[4] in this study, the Si source gases employed were 4% SiH_4 in N_2 for gate insulators and 4% SiH_4 in H_2 for i- and n^+-a-Si:H layers, respectively. Then, a N_2O-plasma treatment of the as-deposited a-SiO_xN_y/a-SiN_x gate insulators was performed again to improve the electrical stability of an inverted-staggered a-Si:H TFT.

2. Experiments

The inset in Fig. 1 depicts the schematic cross section of the fabricated a-Si:H TFT. After patterning of the sputter-deposited 1500 Å Cr gates on the Corning 7059 glass substrate, the a-SiO_xN_y (1400 Å)/a-SiN_x (400 Å), i-a-Si:H (1450 Å) and n^+-a-Si:H (500 Å) films were deposited consecutively in a plasma-enhanced chemical vapor deposition (PECVD, ULVAC CPD-1108D) system. During the deposition process, the RF power densities and chamber pressures for the a-SiO_xN_y, a-SiN_x, i-a-Si:H, and n^+-a-Si:H films were kept at 50, 50, 28, 21 mW/cm^2 and 0.3, 0.45, 0.3, 0.4 Torr, respectively. The substrate temperatures were kept at 180°C for n^+-a-Si:H layer and 250°C for the others. The Al source/drain metal was thermally evaporated and then patterned with the conventional photolithographic technique. CF_4-O_2 plasma etching was used to expose the gate electrode of TFT and also to remove the n^+-a-Si:H layer between Al source/drain electrodes. For device passivation, a 2000 Å of SiO_2 was sputtered onto the a-Si:H TFT.

The N_2O-plasma treatment was performed immediately following the deposition of the a-SiN_x layer. The treatment conditions were RF power density of 28 mW/cm^2, chamber pressure of 0.25 Torr, substrate temperature of 250°C, N_2O flow rate of 100 sccm and treatment time of 12 min. Also, a NH_3-plasma treatment with the same process conditions was also employed for the purpose of comparison. The other fabrication conditions for the devices with/without treatment were kept the same.

The electrical characteristics of the a-Si:H TFTs were measured with an HP 4145B semiconductor parameter analyzer. V_{th}s and μ_{eff}s were determined from the x-axis intercept and the slope of the TFT square-law model. In calculation of the μ_{eff}, the capacitance in the TFT square-law model was measured using the metal/gate insulators/metal capacitor.

3. Results and Discussion

Figure 1 shows the transfer curves for three kinds of a-Si:H TFTs: (a) with N_2O-plasma treatment, (b) with NH_3-plasma treatment, and (c) without treatment. All of the on/off current ratios for these three devices exceeded 10^7 as estimated from the ratios of drain currents, I_{DS}, at $V_{DS}=0$ and 15 V. Their calculated V_{th}s were (a) 5.22, (b) 6.41, and (c) 5.73 V and the μ_{eff}s were (a) 1.013, (b) 1.305, and (c) 1.773 $cm^2/V\cdot s$. The capacitance measured using an ITO/a-SiO_xN_y/a-SiN_x/Al capacitor were (a) 20.15, (b) 19.96 and (c) 19.93 nF/cm^2. When the subthreshold slope S, defined as $dV_{GS}/d(\log I_D)$, was calculated for I_D ranging from 10 pA to 1 nA, the corresponding S values for these three kinds of a-Si:H TFTs were (a) 0.508, (b) 0.470 and (c) 0.352 V/decade, which showed a slight increase after plasma treatment. This phenomenon was similar to that presented in ref. 7.

Figure 2 shows the variations of V_{th} for these three kinds of a-Si:H TFTs after applying a gate bias of 10 V. As can be seen, the TFT with a N_2O-plasma treatment had the smallest V_{th} and V_{th} shift.

Figure 3 shows the forward and backward transfer characteristics of the a-Si:H TFTs with and without N_2O-plasma treatment. During the measurement of forward and backward transfer curves for the a-Si:H TFTs, a delay time of 5 s was used after each V_{GS} voltage step. It took about 25 min to complete the entire transfer curves for V_{GS} sweeping from -10 to 20 and then back to -10 V. This long measurement time allows the electron to be trapped deep in the gate insulator, kinetically causes the generation of a metastable state in a-Si:H, and forms the hysteresis curve in the forward and backward sweepings of transfer characteristics.[7] The experimental data for voltages below -2 V and above 16 V were omitted to emphasize the hysteresis phenomenon. The W_{FB}s, taken from the maximum separations between the forward and backward transfer curves of a-Si:H TFTs, were 0.345 and 1.701 V for the devices with and without N_2O-plasma treatment, respectively. On the other band, the W_{FB} of the NH_3-plasma-treated device was 0.776 V. Hence, the N_2O-plasma-treated a-Si:H TFT had the smallest W_{FB}.

Figure 4 shows the time dependence of drain current $I_D(t)$ normalized by its initial value $I_D(0)$ for these three devices at a temperature of 80°C. The decay of $I_D(t)/I_D(0)$ with time for the N_2O-plasma-treated device was

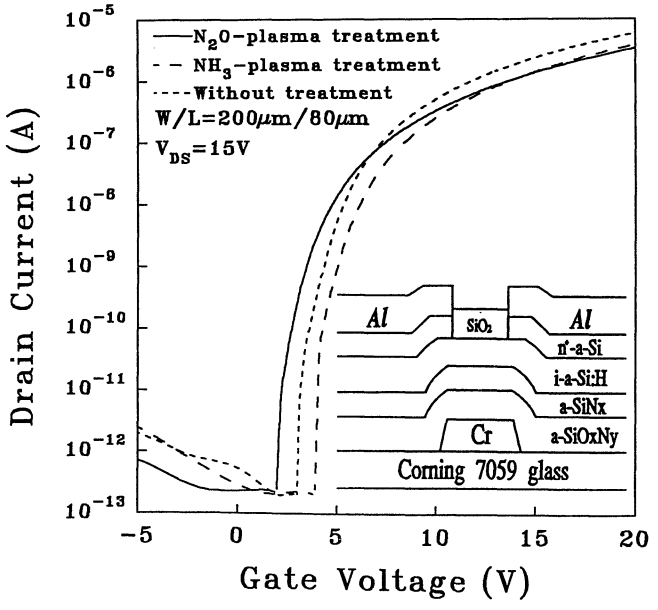

Fig. 1. The transfer characteristics of the three obtained a-Si:H TFTs (a) with N_2O plasma, (b) with NH_3 plasma, and (c) without treatment of gate insulators. The inset shows a schematic cross section of the inverted-staggered a-Si:H TFT.

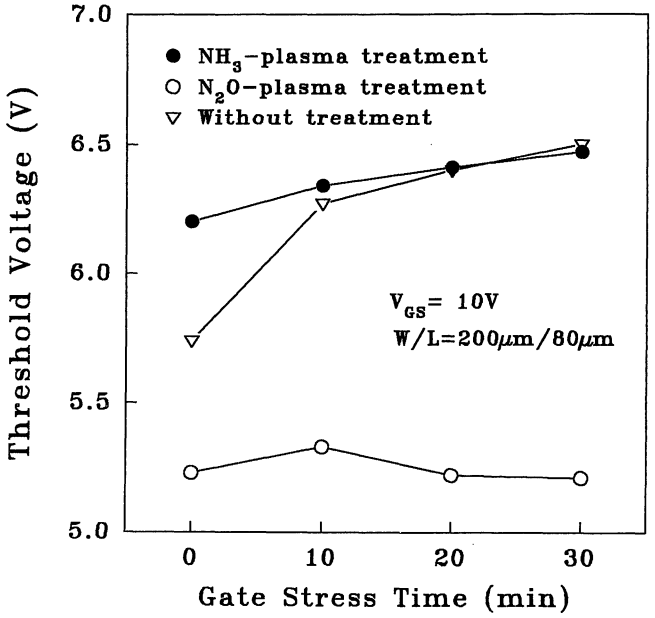

Fig. 2. The variations of V_{th} after applying a gate bias of 10 V for these three a-Si:H TFTs (a) with N_2O plasma, (b) with NH_3 plasma and (c) without treatment of gate insulators.

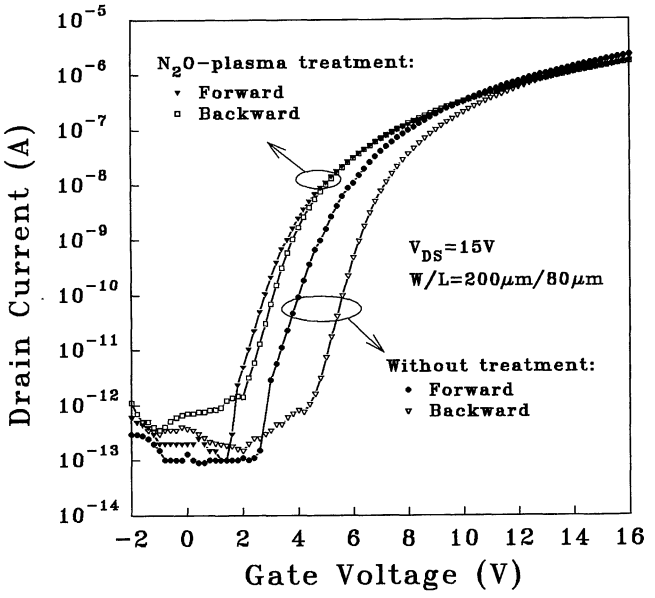

Fig. 3. The forward and backward transfer characteristics for the a-Si:H TFTs with and without N_2O-plasma treatment of gate insulators.

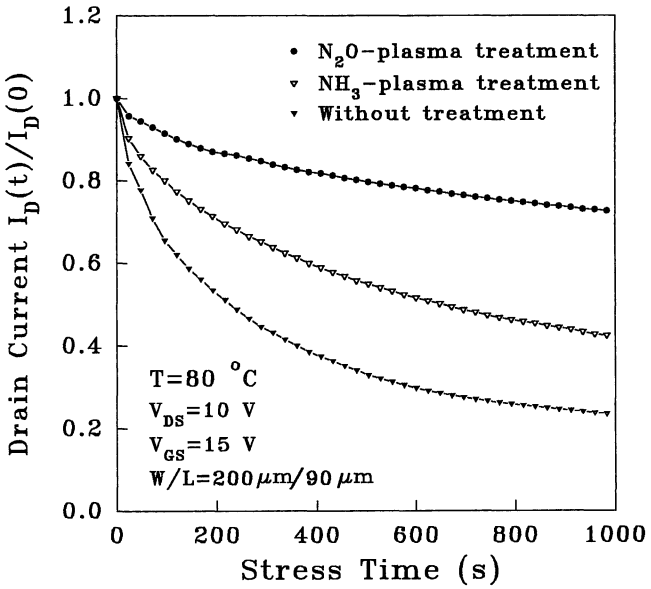

Fig. 4. The time dependence of drain current $I_D(t)$ normalized by its initial value $I_D(0)$ for these three a-Si:H TFTs at a temperature of 80°C.

found to be the smallest.

Table I lists the refractive indices (at a wavelength λ of 632.9 nm) and thicknesses before and after the different plasma treatments for the a-SiN_x layers grown on the Si wafers. These data were measured using a Woollam 12-wavelength spectroscopic ellipsometry. The thicknesses and refractive indices were nearly unchanged after plasma treatments.

Table II summarizes some electrical parameters of these three devices with W/L=200/90 (μm/μm). The data presented are the ranges of at least 5 sets of results taken from the corresponding devices on the substrates. It was clear the N_2O-plasma-treated device had the smaller V_{th} and W_{FB}. However, μ_{eff} of the N_2O-plasma-treated a-Si:H TFT obviously decreased and that of the NH_3-plasma-treated device decreased only moderately.

Furthermore, secondary ion mass spectroscopy (SIMS) analysis of the N_2O-plasma-treated TFT showed a lower H concentration in the surface region of a-SiN_x layer and a higher O concentration at the interface of a-SiN_x/a-Si:H, as compared to those of a TFT without plasma treatment. This incorporation of O atoms after N_2O-plasma treatment might degrade the N-rich condition of a-SiN_x film, resulting in a decrease of μ_{eff}.[4] Also, the reduction of the H concentration could lead to higher electrical stability of the N_2O-plasma-treated device, since the hydrogen-induced defects might be the trapping centers which induced the V_{th} shift.[8]

Table I. The refractive indices and thicknesses before and after different plasma treatments for the a-SiN_x layers grown on Si wafers.

Treatment	Thickness (nm)		Refractive Index (λ=632.9 nm)	
	Before	After	Before	After
N_2O-plasma	105.2	105.0	1.8441	1.8448
NH_3-plasma	102.8	102.5	1.8445	1.8433

Table II. A summary of some electrical parameters for these three kinds of a-Si:H TFTs.

Treatment	V_{th} (V)	μ_{eff} ($cm^2/V\cdot s$)	S (V/decade)
Without	5.46~5.80	1.53~1.58	0.348~0.357
NH_3-plasma	5.96~6.40	1.22~1.24	0.467~0.491
N_2O-plasma	4.98~5.55	0.96~1.01	0.495~0.528

4. Conclusions

In conclusion, the obtained inverted-staggered a-Si:H TFTs with the N_2O-plasma-treated a-SiO_xN_y/a-SiN_x gate insulators had lower V_{th}, V_{th} shift and W_{FB}, as compared to those of the devices with NH_3-plasma treatment and without treatment. The BTS experiments also showed that the N_2O-plasma-treated device had a higher resistance against a prolonged positive gate bias. However, μ_{eff} of the N_2O-plasma-treated a-Si:H TFT obviously decreased. From the above results, we concluded that N_2O-plasma treatment of the as-deposited a-SiO_xN_y/a-SiN_x gate insulators could be used to improve the electrical stability of a-Si:H TFTs.

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