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Modified polycrystalline silicon chemical-vapor deposition process for improving roughness at oxide/polycrystalline silicon interface

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Abstract

A new modified low pressure chemical-vapor deposition process for stacked polysilicon (poly-Si) films is developed in this study. The proposed stacked film process combines polysilicon with amorphous silicon films. In this process, polysilicon film was deposited first at 630 °C, followed by a continuous temperature decrease down to 560 °C for the deposition of amorphous silicon film. It was found that the doped stacked polysilicon films deposited by this process result in lowering of surface roughness, together with reduction of the (311) phase of the doped amorphous silicon and (110) phase of the doped polysilicon. As a consequence, device performance based on the stacked films also improves. Results of surface roughness analysis indicated that the doped stacked polysilicon film has a root-mean square surface roughness (Rrms) of 78 Å, which is smaller than those of doped conventional (630 °C) polysilicon film (Rrms=97 Å), and doped amorphous silicon film (Rrms=123 Å, deposited at 560 °C). Transmission electron microscopic (TEM) observation performed at oxide/polysilicon interface showed that the conventional (630 °C) oxide/polysilicon interface has high angle grain boundaries on the polysilicon side, which may induce leakage current around the interfacial area.

Keywords: Annealing; Grain boundary; Silicon; Silicon oxide

1. Introduction

Polysilicon (poly-Si) films formed by low pressure chemical-vapor deposition with silane (SiH_4) was widely used in integrated circuits for various applications, such as metal-oxide-semiconductor (MOS) gates, interconnects, resistors, emitter contacts,…, etc. Other applications include photovoltaic conversion thin film transistor for large area liquid-crystal displays. The electrical performance of poly-Si is determined strongly by its microstructure, which depends on deposition parameters [1–4]. It was well known that the surface roughness of poly-Si degrades the electrical characteristics of dielectric film on poly-Si [5–7].

For devices adopting the double poly-Si floating-gate structure, the polyoxide requires a low leakage current and high breakdown electric field to obtain adequate data retention characteristics [6,8,9]. However, a nonuniform polyoxide film thickness and rough surface morphology at the oxide/poly-Si interface can cause the polyoxide to have a higher leakage current and lower dielectric breakdown field than those of silicon dioxide grown from a single crystalline silicon substrate [10–12]. This phenomenon is attributed to local electric field enhancement at the rough oxide/poly-Si interface. Moreover, the surface roughness of oxide/poly-Si interface would be

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enhanced after thermal oxidation [12–14]. Therefore, how to reduce the roughness of oxide/poly-Si interface is a critical issue to device performance.

Results of many previous studies showed that amorphous silicon (a-Si) has lower surface roughness than poly-Si [15–19]. However, after annealing or doping (e.g., with phosphorus or boron), the recrystallized a-Si film will exhibit some protrusions on the surface, which is induced by (311) texture and results in a nonuniform surface. Although such problem does not occur in doped poly-Si film deposited at temperatures >600 °C because of their better crystallinity and the (110) columnar structure [18,20], they tend to contain high-angle grain boundaries at the oxide/poly-Si interface. This will lead to nonuniform oxide film surface after oxidation and induce local electric field enhancement.

In this investigation, we developed a stacked poly-Si film process to improve both the (311) texture issue of doped a-Si and the high-angle grain boundary issue of doped poly-Si film. Surface roughness and oxide/poly-Si interface are analyzed by atomic force microscope (AFM) and transmission electron microscope (TEM). The electrical performance of thermally grown oxide on these two different doped poly-Si films was tested by an Al-gate nitride/oxide/poly-Si MOS capacitor structure. The mechanisms leading to the improvements in roughness and electrical performance will be discussed.

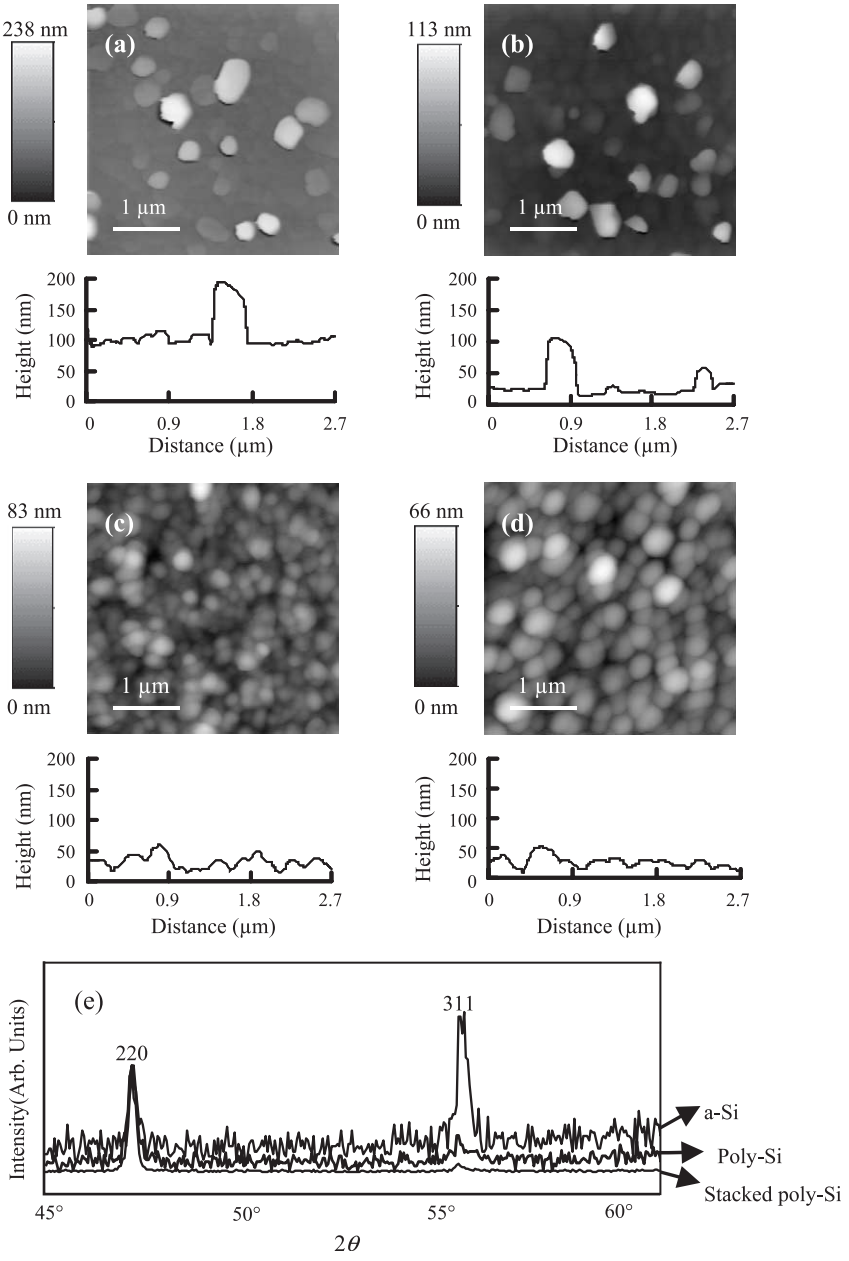

Fig. 1. AFM contact mode images and corresponding line scans of doped a-Si films deposited at (a) 540 and (b) 560 °C, (c) doped poly-Si films deposited at 630 °C and (d) stacked poly/poly-Si/a-Si films. X-ray diffraction results for the stacked poly/poly-Si/a-Si films are presented in (e).

2. Experimental details

All the samples used in this experiment were prepared by low pressure chemical-vapor deposition process and the deposition process was carried out in an induction-heated hot-wall horizontal reactor using monosilane (SiH_4) gas as a silicon source. P-type (100)-oriented silicon wafers with a resistivity of 8–12 Ω cm were used as substrates. The conventional poly-Si films were deposited at a fixed temperature (630 °C) while a-Si films were deposited at two different temperatures: 540 and 560 °C and all the deposition pressure was 0.11 Torr. The thicknesses of the poly-Si and a-Si films were about 4000 and 3000 Å, respectively, irrespective of the deposition temperature. According to the results on the phase dependence of deposition condition [15,17], we have chosen the deposition temperature of 560 °C and an even lower temperature of 540 °C to ensure that the as-deposited phase is a-Si. The stacked poly-Si films were deposited at 630 °C for 30 min, before decreasing the temperature down to 560 °C with a rate of 3 °C/min. The temperature was then held at 560 °C for 60 min without interrupting the deposition process; the total thickness was about 4000 Å. The as-deposited film was then doped with n-type phosphorus using $POCl_3$ gas at 950 °C and atmospheric pressure in an induction-heated hot-wall horizontal reactor. After a 5% HF solution deglazing for 3 min and RCA SC-1/SC-2 cleaning [21], atomic force microscope (Topometrix Explorer) with a resolution of 300×300 pixels was employed in contact mode to analyze the surface roughness. TEM (Phillips Tecnai 20 with field emission gun) interface analysis was made after oxidizing the doped poly-Si films at 950 °C and atmospheric pressure by dry oxidation, leading to a polyoxide thickness about 250 Å. The cross-sectional thin foils were prepared by mechanical thinning to 30 μm in thickness, followed by Ar^+ ion thinning (5 keV, 8° for 20 min) until perforation. TEM was operated at 200 keV and images were acquired with a Gatan CCD camera. Electrical characteristics of MOS dielectric films were measured by an HP4145B semiconductor parameter analyzer. The breakdown voltage was determined by ramp-voltage breakdown test with a ramp rate of 0.1 V/s on an area of 70×70 μm^2 and the breakdown criteria was 1 μA. An X-ray diffractometer (Diano 700) with Cu K_α radiation was employed to determine the texture microstructures of thin films.

3. Results

Fig. 1a–d shows the AFM images of doped a-Si (540 and 560 °C), doped poly-Si (630 °C), and doped stacked poly-Si films, respectively. From these images, it is clear that the doped a-Si films have apparent protrusions on the surface, (Fig. 1a and b), although most part of the surface area is

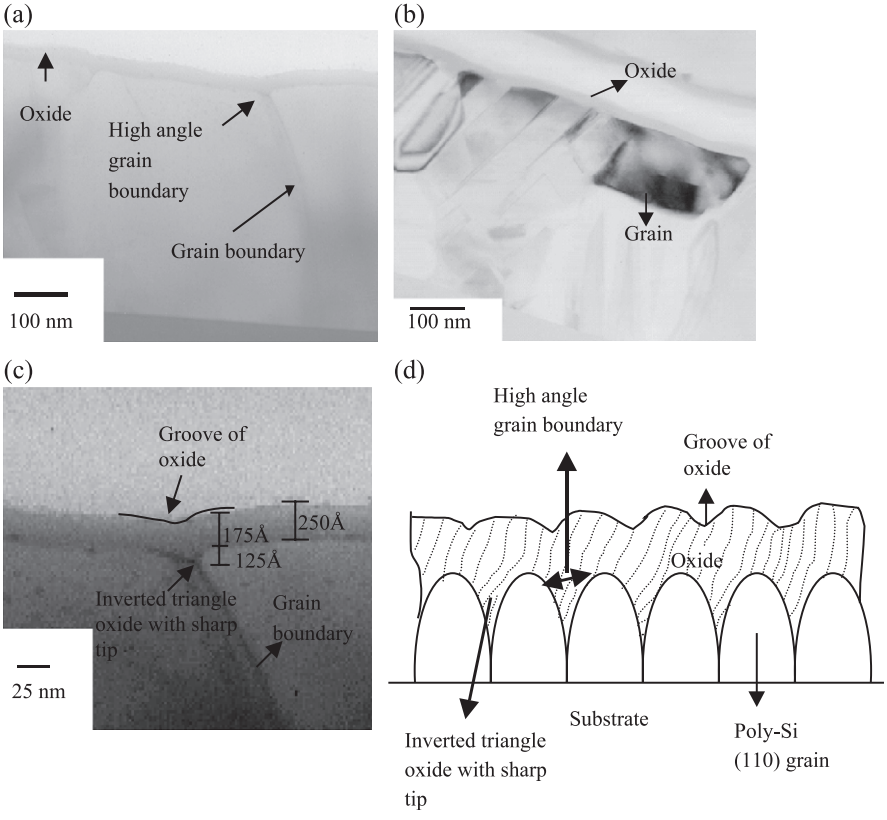

Fig. 2. TEM cross-section micrographs of (a) doped poly-Si and (b) doped stacked poly-Si, (c) the magnified image of (a) around the grain boundary region. A schematic representation of the interface is detailed in (d).

smoother than that of conventional doped poly-Si and stacked poly-Si films. Their corresponding line scans are also shown in Fig. 1 to demonstrate the variation of the surface roughness. Previous studies [15–18] attributed these protrusions to the appearance of a (311) texture after annealing of doped a-Si film. X-ray analysis result (Fig 1e) can clearly see that doped a-Si has highest (311) texture ratio, consistent with the previous studies [15–18]. Also we can see that the stacked poly-Si has least (311) texture ratio, even less than poly-Si. This protrusion will induce local electric field enhancement after oxidation. Because of the protrusion, doped a-Si films have high surface roughness counts with root-mean square surface roughness (Rrms) of 192 Å (540 °C) and 123 Å (560 °C), respectively. On the other hand, doped conventional (630 °C) poly-Si films (Rrms=97 Å) and doped stacked poly-Si films (Rrms=78 Å) have much smaller roughness than the a-Si/poly-Si. From the AFM images, it is also observed that doped stacked poly-Si films have narrow grain size distribution, compared with conventional doped poly-Si. The morphology of conventional doped poly-Si was sharper than stacked doped poly-Si films.

Fig. 2a and b shows the TEM images of oxide/poly-Si interface for conventional doped poly-Si and doped stacked poly-Si, respectively. From Fig. 2a, the doped conventional poly-Si films have (110) columnar grain structure, resulting in straight grain boundaries from polyoxide to the substrate and high angle grain boundaries in the oxide/poly-Si interface. These high angle grain boundaries were induced by the (110) texture columnar structure of doped poly-Si [15–18]. They will induce electric field enhancement, leading to a high leakage current in this area. Because of the recrystallization of a-Si on poly-Si, the doped stacked poly-Si layers do not exhibit (110) texture structure.

Fig. 3 shows the Weibull plots of electrical characteristics of doped stacked poly-Si versus conventional poly-Si films. For MOS capacitor applications, high charge to breakdown and high breakdown field are critical requirements to device performance. From the plot, clearly, higher breakdown voltage was observed for the dielectric film grown on stacked poly-Si. Enhanced electric field of MOS capacitor can be achieved in this case. It can be seen that the conventional poly-Si shows a much wider distribution of breakdown voltages than the stacked poly-Si. That is, the surface roughness of poly-Si film interface is higher than that of stacked poly-Si film.

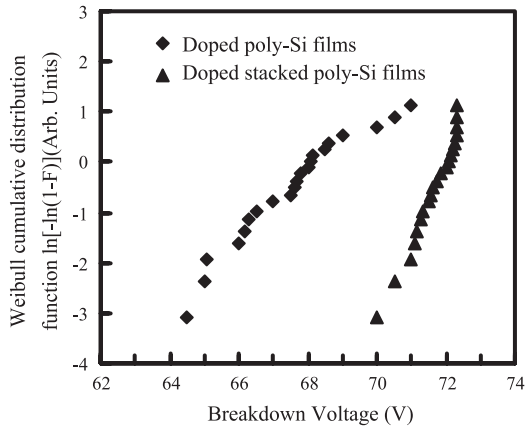

Fig. 3. Weibull plots of electrical characteristics of doped stacked poly-Si film versus conventional poly-Si film.

4. Discussion

According to the above results, one can see that doped a-Si films have a higher surface roughness than poly-Si. Poly-Si contains less (311) phase, but, instead, its (110) phase results in columnar grain structure, which induces high angle grain boundaries after oxidation and degradation in its breakdown strength. Fig. 2c is a magnified image of Fig. 2a around the grain boundary region. It is shown more clearly that, due to the high angle grain boundary, oxide forms an inverted triangle shape with sharp tip at a region adjoining two neighboring grains, causing a groove on surface. The thickness of the inverted triangle oxide is about 125 Å, half of the normal oxide thickness (250 Å). This structure seriously increases the roughness of oxide/poly-Si interface and easily results in local electric field enhancement at this region, which further induces higher leakage current and lower dielectric breakdown field. Fig. 2d is a schematic representation of the oxide/poly-Si interface in detail. From Fig. 2d, we can see that because the poly-Si is the periodic (110) columnar structure, it means that the inverted triangle oxide with surface groove also assume the periodic pattern. Therefore, the dielectric breakdown strength of poly-Si is limited by this structure. On the other hand, from Fig. 2b, the doped stacked poly-Si films with random grain structure do not have apparent periodic high angle grain boundaries, and thus prevent this issue. Apparently, both the doped a-Si and poly-Si suffered from the texture-induced surface roughening effect, and how to control the texture becomes a very important issue to device reliability.

The stacked poly-Si films contain a top a-Si layer and a bottom poly-Si layer. The top a-Si layer will recrystallize after impurity doping. Wang et al. [20] found that the recrystallization of a-Si film (deposited below 600 °C) results in poor crystallinity and low-angle grain boundaries, which give rise to smoother surface. As a consequence, the stacked poly-Si films should have a smoother surface than conventional poly-Si films. From the AFM image (Fig. 1d), one can also see that the recrystallization of the top layer of doped stacked poly-Si contains no distinct textures on the surface just as the doped a-Si did. Because of this recrystallization behavior, the upper layer of stacked poly-Si contains randomly oriented grain boundaries, it also contains no (110) columnar grain structure on the surface. This suggests that the doped stacked poly-Si can improve both the adverse texture effects of doped a-Si and doped poly-Si. This explains why the doped stacked poly-Si

structure has a smoother surface and better electrical performance than the other two.

5. Conclusion

In this study, doped stacked poly-Si films with lower surface roughness and smoother poly-Si/polyoxide interface than doped a-Si and conventional poly-Si films are developed. This new stacked poly-Si film has the poor recrystallization-induced crystallinity as in a-Si but no protrusion on surface and no apparent high angle grain boundaries. Results of electrical breakdown voltage measurements also show that the doped poly-Si film stack has a better performance than the doped conventional poly-Si film.

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