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Flaw detection and measurement for 4K Ultra HD thin-film-transistor array panel

Yao-Chin Wang [a,*], Bor-Shyh Lin [b,c], Kei-Hsiung Yang [b]

[a] Institute of Photonic System, National Chiao Tung University, Taiwan
[b] Institute of Imaging and Biomedical Photonics, National Chiao Tung University, Taiwan
[c] Department of Medical Research, Chi Mei Medical Center, Tainan, Taiwan

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ABSTRACT

Display pixels of liquid-crystal-display televisions (LCD TVs) on thin-film-transistor (TFT) array are getting smaller. This paper introduced the method of voltage imaging technique, which developed and provides initial insight into the thin-film-transistor array flaw detection and measurement for ultra-high-definition (Ultra HD, UHD) LCD TV application. We proposed the measurement of flaw detection, based on TFT array testing and characterization with respect to opto-electric transformation measurement.

1. Introduction

What is Ultra high-definition (Ultra HD) TV? On October 2012, the Consumer Electronics Association (CEA) announced that the official term "Ultra HD" would be used for any display with a 16 × 9 ratio with at least 1 digital input cable carrying a minimum resolution of 3840 × 2160 square pixels. In advanced TV display technologies, they have display high-resolution images in video devices and provide high quality broadcast enabled [1]. With more Ultra high-definition (Ultra HD), 4K Ultra HD, 4K2K, 4K UHD TVs, the "four times HD" TV technology has arrived with some advantage purpose in 2013.

Currently, there are 2 forms of Ultra HD, 4K and 8K, both have an aspect ratio of 16:9: 4K Ultra HD (2160p) has a resolution of 3840 × 2160 (8.3 megapixels), which is roughly equivalent to 4K cinema or 4 times the number of pixels in Full HD format (1080p), shown in Fig. 1. 8K Ultra HD (4320p) produces an astonishing 7680 × 4320 pixel resolution (33.2 megapixels), which is roughly the equivalent of 16 times the pixel resolution of Full HD (1080p). Some believe that Ultra HD technology raises Ultra HDTV.

Flaw detection plays a major role in mass production of quantitative visual tasks involving FPD cost and quality seen at different positions on the display maker [2]. Flaw detection is an important characteristic to measure in TFT array panels. Studies have shown that differences in-process positions relative to the testing method [3–6]. Thus, poor detection ability can lead to yield loss interpretation and difficult decrease controlling process accuracy in detection tasks. However, it is necessary to detect flaw with methodology of these high-resolution displays and establish testing in-process yield requirements on the performance. Resolution and sub-pixel structure differ greatly among display technologies. The general TFT array performance measurements include electrical characteristics tracking and flaw detection [7]; they impact the in-process quality, manufacture cost and yield managing.

Moreover, because 4K UHD TV displays are smaller in pixel size than normal TV displays. Resolution and pixel structure design differ greatly among display technologies. Measuring and detecting these characteristics provide information on how well the TFT array display panel. For

* Corresponding author.
E-mail address: autherkyn@gmail.com (Y.-C. Wang).

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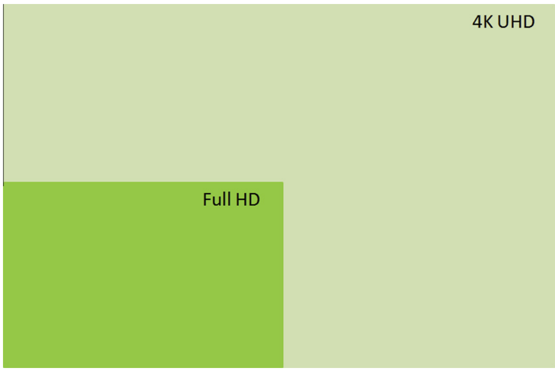

Fig. 1. 4K UHD (2160p) has a resolution of 3840 × 2160 (8.3 megapixels), which is roughly equivalent to 4K cinema or 4 times the number of pixels in Full HD format (1080p).

current testing equipment supplier, they still cannot provide good solution and face limitation for TFT array flaw detection in 4K UHD TVs. The paper was proposed the flaw detection enhancement by using voltage imaging technique and corrected.

2. Materials and methods

2.1. Classification of flaws

There are many types of flaws in a thin-film-transistor array. Normally, all flaws can be classification into two groups, one is line defect and the other one is pixel defect.

Line defect is classified according to which line is short or open. Few types of line defects are widely referred; gate open, data open, gate-to-gate short, data-to-data short, gate-to-data short, and data-to-com short.

Pixel defect is conventionally classified by its defected feature; TFT gate open, TFT data open, TFT pixel open, low TFT on-current, high TFT off-current, TFT via hole missing, pixel-to-data line short, pixel-to-gate line short, storage capacitor short, pixel-to-pixel short across data line or across gate line, data line residue under pixel, and amorphous silicon residue under pixel.

2.2. 4K Ultra HD thin-film-transistor array panel

In this study, a critical single small-pixel sized defect was detected by a material of 65″ TFT array of UHD display panel. The panel boasts ultra-high-resolution and the resolution quality of 3840 (R, G, B) × 2160. Fig. 2 is the material of 65″ TFT array of UHD display panel. Fig. 3 illustrated the layout of the TFT Array for detection.

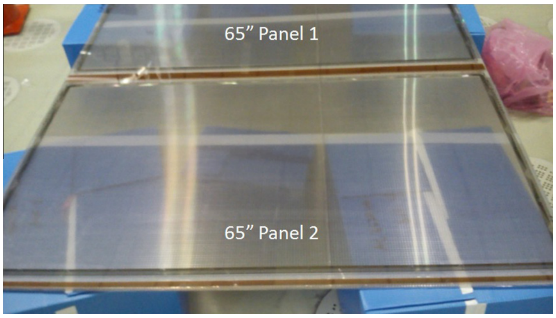

Fig. 2. The material of 65″ 4K UHD TFT array panel.

In an active-matrix thin-film-transistor array, the other source/drain terminal is connected to a transparent conductor, which is serves as one electrode of a capacitor and isolated from the surrounding pixels. A thin-film-transistor array panel generally consists of a two-dimensional array of each controlled pixel. There is one set of vertical metal lines and, on another plane, a second set of horizontal metal lines. The gate line is connected to the gate of a thin-film transistor at an individual pixel, and the data line is connected to one of its source and drain terminals. The two-dimensional array described is fabricated on a glass substrate and is called the active-matrix thin-film-transistor array.

2.3. Detection and measurement

We proposed an approach method of opto-electric transformation with TFT characterizing and testing operation theory is using voltage imaging technique. The measurement methodology proposed in this study is for flaw detection on TFT array panels.

In Fig. 4, the electro-optical modulator senses the induced voltage by pixels' electric fields and showed the measured pixel voltage with TFT characterizing, and then judging good pixels or bad pixels. Fig. 4(a) is measurement of opto-electric transformation with no voltage applied by modulator. Fig. 4(b) is pixel voltage by opto-electric

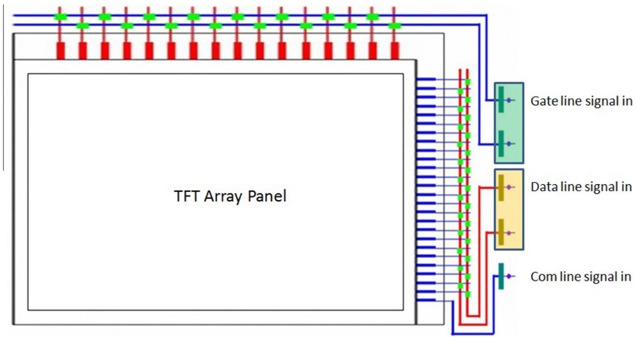

Fig. 3. Illustration of the layout of the TFT Array panel.

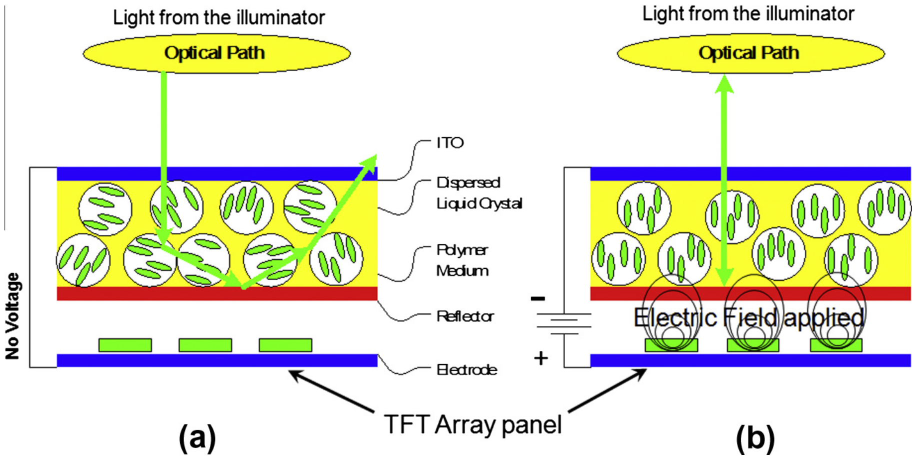

Fig. 4. (a) Measurement of opto-electrical transformation without voltage applied by modulator (b) with voltage applied by modulator.

transformation measurement with voltage applied by modulator. The bad pixels shown electrical leakage, induced pixel voltage drop caused by capacitive coupling due to data voltage drop be dV_{data}, and the pixel voltage drop, dV_{pixel} is expressed as follow,

$$dV_{pixel} = dV_{data} \cdot \left[C_{dp} \cdot X/(C_{dp} + C_{st} + C_{gd})\right],$$

where C_{dp} denotes the equivalent capacitance of bad pixels with electrical leakage. X is ratio of total area. C_{st} is the capacitance of storage capacitor. C_{gd} is the capacitance of TFT parasitic capacitor. In order to reduce the measurement noise, the voltage imaging technology uses four image acquisition frames, *a*, *b*, *c*, and *d*, to get the pixel voltage V_{pixel}, and V_{pixel} can be calculated as follow,

$$V_{pixel} = (V_a - V_b - V_c + V_d)/2,$$

where V_a is voltage denotes the frame a of voltage image acquisition. V_b is voltage denotes the frame b of voltage image acquisition. V_c is voltage denotes the frame c of voltage image acquisition. V_d is voltage denotes the frame d of voltage image acquisition. V_{pixel} is voltage denotes the pixel voltage.

Fig. 5 shows the comparison of normal and defective pixels under the driving pattern. In this case, the measured voltage of the normal pixel (VN), the defective pixel with pixel point defect (VD1), and the pixel broken with data line open (VD2) of critical small-pixel flaws are calculated as follows: VN = 20.74 V, VD1 = 10.96 V, and VD2 = −21.22 V. The overlap capacitance is assumed to be 0.035 pF for pixel electrode and data line overlap and 0.7 pF for the leakage short with data lines. Therefore, the voltage difference between the normal pixel and the defective pixel is large enough to differentiate them. It is not considered the line delay of both gate line and data line; the real whole plate might be different from these data of the measured voltage. It might induce larger voltage drop because of larger overlap capacitance.

However, the overlap capacitance is assumed for pixel electrode and data line overlap; also for the leakage short with data-to-data. So, the voltage difference between the normal pixel and the defective pixel is enough large to differentiate them. In order to enable detecting and improve detection capability for a pixel-to-pixel short defect and the small-pixel sized defect, two adjacent pixels need to

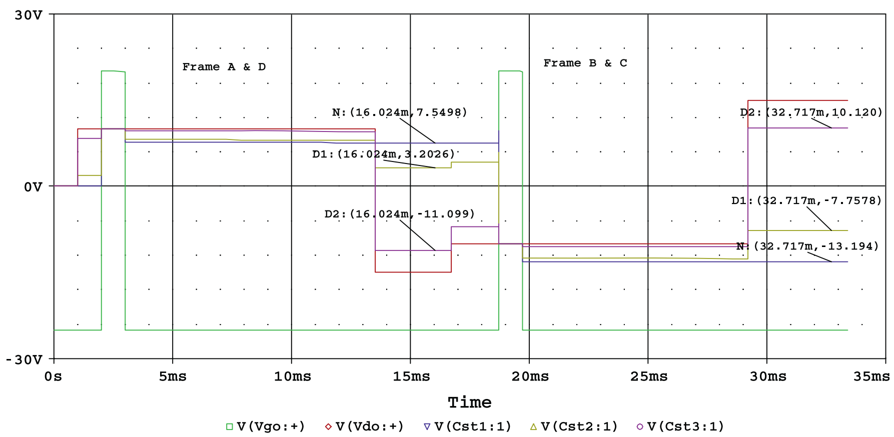

Fig. 5. Comparison of normal and defective pixel under the driving pattern. Here, VN denotes the normal pixel, VD1 denotes the defective pixel with pixel point defect, and VD2 denotes the pixel broken with data line open.

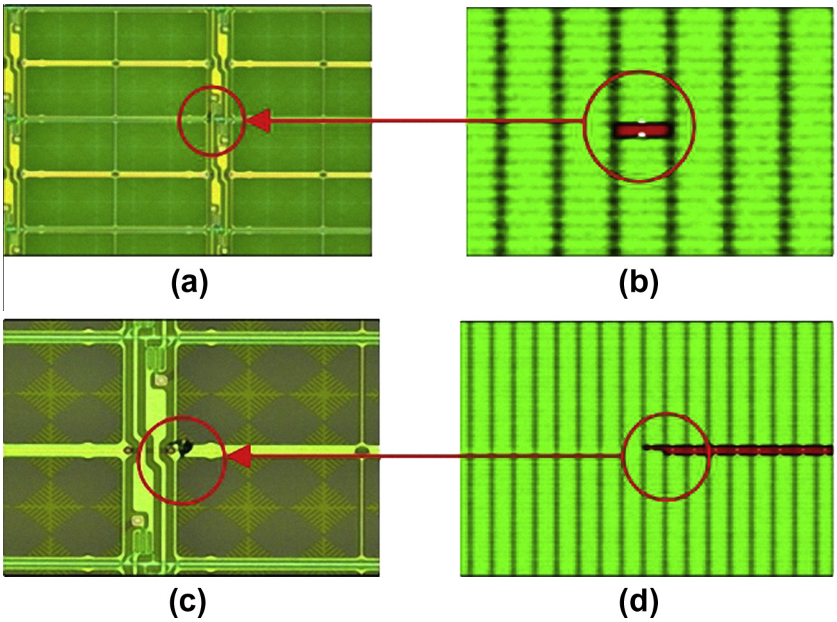

Fig. 6. The critical defects were detected (a) pixel point defect review, (b) the voltage imaging of (a), (c) pixel data line broken review, and (d) the voltage imaging of (c).

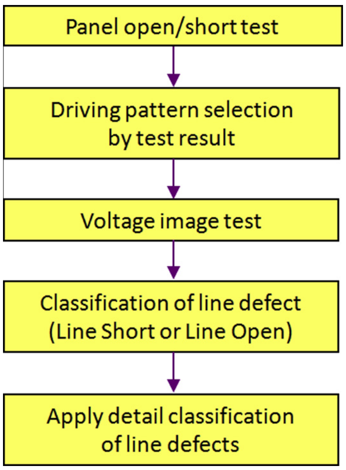

Fig. 7. The flow chart showing different steps of the implementation process.

Table 1
The different detection types, and sensitivity of this technique in terms of detecting. (Y = yes, N = no, P = partial).

Defect type	Detecting
Gate/data open	Y
Gate-to-data short	P
Data-to-data short	P
TFT gate/data/pixel open	Y
TFT via hole missing	Y
Low TFT on-current	Y
High TFT off-current	Y
Pixel-to-data/gate line short	Y
Storage capacitor short	Y
Pixel-to-pixel short across data/gate line	Y
Data line residue under pixel	P
Amorphous silicon residue under pixel	P
Special defects of interlayer	N

have an opposite polarity of voltage that makes the voltage of the defect to be 0 V.

3. Experimental results

The voltage step between two consecutive gray levels to differentiate a defect from a small-pixel sized of sub-pixel. It should be drop down larger particle in order to detect a single defect. A data line residue under pixel and an amorphous silicon residue under pixel point were detected. The data line broken area between the residues form a capacitor and a small voltage is generated in these types of defects due to this variation capacitance.

The detected critical pixel point and data line broken defects are shown in Fig. 6. The artificial defects were detected, Fig. 6(a) is pixel point defect review, Fig. 6(b) is the voltage imaging of Fig. 6(a) and (c) is the pixel data line broken review, Fig. 6(d) is the voltage imaging of Fig. 6(c). Fig. 7 is the flow chart showing different steps of the implementation process. And, Table 1 shows the different detection types, and sensitivity of this technique in terms of detecting.

4. Discussions

The defect detection capability for voltage imaging technique, it depends on the inter-digitized shorting bar design configuration as well as the driving pattern. The designed shorting bar configuration provides the highest defect detection capability. The driving voltage presented in this report is just an example. It should be modified for each customer's process, because each customer has his own design parameters such as a storage capacitor capacitance, shorting bar resistance, TFT on and off current, TFT parasitic capacitance, and display technologies. The defect type of TFT array was reviewed and new application was developed to detect small-pixel sized defects capability. The flaw detection on 4K UHD TFT array, it estimates to get better reporting.

5. Conclusions

In the past, it is difficult to differentiate a defect from a small-pixel sized and also suffer the limitation of detecting the critical defect in small-pixel-sized TFT array and facing an unstable charge density and array structure with optical-sensing sensitivity issue [3]. The electron beam schemes only can inspect a few kinds of flaws and detected, and it also demands of high stability of the instruments and long working time for them [5]. For the electrical testing scheme requires a large number of contact pins for direct contact and measurement, it should be take higher cost, longer working-time for product-line [6]. The results presented here is including critical electrical leakage pixel defect, and is useful in identifying the causes of array defects on the in-process small pixel panels testing. Furthermore, the TFT array testing can be applied into the in-line testing of TFT array process for yield managing. It is enhancing the testability of TFT array with high-resolution display panels' inspection [8–11]. An effective electrical testing scheme depends on the configuration of pixel circuit and panel design by using this proposed testing, it can be examined defects before LCD assembly is performed [12]. The proposed testing scheme can be detected without any hard contact and panel damage during in-process detection.

Acknowledgments

The Voltage Imaging Technique is a trademarked proprietary technology used in the in-process testing systems from PDI and Orbotech.

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