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Design of high-voltage-tolerant stimulus driver with adaptive loading consideration to suppress epileptic seizure in a 0.18-μm CMOS process

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Abstract A novel design of high-voltage-tolerant stimulus driver for epileptic seizure suppression with low power design and adaptive loading consideration is proposed in this work. The proposed design can deliver the required stimulus current within a specific range of loading impedance. Besides, this design in 0.18-μm low-voltage CMOS process can be operated with high supply voltage (V_{CC}) of 5–10 V without using the high-voltage transistors, and the process steps of high-voltage transistors can be reduced. The proposed design can be further integrated for an electronic epilepsy prosthetic system-on-chip.

Keywords Adaptive loading · Epileptic seizure suppression · High-voltage tolerance · Implantable device · Stimulator · System-on-chip (SoC)

1 Introduction

Epilepsy is one of the common neurological diseases, which is caused by transient abnormal discharge in brain [1]. Approximately 1 % of the people in the world are affected by this seizure [2]. If this seizure cannot be well controlled, patients will suffer from defects in sensations, emotions, memories, and other related activities. Pharmacologic treatments are the most common way used to suppress epileptic seizure [3]. There are more than 20 types of medications, and each is developed for specific type of epileptic seizure. However, there are still many patients who do not respond to medications. For these medically refractory patients, the surgical treatment is used to remove some tissues from brain [4]. It is a risky treatment because patients may lose some physical functions permanently after taking the surgery. In addition, there is no guarantee that epileptic seizure can be cured completely by surgery.

Recently, it has been demonstrated that the abnormal discharge signal to cause epilepsy can be suppressed by electrical stimulation as the epileptic seizure happens [5, 6]. Comparing with the traditional treatments, the electrical stimulation is safer, flexible, recoverable, and non-destructive. Some epilepsy control systems have been studied [7]. Besides, opposed to an open-loop seizure control system, a closed-loop system is more plausible for seizure control [8]. Figure 1 shows the functional block diagram of the closed-loop epileptic seizure monitoring and controlling system in an implantable device [9]. This implantable device consists of the signal conditioning, microcontroller, and stimulator to form a closed-loop seizure controller. The stimulus current is 20–50 μA, which is able to suppress epileptic seizures of Long-Evans rats. Since the stimulus current is conducted by a 4-microwire bundle, each made of Teflon-insulated stainless steel wire, to stimulate the right-side zona incerta, the effective loading impedance of electrode and brain tissue varies from 100 to 250 kΩ. That is to say, the required stimulus voltage (2–12.5 V) is much higher than the supply voltage of the system (V_{DD} = 1.8 V).

Due to the low cost for mass production, CMOS technologies are more attractive to realize the implantable device for biomedical electronics applications [10]. For system-on-chip (SoC) purpose, the microcontroller and signal conditioning blocks in the implantable device can be

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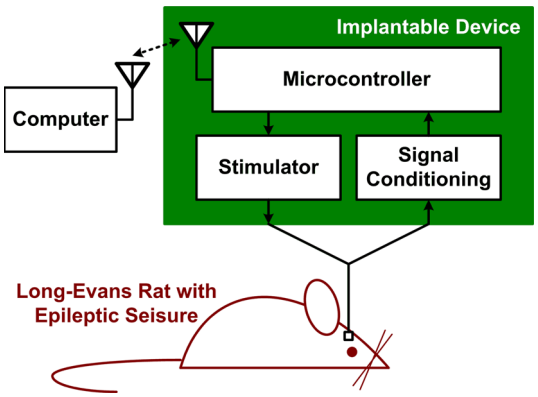

Fig. 1 Block diagram of implantable device for epileptic seizure suppression

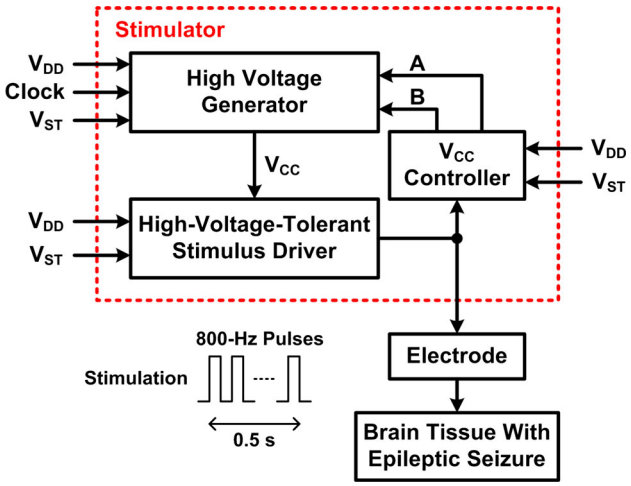

Fig. 2 Block diagram of high-voltage-tolerant stimulator with adaptive loading consideration

realized in low-voltage CMOS process [11, 12]. Furthermore, the microcontroller and signal conditioning blocks for the epileptic seizure monitoring and controlling SoC realized in 0.18-μm CMOS process have been presented recently [13, 14]. Besides, a stimulator with high-voltage tolerance and adaptive loading consideration is also needed.

In this work, a high-voltage-tolerant stimulator with low power design and adaptive loading consideration in a 0.18-μm 1.8-V/3.3-V CMOS process is proposed. Without using the high-voltage transistors, the process steps can be reduced, the fabrication yield can be increased, and the chip cost can be lowered. A stacked MOS configuration was used in this work to prevent from reliability issues such as electrical overstress. The proposed stimulator can deliver the required stimulus current within the loading impedance of 100–250 kΩ. The detailed design procedures and simulation/measurement results of the stimulator will be presented in Sects. 2 and 3. The performances of this work and those of the reported stimulators will be compared in Sect. 4. The animal test results with the silicon chip and discrete components in the closed-loop epileptic seizure monitoring and controlling system will be presented in Sect. 5.

2 Proposed high-voltage-tolerant stimulator

The proposed stimulator consists of the high-voltage-tolerant stimulus driver, V_{CC} controller, and high voltage generator, as shown in Fig. 2. A 1.8-V system supply voltage (V_{DD}), a 25-MHz clock, and a stimulation signal (V_{ST}) are used in this circuit. The stimulus current can be sent to the brain tissue with epileptic seizure through the electrode.

Once the signal conditioning block in Fig. 1 detected the epileptic seizure, the stimulator becomes active. The stimulus current of pulses with 800-Hz frequency, 40 % duty cycle, 20–50-μA amplitude, and 0.5-s duration is used to suppress the seizure [9]. The required supply voltage for stimulus driver (V_{CC}) is varied from 4 to 10 V.

As stimulator active, the stimulation signal V_{ST} is sent to control the high-voltage-tolerant stimulus driver. The stimulus driver receives the V_{DD}, V_{ST}, and variable voltage V_{CC}, and then delivers the stimulus current to brain tissue through the electrode. The V_{CC} controller detects the stimulus current, and then sends the control signals A and B to the high voltage generator. The high voltage generator receives the clock signal, V_{DD}, and the control signals A and B, and then delivers variable voltage V_{CC} to the stimulus driver. The detailed circuit design procedures of each block to operate in the loading impedance of 100–250 kΩ will be discussed in following paragraphs.

2.1 High-voltage-tolerant stimulus driver and V_{CC} controller

In this work, the loading impedances (R_L) within 100 and 250 kΩ are divided into four operating regions, which are 100–133, 133–168, 168–213, and 213–250 kΩ, respectively. Each region adopts its suitable voltage level of V_{CC}. Figure 3 shows the design of high-voltage-tolerant stimulus driver and V_{CC} controller. Both 1.8-V transistor (shown with white gate oxide) and 3.3-V transistor (shown with gray gate oxide) in commercial 0.18-μm CMOS process are used. The sizes of transistors in the stimulus driver are listed in Table 1.

In the stimulus driver of Fig. 3, the stacked MOS configuration with 3.3-V transistors is used between V_{CC} and GND to sustain ~10 V without the electrical overstress issue [15]. The stimulus driver consists of input stage (1.8-V inverters), bias circuit (R_1 resistor chain), level

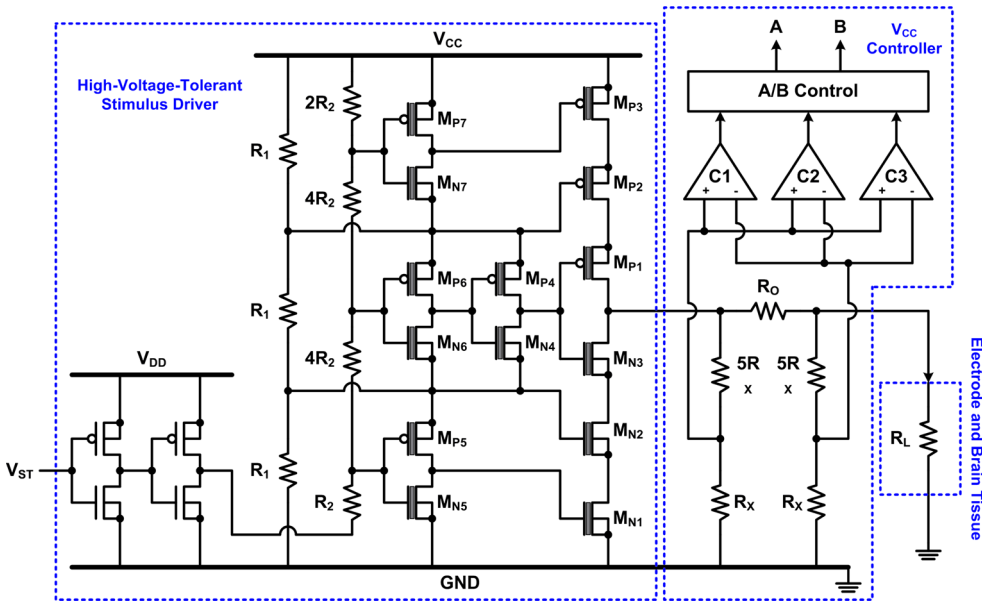

Fig. 3 Circuit schematics of proposed stimulus driver and V_{CC} controller

Table 1 Sizes of transistors in stimulus driver

PMOS	Width/length	NMOS	Width/length
M_{P1}	10 μm/0.5 μm	M_{N1}	1 μm/0.5 μm
M_{P2}	10 μm/0.5 μm	M_{N2}	1 μm/0.5 μm
M_{P3}	10 μm/0.5 μm	M_{N3}	1 μm/0.5 μm
M_{P4}	2.5 μm/0.5 μm	M_{N4}	1 μm/0.5 μm
M_{P5}	2.5 μm/0.5 μm	M_{N5}	1 μm/0.5 μm
M_{P6}	2.5 μm/0.5 μm	M_{N6}	1 μm/0.5 μm
M_{P7}	2.5 μm/0.5 μm	M_{N7}	1 μm/0.5 μm

Table 2 Relationship of V_{CC}, V_{Ro1}, V_{Ro2}, and A/B in stimulus driver and V_{CC} controller

V_{CC} (V)	V_{Ro1} (V)	V_{Ro2} (V)	Control Signals (A/B)
5.04	<0.61	<0.60	0/0
6.48	0.61–0.80	0.60–0.79	0/1
7.92	0.80–0.98	0.79–0.97	1/1
9.36	>0.98	>0.97	1/0

shifter (R_2 resistor chain), control circuit (3.3-V inverters), and output stage (stacked 3.3-V MOS). Besides, the deep N-well layer is used to isolate the P-well region of each stacked NMOS from the common P-substrate. At the input stage, two inverters with 1.8-V transistors play the role of input buffer with 1.8-V V_{DD}. The R_1 resistor chain, which consists of diode-connected MOS, is used to provide the bias voltages of $2V_{CC}/3$ and $V_{CC}/3$. The other R_2 resistor chain, which consists of diode-connected MOS with smaller width/length ratio, acts like the level shifter to transfer 1.8-V signal to high-voltage one. The 3.3-V inverters receive the high-voltage signals and then control the output stage. The PMOS and NMOS in output stage are well controlled to turn on or off during stimulation on or off.

Within four operating regions, which R_L are 100–133, 133–168, 168–213, and 213–250 kΩ, the voltage levels of V_{CC} are selected to 5.04, 6.48, 7.92, and 9.36 V, respectively. The stimulation on/off is controlled by the 1.8-V signal V_{ST}. Whether the stimulation is turned on or off, all voltage differences across the MOS transistors are lower then their sustainable voltages (1.8 or 3.3 V) to prevent from reliability issues. Even if the temperature varies from −25 to 125 °C, the simulation result shows that each 1.8- or 3.3-V transistor sustains only 1.8 or 3.3 V at most.

In the V_{CC} controller of Fig. 3, an output resistor ($R_O = 2$ kΩ) is arranged before the electrode and brain tissue. The voltage difference between R_O (V_{Ro1}–V_{Ro2}) is divided by R_X resistor chains, and then distinguished by comparators (C1, C2, and C3). Each comparator has the designed transfer curve to detect the voltage difference between R_O. Once the voltage difference between R_O is smaller than 0.08 V, which is obtained from 40 μA × 2 kΩ, the control signals A/B will change. The V_{CC} controller sends out A/B signals as 0/0 → 0/1 → 1/1 → 1/0. Controlled by the A/B signals, the high voltage generator delivers suitable V_{CC}.

At the beginning of each stimulation ($V_{ST} = 1.8$ V), the control signals A/B are 0/0 and the high voltage generator starts to deliver 5.04-V V_{CC}, the stimulus current flowing through R_O is higher (lower) than 40 μA if the R_L is lower (higher) than 133 kΩ. Once the stimulus current flowing through R_O is lower than 40 μA, the voltage difference between R_O is smaller than 0.08 V, and the control signals A/B will transfer from 0/0 to 0/1 to switch the V_{CC} to

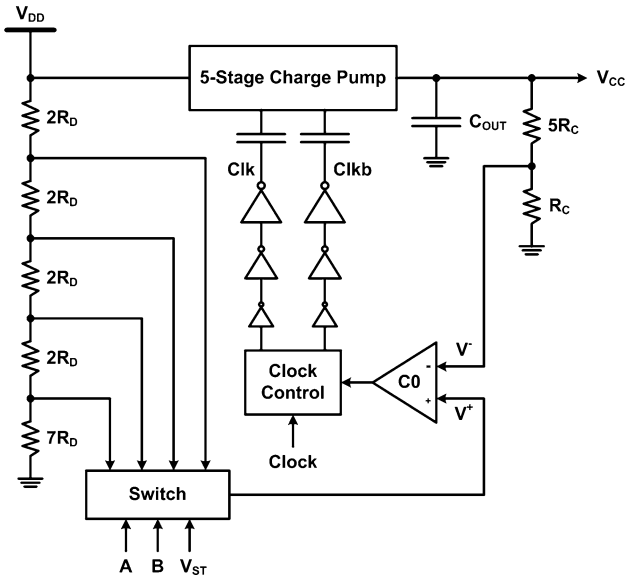

Fig. 4 Design of high voltage generator with adjustable output voltage (V_{CC})

6.48 V. In this state, the stimulus current flowing through R_O is higher (lower) than 40 μA if the R_L is lower (higher) than 168 kΩ. Once the stimulus current flowing through R_O is lower than 40 μA again, the control signals A/B will transfer from 0/1 to 1/1 to switch the V_{CC} to 7.92 V. If the stimulus current is still lower than 40 μA, which means the $R_L > 213$ kΩ, the control signals A/B will transfer to 1/0 to switch the V_{CC} to 9.36 V. The stimulus driver can therefore deliver 40 ± 10 μA stimulus currents with various loading impedance. After one pulse of stimulation during 0.5 ms, the A/B signals return to 0/0. This operating procedure is also shown in Table 2 with the required V_{CC} and the voltage between R_O (V_{Ro1} and V_{Ro2}).

After each stimulation, the stimulator is turned off ($V_{ST} = 0$). The stimulus driver keeps the electrode and brain tissue grounded to prevent from charge storing in brain.

2.2 High voltage generator

As shown in Fig. 4, the high voltage generator consists of voltage dividers (resistors), A/B/V_{ST}-controlled switch, comparator (C0), clock control, clock buffers, and 5-stage charge pump circuit. The clock control is used to generate interweaved signals (Clk and Clkb) which depend on the reference clock and the output signal of comparator. One of the input voltages of comparator (V^-) is $V_{CC}/6$, while the other one (V^+) is $7V_{DD}/15$ (0.84 V), $9V_{DD}/15$ (1.08 V), $11V_{DD}/15$ (1.32 V), or $13V_{DD}/15$ (1.56 V), according to the operating regions. The used 5-stage charge pump circuit is shown in Fig. 5. This charge pump circuit has been studied without suffering the gate-oxide reliability issue [16]. As shown in Fig. 5, there are two charge transfer branches. The control signals of two branches are intertwined. The clock signals (Clk and Clkb) are out-of-phase but with the amplitude of V_{DD}. When the clock signals of first, third, and fifth pumping stages in first branch are Clk, those in second branch are Clkb. Similarly, when the clock signals of second and forth pumping stages in first branch are Clkb, those in first branch are Clk. Since the clock signals of two branches are out-of-phase, the output voltage (V_{CC}) can be pumped to high alternately. To avoid the body effect, the bulks of the transistors in the charge pump are connected to their sources. The output voltage of the 5-stage charge pump circuit with 1.8-V V_{DD} supply can be ideally pumped up to ∼10 V.

At the beginning of first stimulation, there is no charge stored at the output capacitor of high voltage generator (C_{OUT}), and output voltage of high voltage generator (V_{CC}) is initially 0 V. Since the V^+ is higher than the V^-, the high voltage generator is activated, and the output voltage of high voltage generator increases. The charge pump keeps activated until the V^- is slightly higher than V^+. The feedback loop in the high voltage generator keeps the charge pump circuit delivers the required V_{CC}. After each stimulation, the V^+ is set to 0 V as $V_{ST} = 0$, and the high voltage generator stops pumping until next stimulation.

3 Simulation and measurement results

The proposed high-voltage-tolerant stimulus driver and V_{CC} controller have been fabricated in a 0.18-μm 1.8-V/3.3-V CMOS process. Figure 6 shows the chip photograph. This circuit occupies a chip area of 100 × 160 μm^2. Under measurement, Agilent E3631A is used to provide the fixed 1.8-V V_{DD} and the adjustable V_{CC}. HP 33120A is used to supply the stimulation signal V_{ST} to enable the stimulator. Tektronix 3054B is used to observe stimulus voltage/current of the stimulator.

Figure 7 shows the measured stimulus currents passing through resistors, where 100- and 250-kΩ resistors are used to represent the equivalent loading impedance on simulating site. Besides the purely resistive model, some electrodes may be modeled as a series resistor and capacitor. The measured stimulus currents with 100-kΩ/250-kΩ loading resistor and 1-μF loading capacitor in series ($R_L + C_L$) are shown in Fig. 8. The stimulus current of pulses are not degraded by additional loading capacitor. Figure 9 summarizes the measured stimulus currents as the loading impedance varies from 100 to 250 kΩ. The stimulus current of proposed design maintains 40 ± 10 μA with various loading impedance. Besides, the A/B signals can be correctly sent out. The power consumption is ∼1 mW (∼2 mW) under 100-kΩ (250-kΩ) loading impedance.

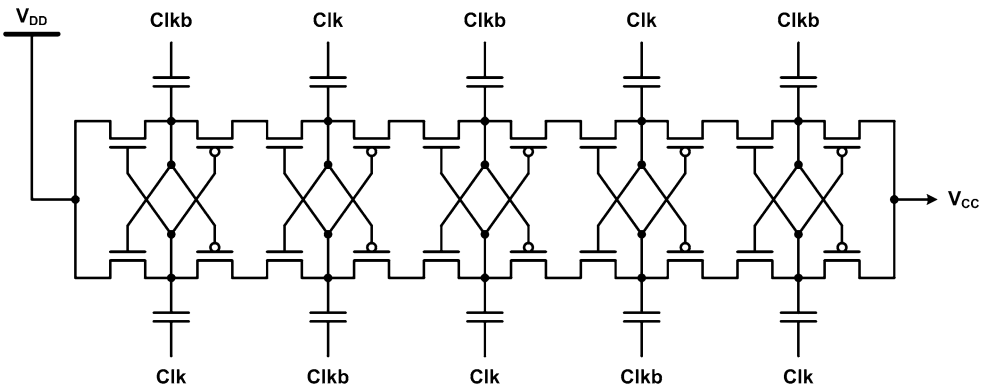

Fig. 5 Schematic circuit of 5-stage charge pump

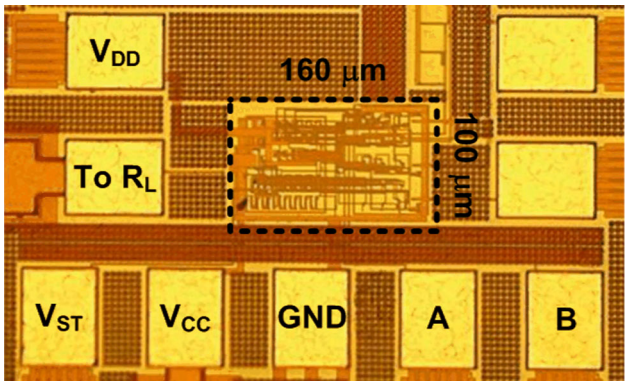

Fig. 6 Chip photograph of high-voltage-tolerant stimulus driver and V_{CC} controller

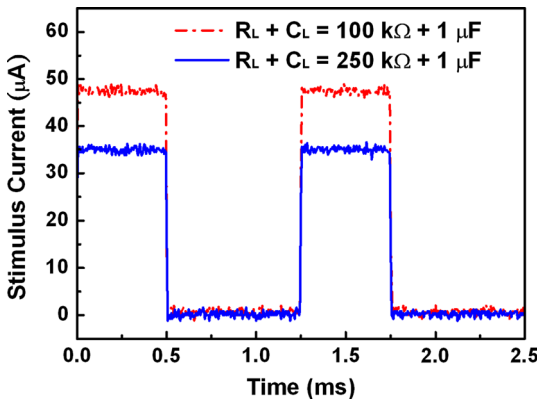

Fig. 8 Measured stimulus currents with resistive and capacitive loading impedance ($R_L + C_L$)

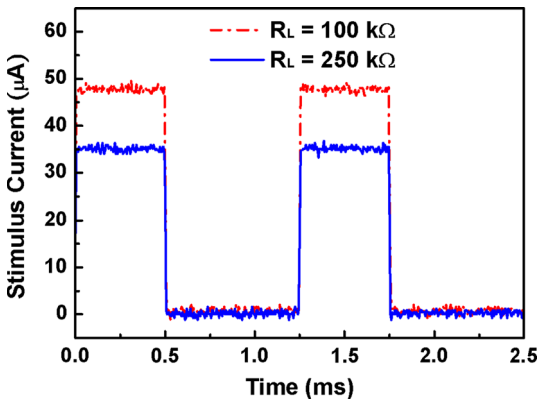

Fig. 7 Measured stimulus currents with resistive loading impedance (R_L)

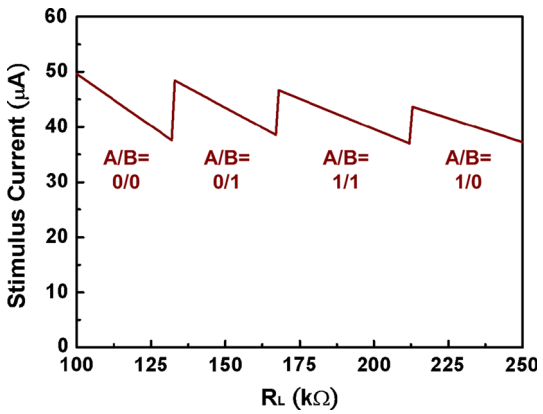

Fig. 9 Measured stimulus currents and control signals A/B under different loading impedance (R_L)

The layout area of the high voltage generator in the 0.18-μm CMOS process is about 500 × 1,100 μm^2. Due to the limitation in area of test chip, the high voltage generator has not been integrated in the stimulator. Even so, the high voltage generator with adjustable output voltage is also simulated in this work. The high voltage generator has been simulated in HSPICE with the same 0.18-μm CMOS process. Figure 10 shows the simulated voltage waveforms of V_{CC} in four operating regions. Table 3 summarizes the simulated performances of the high voltage generator, including the V_{CC}, peak-to-peak ripple voltage in V_{CC} (V_{PP}), total power consumption, and the transition time from previous operating region to itself. As the A/B signals are 0/0, 0/1, 1/1, and 1/0, the output voltages of high voltage generator are 5.09, 6.51, 7.98, and 9.42 V, respectively, which are closed to the required V_{CC} for stimulus driver.

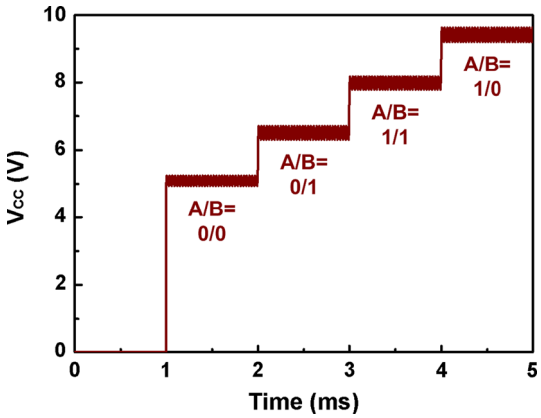

Fig. 10 Simulated voltage waveforms of V_{CC} under different control signals A/B

Table 3 Simulated performances of high voltage generator

Control Signals (A/B)	Output V_{CC} (V)	Output V_{PP} (V)	Power consumption (mW)	Transition time (μs)
0/0	5.09	0.30	1.21	1.08
0/1	6.51	0.40	1.27	1.17
1/1	7.98	0.39	1.56	0.92
1/0	9.42	0.42	2.15	1.39

Table 4 Comparison among stimulators in recent literature

	[17]	[18]	This work
CMOS process (μm)	0.8	0.35	0.18
	5 V/20 V	3.3 V/24 V	1.8 V/3.3 V
Loading impedance (kΩ)	100	24–200	100–250
Stimulus current (μA)	136	30	40 ± 10
Supply voltage (V)	8.95	12–22	1.8

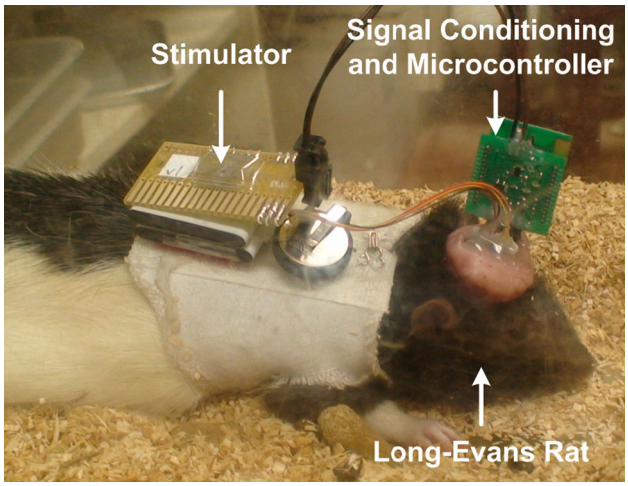

Fig. 11 Measurement setup for animal test

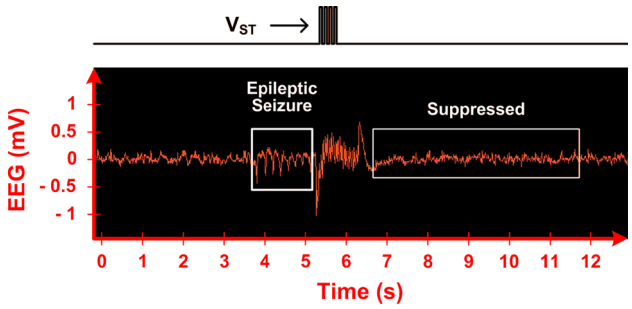

Fig. 12 Experimental result on EEG signal of Long-Evans rat

4 Discussion and comparison

The comparison among the reported on-chip stimulators in recent literature [17, 18] and this design is summarized in Table 4. To sustain high stimulus voltage caused by the product of loading impedance and stimulus current, high-voltage processes are usually used. In this work, the stimulator has been designed to deliver the required stimulus current and to sustain high voltage in low voltage process. Without using the high-voltage transistors, the stimulator can be integrated with the microcontroller and signal conditioning blocks into a chip.

5 Animal test

The fabricated chip of the proposed stimulus driver and V_{CC} controller is further integrated into the closed-loop epileptic seizure monitoring and controlling system for animal test, as shown in Fig. 11. All experimental procedures have been reviewed and approved by Institutional Animal Care and Use Committee of National Cheng-Kung University, Taiwan.

Although the charge pump system has not been integrated in the chip, the V_{CC} voltage is provided from the external supply. In this experiment, the stimulus current is conducted by a 4-microwire bundle, each made of Teflon-insulated stainless steel. Whenever the system detects an epileptic seizure, the proposed stimulator is activated to stimulate the Long-Evans rat. Figure 12 shows the electroencephalography (EEG), where the epileptic seizure with abnormal discharge is detected during 3.5–5 s, and the microcontroller activated the proposed stimulator. At this measurement, the loading impedance is measured to be $\sim$150 kΩ, and the required V_{CC} is 6.48 V. After stimulation, the intensive and rapidly brain activity in Long-Evans rat is suppressed.

6 Conclusion

Design of high-voltage-tolerant stimulator for electronic epilepsy prosthetic SoC in a 0.18-μm CMOS process is

proposed. The stimulator consists of the high-voltage-tolerant stimulus driver, V_{CC} controller, and high voltage generator. The proposed design with 1.8- and 3.3-V transistors can operate within 5.04 and 9.36 V without electrical overstress issues. The functions of the high-voltage-tolerant stimulus driver and V_{CC} controller have been verified in silicon chip. While the loading impedance varies from 100 to 250 kΩ, the proposed design can deliver required stimulus current.

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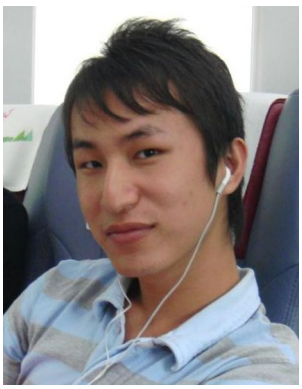

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