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Introductory Invited Paper

Single-trap-induced random telegraph noise for FinFET, Si/Ge Nanowire FET, Tunnel FET, SRAM and logic circuits

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ABSTRACT

In this paper, we comprehensively review the impacts of single-trap-induced random telegraph noise (RTN) on FinFET, Ge/Si Nanowire FET and Tunnel FET (TFET). The resulting influences on the thermionic-based current conduction such as FinFET, Si-NW FET and Ge-NW FET (at low drain bias) as well as interband tunneling dominated current conduction such as TFET and high-drain-biased Ge-NW FET are extensively addressed in device and circuit level. The location of the trap is shown to have profound impacts and the impacts vary with bias conditions and trap types. The worst-case analysis of the stability/performance and leakage/delay for all possible trapping/detrapping RTN combinations are investigated for FinFET, Si-/Ge-NW FETs and TFET based 6T/8T SRAM cells and logic circuits.

1. Introduction

With aggressive MOSFET scaling, the number of constituent atoms (including semiconductors, insulator materials and dopant species) as well as number of defects in a single transistor reduces to the countable regime with few atomic layers or traps inside the device [1,2]. The sparse and discrete charge and matter immensely aggravate device variability and hinder circuit functionality [3,4]. Among the existing variation sources, random telegraph noise (RTN) caused by the trapping/detrapping of conducting carriers by/from individual traps at the interface [5–7], exhibits stronger geometry dependence on active area [8–14] and long-tailed distribution that could exceed the impact of random dopant fluctuation for planar BULK MOSFETs at 22 nm and beyond [8–10]. In addition, the increasing importance of RTN with decreasing channel carriers [12,15–18] poses a stringent obstacle to supply voltage scaling for low-power applications.

Fig. 1(a) shows the typical syndrome of a two-level drain current (I_D) fluctuation varying with time in the presence of a single trap [5,6,19]. In Fig. 1(a), several important parameters are demonstrated: time-to-capture (τ_c), time-to-emission (τ_e) and amplitude (ΔI_D) which indicate the time elapsed to capture and emit a carrier from the trap point of view and the resulting influence on magnitude of I_D fluctuation due to the trapping/detrapping of the carrier, respectively. Over long period of time, the values of τ_c and τ_e are random and found to follow Poisson distribution (Fig. 1(b)) [5] while the magnitude of ΔI_D is essentially constant for a given condition. The impact of I_D fluctuation due to RTN changes the device strength similar to other static variation sources (such as random dopant fluctuation). On the other hand, the transient properties of time constants (τ_c and τ_e) in RTN are shown to introduce unique variations depending on the cell access history (single access or multiple accesses), trap characteristics and previous states for SRAM stability and logic delay [9,20–22].

Numerous previous studies focused on the measurement, characterization and theoretical assessment of RTN for planar BULK MOSFETs. In [8–10,20,23–24], the characteristics of RTN are examined through extensive measurements from large amount of well-designed samples. It is found that because of its log-normal distribution [8–10], RTN induced threshold voltage (V_T) variation may overwhelm the contribution from random dopant fluctuation at $\sim$3 sigma level which is believed to arise from the complex, multiple level RTN and the interaction of traps with percolation path. Furthermore, as reported in [15–18], there exist more extreme/occasional transistors with significant impact at smaller/negative gate overdrive. In subthreshold region, in addition to the sparse carriers to screen the influence of charged trap [12], the exposed critical current percolation path that dominants the subthreshold leakage is another important factor for anomalously larger RTN impact. Various 3D atomistic simulations [25–28] considering the presence of a single charged trap together with other variation sources simultaneously are performed for the understanding of underlying mechanisms. It is observed that random dopant fluctuation, in conjunction with specifically located trap could result in rare but dramatic changes in device characteristics and larger RTN impact. In addition, evaluations are conducted extensively for logic circuits with various low operating voltages, transistor sizes, logic stage numbers, logic gate types and substrate

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biases [29,30]. Small number of samples is shown to exhibit larger RTN-induced delay fluctuation (10.4% of nominal oscillation frequency at 0.65 V for ring oscillators fabricated in 40 nm CMOS technology) and the impact can be mitigated by increasing supply voltage, transistor size and logic stage number. Furthermore, the susceptibility of cell robustness to RTN for the minimum-sized SRAM circuits is higher/important than other applications and attracts much attention recently [21,31–39]. Various characterization techniques and monitoring metrics such as accelerated testing [31], alternating-bias measurement [32], dynamic margins [33], and model approximations [35–39] are proposed for the analysis of large-scale SRAM chips. It is revealed that a cell skewed toward less read margin is more vulnerable to RTN [38] which could lead to 50 mV V_{min} degradation [32].

Moreover, in order to extend Moore's law, several emerging device structures or materials to replace the conventional MOSFETs are proposed. Among the possible choices, the FinFET and Gate-All-Around (GAA) transistors offer superior short-channel characteristics and better variability immunity. The use of high-mobility channel materials (such as Germanium (Ge)) is promising to increase current drive and boost circuit performance. For ultra-low-voltage applications, Tunnel FET (TFET) that utilizes interband tunneling as the current conduction mechanism surmounts the theoretical limitation of thermionic subthreshold slope to offer lower leakage current while maintaining satisfactory performance at low-voltage [40,41]. For TFET, several pioneering works macroscopically evaluated the effects of interface traps induced after the consecutive positive-bias and hot-carrier stresses [42–44] as well as investigated the behaviors of low frequency noise [45,46] and ambipolarity [47]. In [63], the sensitivity to single-trap-induced RTN is comprehensively elaborated for TFET under the influence of a discrete acceptor-type or donor-type trap. It is observed that significant RTN impacts in TFET comes from the distortion of band profiles and critical tunneling path that could lead to drastic leakage degradations. The geometry dependence of RTN and its interactions with work-function variation are assessed for the first time. Furthermore, the worst-case predictions resulting from the trapping/detrapping in each transistor are considered to account for all possible RTN patterns for TFET-based SRAM cell and various commonly used sense amplifiers [64].

In this paper, we review the impacts of single-trap-induced RTN on several emerging transistor candidates such as FinFET [48–61], Si and Ge GAA nanowire [62] and TFET [63–65], along with the resulting impacts on SRAM and logic circuits. For the RTN impacts, the static changes in drain currents by an acceptor-type trap (carry a negative charge in trapped state) or donor-type trap (carry a positive charge in detrapped state) for NFET and PFET are considered, respectively. The dynamic current transition determined by the τ_c and τ_e of conducting carriers is not included. This paper is organized as follows. In Section 2, we describe the impacts of RTN on FinFETs with trap at various locations and under different device designs. The resulting influence on FinFET 6T SRAM cells and several logic circuits is examined as well. Section 3 discusses and compares the sensitivity of Ge/Si based NanoWire (NW) transistors, 6T SRAM cells and inverters to RTN. The significant band-to-band tunneling current in Ge-NW FETs lead to different drain bias dependence from the Si counterparts. The analysis of RTN for TFET is illustrated in Section 4. The differences in the RTN immunity as well as the underlying mechanisms that govern the distinct impacts between TFET and FinFET are discussed in this section.

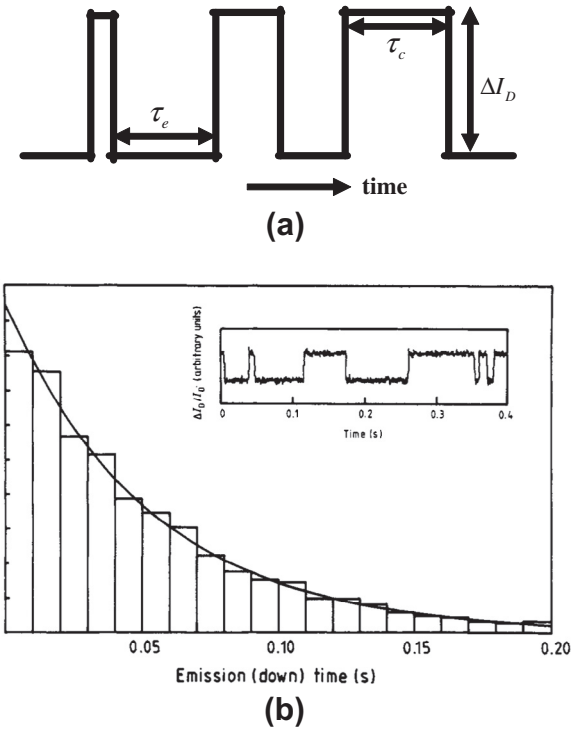


Fig. 1. (a) Schematic of transient waveform showing the two-level I_D fluctuation due to RTN in n-type MOSFET and (b) the distribution of emission times at 95 K and V_{GS} = 1.115 V [5].

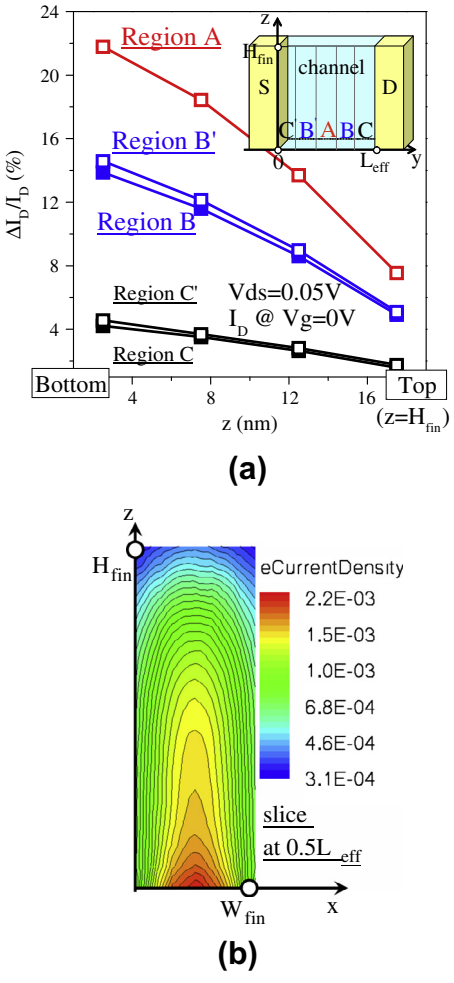


Fig. 2. (a) Dependence of RTN amplitude ($\Delta I_D/I_D$) on trap location across FinFET sidewall interface and (b) the electron current density of a cross section sliced at the middle of source/drain and V_g = 0 V [48–50].

The worst-case analysis of robustness for TFET based 8T SRAM cell and commonly used sense amplifiers are described. Finally, we summarize this review in Section 5.

2. FinFET devices and circuits

Fig. 2 shows the dependence of RTN amplitude ($\Delta I_D/I_D$ where ΔI_D is defined as I_D (detrapped) – I_D (trapped)) on the position of a single charged trap placed across FinFET sidewall interface [48–50]. The sidewall interface is divided into horizontal (from source to drain denoted in sequence as Region C′, Region B′, Region A, Region B and Region C) and vertical (along fin height indicated as z-axis) directions for the location analysis of RTN amplitude. Similar to the planar BULK MOSFET at low V_{ds} [25], significant RTN amplitude is found for the trap located near the middle region between source and drain (Region A), and the RTN amplitude decreases toward the source/drain (Regions C and C′) [48–50,57,58]. The noticeably higher sensitivity to RTN in the middle region results from the direct influence of the charged trap on the critical potential barrier that determines the subthreshold current at low V_{ds}. Across the fin height direction, the trap located near the bottom of sidewall interface (z = 0 nm) is closer to the path with higher subthreshold current (due to the fringing drain field penetration through buried oxide into lightly doped fin channel, as shown in Fig. 2(b)), thus leading to larger impact of RTN. However, for the case with significant quantum confinement and volume inversion in the subthreshold regime [57,58], the carrier distribution is lifted upward, making the spot with larger RTN amplitude higher accordingly (located around half fin height).

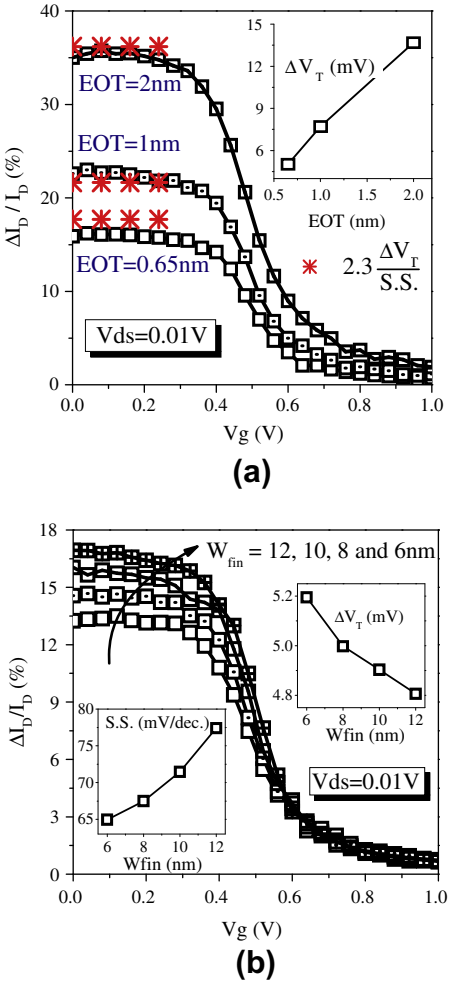


Fig. 3. Dependence of RTN amplitude for FinFET with various (a) EOT and (b) fin width (W_{fin}). The single trap is placed at the center of sidewall interface [48].

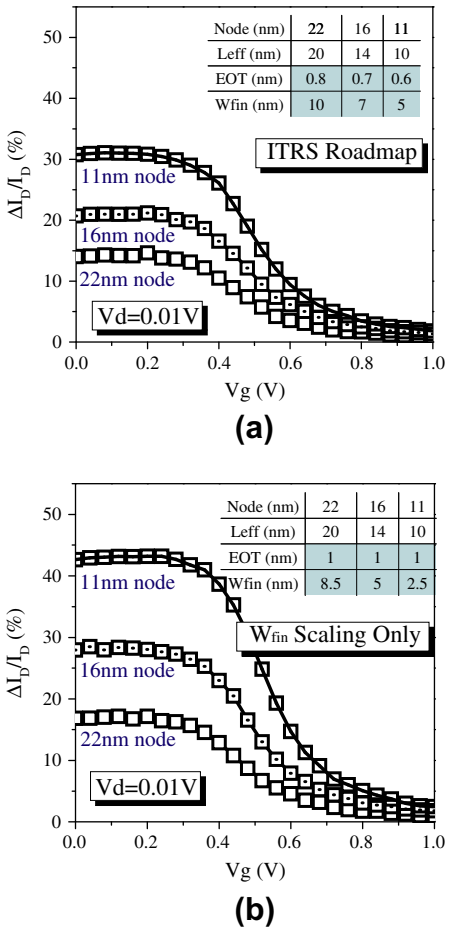


Fig. 4. Comparisons of RTN amplitude for scaled FinFET based on the designs of (a) the ITRS prediction that scales both EOT and W_{fin}, and (b) W_{fin} scaling only. The FinFETs are designed with comparable S.S. (85 mV/decade), and the single acceptor-type trap is placed at the center of sidewall interface [48].

In Figs. 3–5, the geometry dependences and various device designs for scaled SOI FinFET are assessed from the perspective of RTN amplitude [48,59]. The dependence of RTN amplitude for FinFET on equivalent oxide thickness (EOT) and fin width (W_{fin}) across wide range of V_g is shown in Fig. 3. As can be seen, with decreasing conducting carriers [12], RTN amplitude increases with reduced screening effect at lower V_g. In subthreshold region, the RTN amplitude is modeled as [59],

$$\frac{\Delta I_D}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_T}\Delta V_T = 2.3\frac{\Delta V_T}{\text{S.S.}}$$

which is proportional to the trap-induced V_T shift (ΔV_T) and inversely proportional to device subthreshold slope (S.S.). As can be seen in Fig. 3(a), the simplified model shows fairly good agreement with the simulated results and reveals the factors that determine RTN amplitude in the subthreshold region. In Fig. 3(a), it is observed that thinner EOT reduces RTN amplitude owing to better electrostatic integrity which suppresses the trap-induced potential perturbation ((ΔV_T) in the inset of Fig. 3(a)), however, decreases S.S. that possibly increases the value of $\Delta I_D/I_D$. Specifically, the reduction of ΔV_T with smaller EOT (3X improvement in RTN amplitude) overwhelms the decrease in S.S. (cause 1.2X degradation of RTN amplitude), thus resulting in the better RTN immunity with EOT scaling. Fig. 3(b)

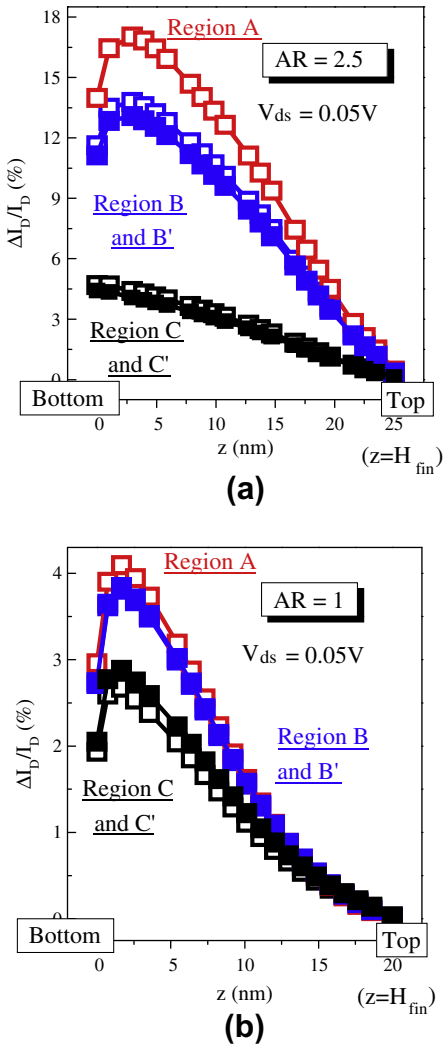


Fig. 5. Impact of aspect ratio (AR = H_{fin}/W_{fin}) on FinFET RTN amplitude: (a) AR = 2.5 and (b) AR = 1 for a single acceptor-type trap located at various positions [59].

shows the dependence of RTN amplitude on different fin width designs (W_{fin} = 6–12 nm). Due to the increases in ΔV_T (resulting from the close proximity between the interface trap and current conducting path) and smaller S.S. (see the inset of Fig. 3(b)), FinFETs with thinner W_{fin} are more susceptible to RTN, implying a possible concern for scaled FinFET using thin W_{fin}.

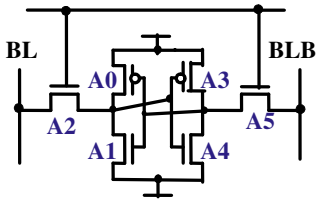
With the observations in Fig. 3, Fig. 4 compares the RTN amplitude of scaled FinFETs for the 22-, 16-, and 11-nm technology nodes based on the following design strategies: (1) the prediction of ITRS with both EOT and W_{fin} scaling (Fig. 4(a)), and (2) considering W_{fin} scaling only (Fig. 4(b)). The tables shown in Fig. 4 illustrate the geometries of various FinFETs with comparable S.S. (85 mV/decade) for fair comparison. As can be seen in Fig. 4(a), the reduction of gate area and closer proximity of the interface trap to the current path lead to higher sensitivity to RTN in scaled FinFET. Compared with the RTN amplitude shown in the 22-nm node, 1.5X and 2.2X larger RTN amplitude are observed for the 16-nm and 11-nm node, respectively. On the other hand, significantly larger degradations in RTN amplitude are found for FinFETs with only W_{fin} scaling (Fig. 4(b)). The RTN amplitude of 16-nm (or 11-nm) node FinFET becomes 1.7X (or 2.5X) inferior to the case in 22-nm node. In other words, scaling EOT and W_{fin} simultaneously is suggested to reduce the impact of RTN while sustain satisfactory electrostatic integrity for scaled FinFET devices.

In addition to the device designs with various EOT and W_{fin}, the selection of aspect ratio (AR = H_{fin}/W_{fin}) for FinFET alters the susceptibility to RTN amplitude. Fig. 5 demonstrates the impact of AR on FinFET RTN amplitude in OFF state (V_g = 0 V) for a single acceptor-type trap placed across the sidewall interface [59]. For fair comparison, various aspect-ratio FinFETs are evaluated under a given total effective width ($2H_{fin} + W_{fin}$). Under this criterion, device with higher AR results in thinner W_{fin} and better gate controllability. Due to its closer distance to interface trap and smaller S.S., considerably larger RTN amplitude occurs for the FinFET with AR = 2.5 than the case with AR = 1. In other words, for a given total effective width, the FinFET designed with lower aspect ratio exhibits better immunity to RTN.

Furthermore, in the presence of other intrinsic variation sources, the single charged trap in lightly-doped FinFET is shown to interact with random dopant fluctuation, line edge roughness or work function variation and extends the RTN distribution tail to increase the RTN amplitude and its variation [57]. However, due to the characteristics of volume inversion that conducts current away from the influence of interface trap [66], FinFET exhibits smaller RTN dispersions than those of planar BULK MOSFET which shows stronger interactions and severer variability from its surface conduction [25,48].

In Figs. 6–12, we review the impacts of RTN on the cell stability/performance of FinFET 6T SRAM cells and leakage/delay of several FinFET logic circuits [48]. For circuit analysis, the single charged acceptor-type and donor-type trap is considered for NFET and PFET devices, respectively in the worst position (middle/bottom region of sidewall interface shown in Fig. 2(a)). Due to the trapping and detrapping of a charge at the interface trap, each transistor contributes two-level current fluctuation and results in 2^n possible combinations for the circuit-level analysis with n transistors in certain circuit.

For 6T SRAM cell shown in Fig. 6, there exists 64 possible combinations which are binary coded with the cell transistor labeled from A0 to A5, and the bit values of "0" and "1" represent the "detrapping" and "trapping" states, respectively [48–50]. Hence,



Cell Type: (**A5***2^5+**A4***2^4+**A3***2^3+**A2***2^2+**A1***2^1+**A0***2^0)

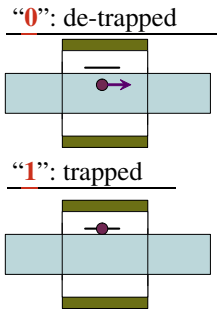


Fig. 6. Possible combinations of two-level RTN in each cell transistor for the worst-case analysis of conventional 6T SRAM cell. The cell type denotes the status (trapping or detrapping) of each device in the cell. The single trap is located at the worst position [48–50]. The A0/A3, A1/A4 and A2/A5 indicate the pull-up, pull-down and pass-gate cell transistors.

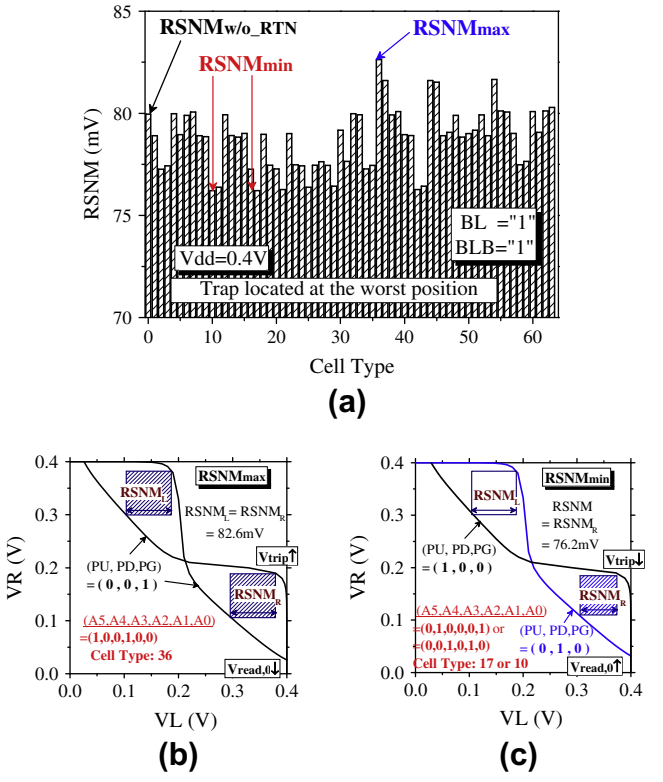


Fig. 7. (a) RSNM variations of 6T FinFET SRAM cell formed by trapping/detrapping in each device (64 combinations) and the READ butterfly curves for the cases with (b) maximum and (c) minimum RSNM at V_{dd} = 0.4 V. The PU, PD and PG shown in Fig. 7(b) and (c) denote pull-up, pull-down and pass-gate transistors, respectively [48–50].

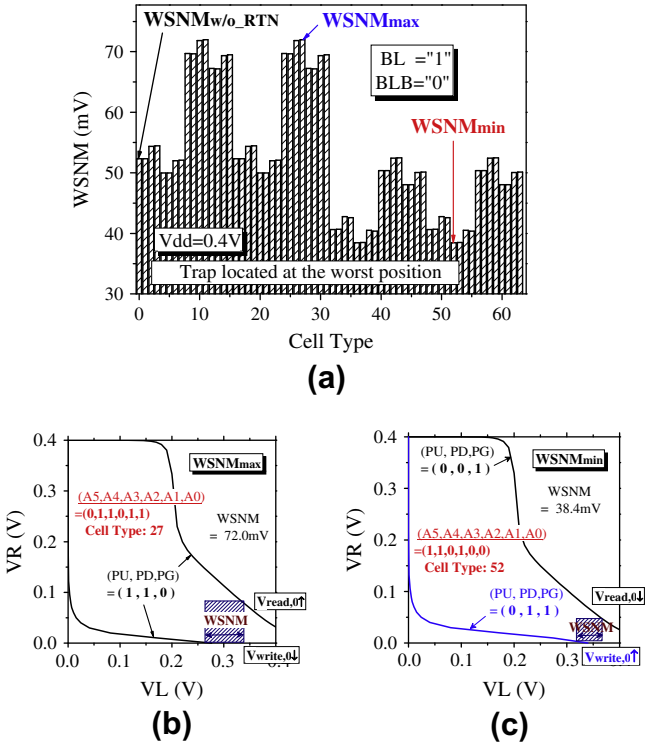


Fig. 8. (a) 64 possible WSNM of 6T FinFET SRAM cell due to trapping/detrapping in each device and the WRITE butterfly curves for the cases with (b) maximum and (c) minimum WSNM [48–50].

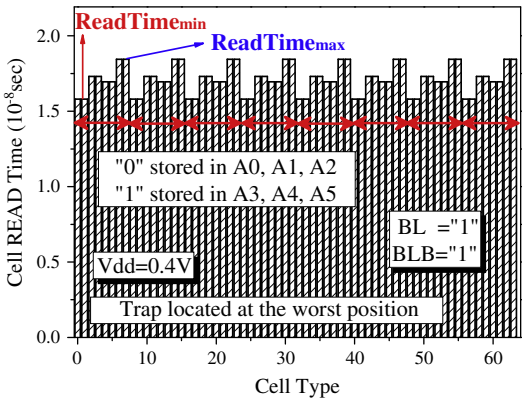


Fig. 9. The cell READ access time variation of 6T FinFET SRAM cell caused by RTN. The READ access time determined by the pull-down and pass-gate transistors is insensitive to the RTN in pull-up devices (A0/A3).

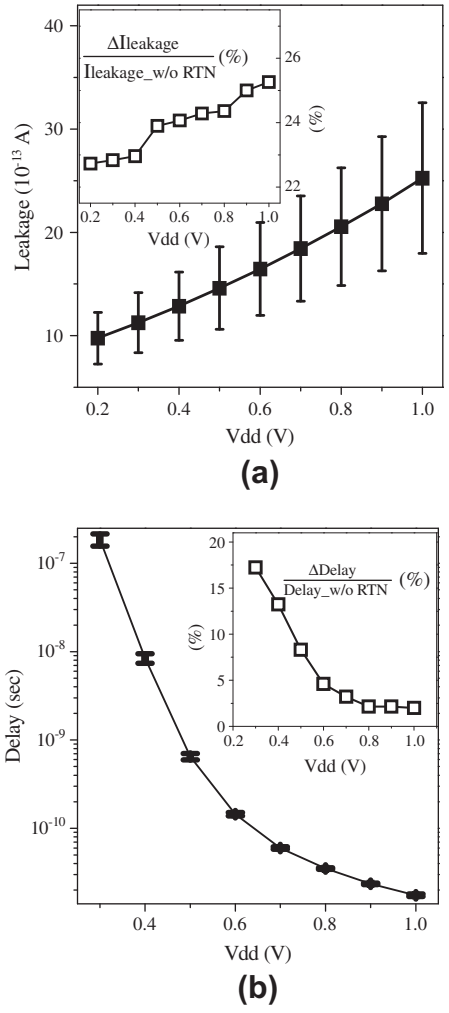


Fig. 10. (a) Leakage and (b) delay of FinFET inverter considering RTN. The error bars represent the variations from the four possible combinations with trapping/detrapping in NFET and PFET. The single trap is placed at the worst position [48,50].

the "0" cell type means that all six transistors are free from RTN, whereas the "63" cell type indicates that there is a charged trap in each and every cell transistor. Fig. 7(a) summarizes the 64 possible values of READ Static Noise Margin (RSNM) for the 6T FinFET

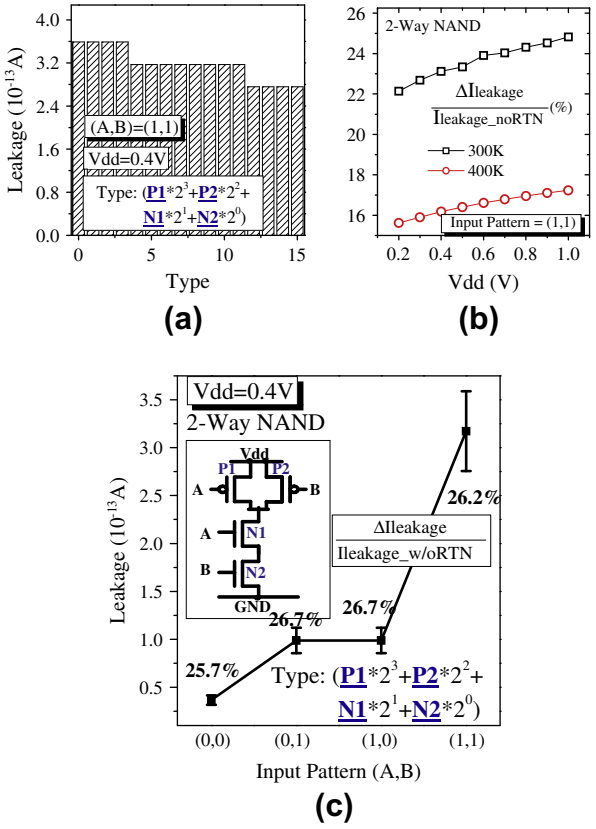


Fig. 11. The leakage variation of FinFET 2-Way NAND (with input pattern (A, B) = (1, 1)): (a) with all possible combinations, and (b) the V_{dd} dependence of leakage at T = 300 K and 400 K. Fig. 11(c) compares the leakage for different input patterns at V_{dd} = 0.4 V. The error bars denote leakage variation among 16 combinations in (a) [48,50].

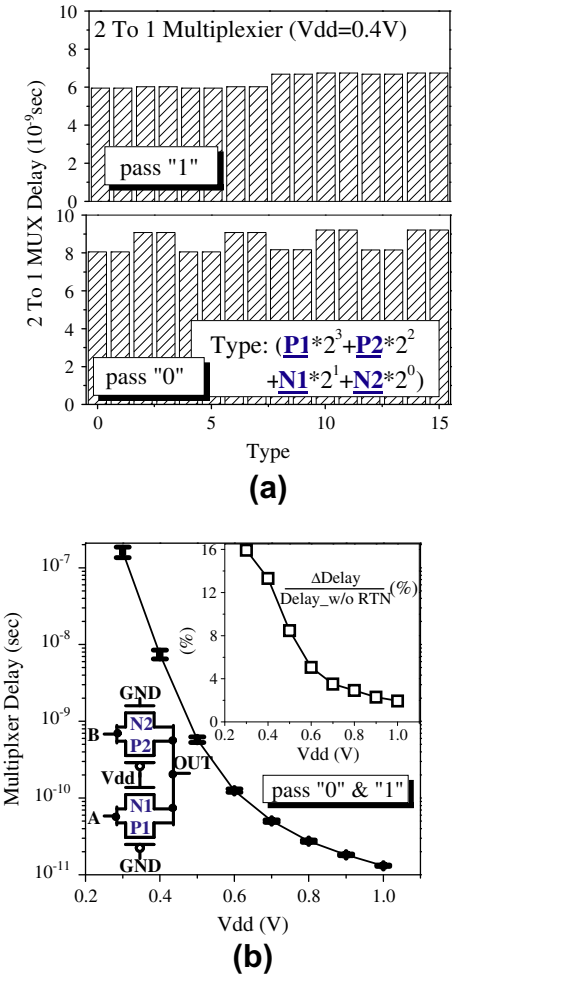


Fig. 12. (a) Delay fluctuation of 2-To-1 FinFET multiplexer due to trapping/detrapping in each device (16 combinations) at V_{dd} = 0.4 V and (b) the dependence of delay on V_{dd} for a single trap in the worst position [48,50].

SRAM cell at V_{dd} = 0.4 V, targeting for the operating regime with higher RTN impact (Fig. 3). The RSNM, as an indicator of cell robustness in READ operation, is calculated by the maximum square that can fit inside the READ butterfly curves [67]. Therefore, larger inverter trip voltage (V_{trip}) and smaller READ disturb ($V_{read,0}$) are beneficial for better stability. Among the possible combinations [48–50], the maximum RSNM occurs in the SRAM cell with symmetrical RTN patterns (cell type = 36). In such cell with (PU, PD, PG) = (0, 0, 1) as shown in Fig. 7(b), the stronger/detrapped pull-up and pull-down cell transistors combined with weaker/trapped pass-gate device increases cell trip voltage and suppresses READ disturb, thus resulting in symmetric/larger margin. Fig. 7(c) shows the case of minimum RSNM composed of the asymmetrical pair (cell type = 10 or 17) with smaller RSNM squeezed by the larger READ disturb and smaller trip voltage from the opposite half cells. In such RTN configurations, the trapping mechanism happens in the pull-up and pull-down cell transistors from the opposite half cells (A5, A4, A3, A2, A1, A0) = (0, 1, 0, 0, 0, 1) or (0, 0, 1, 0, 1, 0).

Fig. 8 shows the WRITE Static Noise Margin (WSNM) variation caused by RTN at V_{dd} = 0.4 V [48–50]. The WSNM, relating to the competition between pass-gate and pull-up cell transistors, increases with stronger pass-gate and weaker pull-up devices. Due to its mitigated $V_{write,0}$ (determined by the voltage divider between pull-up and pass-gate transistors in the side of writing "0") and higher READ disturb, the cell type 27 with symmetrical RTN patterns (all pull-up and pull-down devices in trapped state whereas both pass-gate transistors in detrapped state) spans the margin between WRITE butterfly curves and exhibits the largest WSNM (Fig. 8(b)). On the other hand, the WSNM (cell type = 52) is limited by the asymmetrical RTN patterns with (PU, PD, PG) = (0, 0, 1) and (0, 1, 1) for the side of writing "1" and "0", respectively. In this type, the margin diminishes with larger $V_{write,0}$ and smaller $V_{read,0}$, leading to the WSNM that is ~34 mV smaller than the maximum one. Besides, due to its severer $V_{write,0}$ variations shown in Fig. 8(b) and (c), WSNM is more vulnerable to RTN than the RSNM counterpart.

Fig. 9 shows the cell READ access time fluctuations among 64 possible combinations at V_{dd} = 0.4 V. The cell access time is estimated from the time required to develop 10%V_{dd} bit-line differential voltage and relates to the current through pass-gate and pull-down transistors. As such, the RTN variations in pull-up devices (A0/A3) exhibit marginal impact on cell READ performance while for the cell types with trapping in pass-gate (A2/A5) or pull-down (A1/A4) cell transistors, the READ current reduces and directly increases the cell access time.

Fig. 10 shows the impacts of RTN on the leakage/delay of the FinFET inverter at various V_{dd} [48,50]. The error bars represent leakage/delay variations from the four possible RTN combinations formed by trapping/detrapping in NFET and PFET. As can be seen in the inset of Fig. 10(a), the leakage variation induced by RTN is around 24% at V_{dd} = 0.5 V and gradually increases with V_{dd}. On the other hand, the delay variation induced by RTN decreases with increasing V_{dd} due to the increasing/extra carriers to screen the charged trap (Fig. 10(b)). For FinFET inverter delay, the impact of

RTN significantly increases for V_{dd} smaller than 0.6 V and reaches ~17% at V_{dd} = 0.2 V.

Fig. 11 shows the leakage analysis of 2-Way NAND with 16 possible RTN combinations coming from the trapping/detrapping in each transistor [48,50]. Fig. 11(a) illustrates the corresponding 16 types with input pattern (A, B) = (1, 1) at V_{dd} = 0.4 V. Since the leakage current is dominated by the OFF transistors (e.g. two PFETs for (A, B) = (1, 1)), the impact of RTN on 2-Way NAND leakage can be found for trapping/detrapping happening in P1/P2 devices. Moreover, it can be seen that the PFETs in trapped state degrades the device strength and in turn, reduces the overall leakage. The impact of temperature on 2-Way NAND leakage variation is shown in Fig. 11(b). As can be seen, due to the significant degradation in S.S. [48], rising temperature from 300 K to 400 K mitigates the influence of RTN and suppresses the RTN-induced leakage current variation in 2-Way NAND. Among various input patterns, 2-Way NAND shows comparable leakage variation ~25% which is similar to the influence in FinFET inverter.

Transmission gate based multiplexers (MUX) are important for critical data flow elements such as shifters and for the control portion of microprocessor. Fig. 12(a) shows the impacts of RTN on 2-To-1 MUX delay with 16 possible RTN combinations (defined in the inset of Fig. 12(a)) for passing "1" and passing "0" through input A [48,50]. Due to the difference in gate overdrive (i.e. V_g–V_s where V_T is similar for NFET/PFET and is neglected for simplicity), the critical transistor that determines the overall delay suffers the largest RTN impact and changes depending on the data delivered to the output node. For pass "1", the initial state in output node is GND and the resulting gate overdrives are $V_{dd} - V_{output}$ and V_{inputA} – GND for NFET and PFET, respectively. In such case, P1 transistor (shown in Fig. 12(b)), with higher/fixed gate overdrive, dominates the overall delay and exhibits significant RTN impact during passing "1". On the other hand, N1 device that sustains firm/high gate overdrive ($V_{dd} - V_{inputA}$) determines the overall delay and shows higher susceptibility to RTN for the case of passing "0". The dependence of delay on V_{dd} considering pass "1" and pass "0" along with 16 combinations is shown in Fig. 12(b). As expected, the delay variation increases with decreasing V_{dd} and reaches ~16% at V_{dd} = 0.2 V.

3. Si/GE Nanowire FETs and circuits

Germanium (Ge) MOSFETs with higher mobility are attractive for enabling higher current drivability and regarded as promising candidate to replace conventional silicon (Si) transistors. Gate-All-Around NanoWire (GAA NW) device structure (inset of

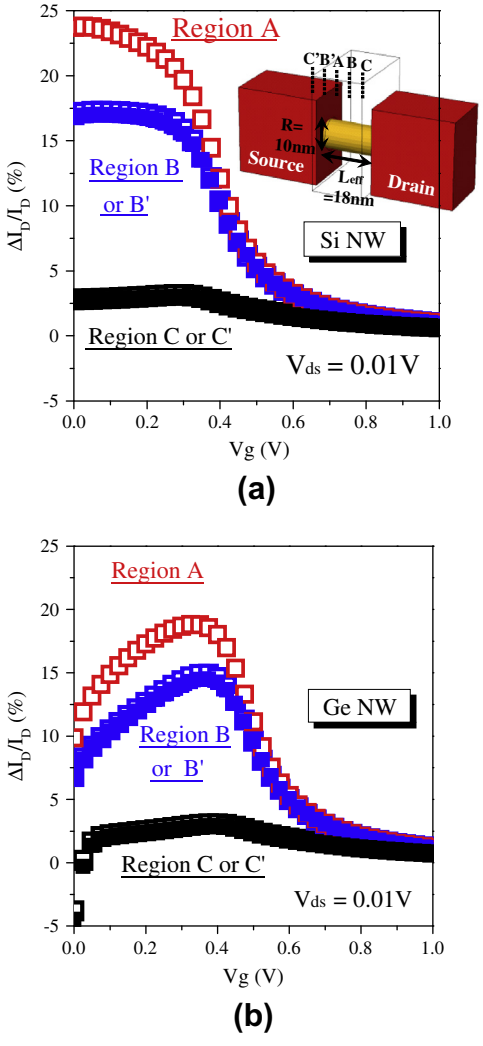


Fig. 13. Dependence of RTN amplitude on trap location for (a) Si-NW and (b) Ge-NW FET at V_{ds} = 0.01 V. The NW transistor is divided into five regions from source to drain to assess the impact of trap location (inset of Fig. 13(a)) [62].

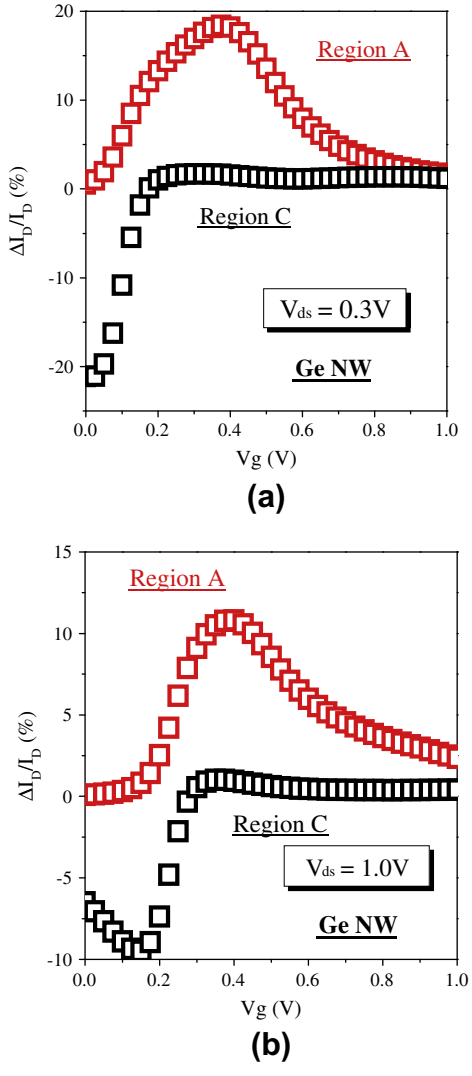


Fig. 14. Comparison of RTN amplitude for Ge-NW FET with trap in Region A and Region C at V_{ds} = (a) 0.3 V and (b) 1.0 V. The negative RTN amplitude indicates the I_D increase in the presence of an acceptor-type trap [62].

Fig. 13(a)), with superior gate control, is suitable for the use of Ge transistors that intrinsically possess higher permittivity and severer short channel effects. In addition to the subthreshold leakage, the contribution of band-to-band tunneling current is important for Ge with smaller band gap. Whether the influence of RTN on Ge-NW MOSFETs and related circuits differs from the Si counterparts is reviewed in this section.

Because of its cylindrically symmetrical structure, the single acceptor-type is placed laterally from source to drain to assess the dependence of RTN amplitude on trap location for NW FETs [62]. Fig. 13 compares the RTN amplitude for Si-NW and Ge-NW at V_{ds} = 0.01 V. As can be seen, significant RTN amplitude is observed for both Si-NW and Ge-NW FETs with single charged trap near the middle region between source/drain (Region A) and gradually decreases toward the source and drain regions (Region C' and Region C) which is similar to the case of planar BULK MOSFETs [25] and FinFETs [48–50,57,58]. However, with increasing V_{ds}, distinct characteristics of RTN amplitude are observed for Ge-NW devices [62]. It can be seen in Fig. 14 that for trap placed in Region A, the influence of charged trap is screened through the noticeable band-to-band tunneling current, thus suppressing RTN amplitude at V_{ds} = 0.3 V and 1.0 V (especially for the cases around V_g = 0 V). On the other hand, Ge-NW FET exhibits negative RTN amplitude at low V_g with single trap placed near drain side (Region C), which means the current actually increases under the influence of an acceptor-type interface trap. The enhanced current results from the extra band-to-band current generated in the vicinity of drain side where exhibits perturbed band structure and higher electric field in the presence of the charged trap [62].

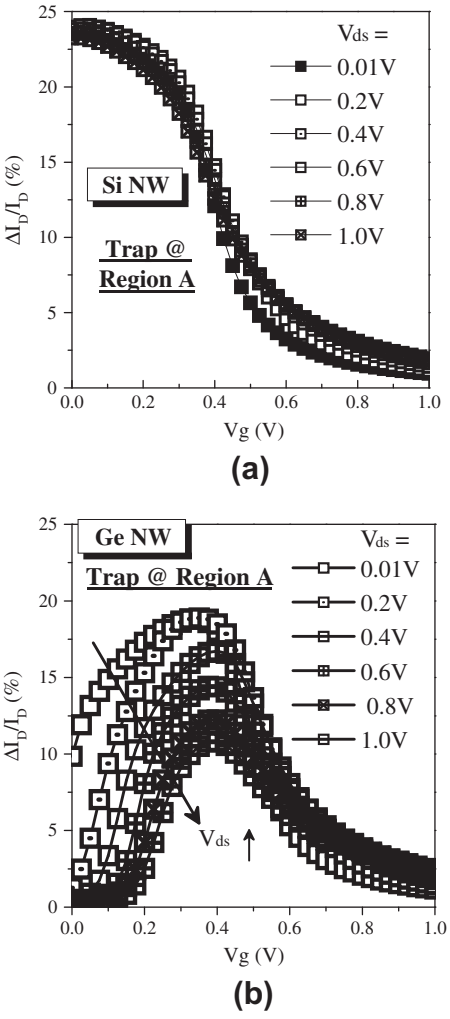


Fig. 15. Impact of V_{ds} on RTN amplitude for (a) Si-NW and (b) Ge-NW FET with single acceptor trap located in Region A [62].

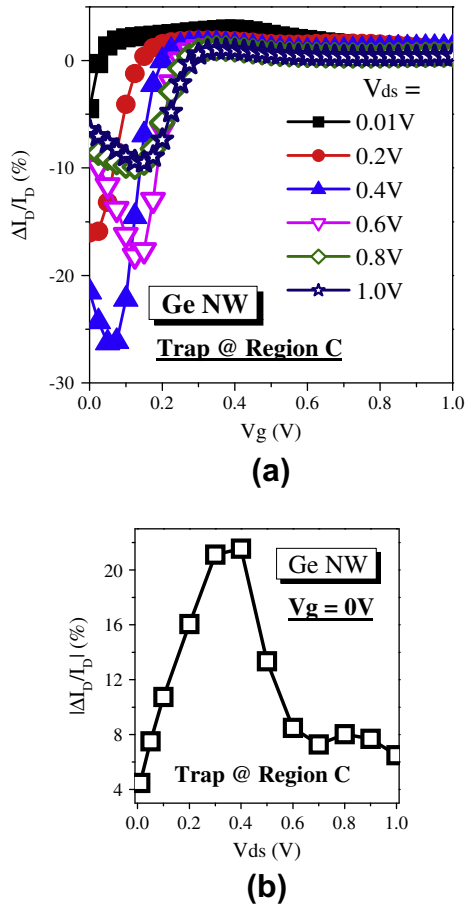


Fig. 16. (a) RTN amplitude of Ge-NW FET at various V_{ds} with single acceptor trap in Region C, and (b) the V_{ds} dependence of absolute values of OFF-state RTN amplitude for the conditions in (a) [62].

With band-to-band tunneling current, the RTN amplitude of Ge-NW FET shows higher dependence on V_{ds} that directly alters the lateral electric field and significantly impacts device characteristics around the OFF state [62]. Fig. 15 compares the RTN amplitude for Ge-NW and Si-NW FETs with single trap located near the middle of source/drain (Region A) at various drain biases. Compared with Si-NW FET, the RTN amplitude in Ge-NW FET shows stronger dependence on V_{ds}, particularly for the cases at lower V_g where tunneling leakage dominates the overall current. The increasing tunneling current at higher V_{ds} provides more carriers to screen the charged trap and reduces RTN amplitude. On the other hand, the RTN amplitude of Si-NW FET is nearly insensitive to V_{ds}. Fig. 16 shows the V_{ds} dependence of RTN amplitude for Ge-NW FET with trap placed around drain side (Region C). It is found that obvious/larger negative RTN amplitude (current increase) happens for trap in the proximity of drain side. Specifically, the maximum OFF-state RTN amplitude occurs at V_{ds} = 0.4 V where the charged trap demonstrates the highest distortion on the band structure (electric field) and induces considerable current increase [62].

Due to its distinct dependence on trap location and V_{ds}, we address the impacts of RTN on Ge-NW FET based 6T SRAM cell and inverter with trap located in Region A or Region C at V_{ds} = 0.3 V and 1.0 V [62]. Figs. 17 and 18 demonstrate the 64 possible RSNM formed by trapping/detrapping in each cell transistor (with cell

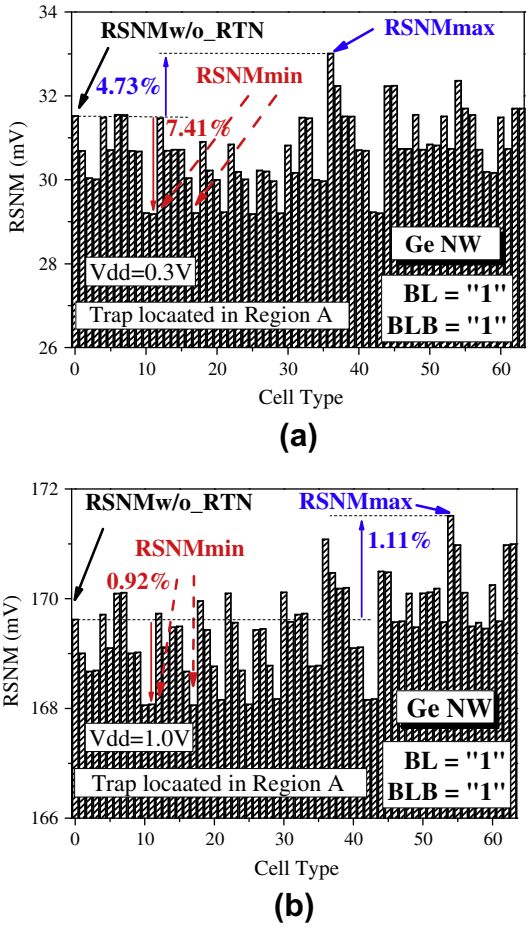


Fig. 17. The 64 possible RSNM for 6T Ge-NW SRAM cell at V_{dd} = (a) 0.3 V and (b) 1.0 V with single trap placed at Region A. The cell type is defined in Fig. 6 [62].

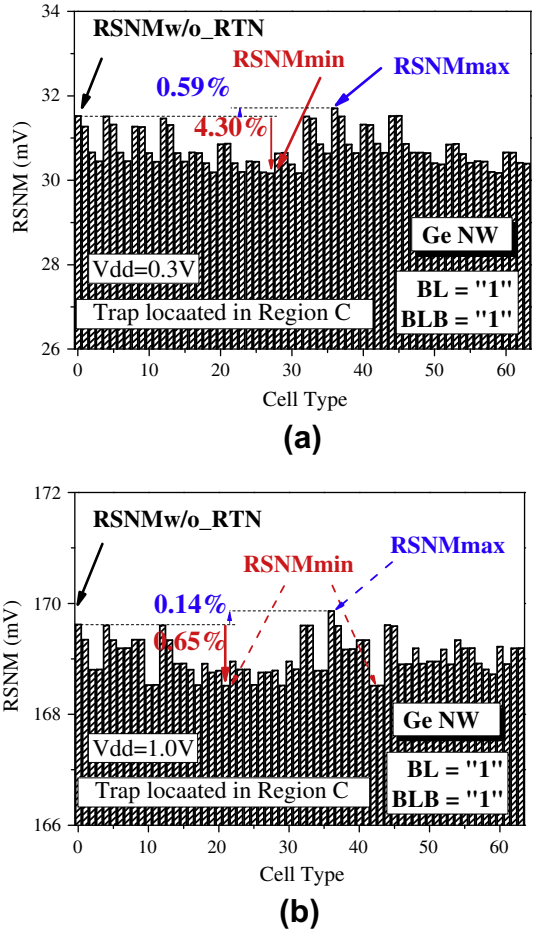


Fig. 18. The 64 possible RSNM for Ge-NW 6T SRAM cell at V_{dd} = (a) 0.3 V and (b) 1.0 V with single trap located in Region C [62].

type defined in Fig. 6). For trap located in the middle between source/drain (Fig. 17), the maximum and minimum RSNM of Ge-NW FET based 6T SRAM cell occur at cell type = 36 and 10 (or 17) at V_{dd} = 0.3 V, which are identical to the FinFET counterpart at V_{dd} = 0.4 V (see Fig. 7). However, at V_{dd} = 1.0 V, the pull-down and pass-gate transistors are in strong inversion regime and exhibit negligible RTN impact (with ~0% RTN amplitude in Fig. 15(b)). Thus, the impact of RTN on RSNM is dominated by the fluctuation of inverter trip voltage and the maximum RSNM happens in the RTN patterns (cell type = 54) with stronger/detrapped pull-up and weaker/trapped pull-down cell devices (cell with (PU, PD, PG) = (0, 1, 1)). Fig. 18 illustrates the 64 possible RSNM configurations for the trap placed around Region C at V_{dd} = 0.3 V and 1.0 V. Compared with the results shown in Fig. 17, it is observed that Ge-NW 6T SRAM cell with single charged trap in Region C shows smaller RSNM variation than that in Region A. The higher susceptibility of RSNM for the cell with trap in Region A can be explained in Fig. 14 which reveals larger RTN amplitude across the range of cell operation (~0.4 V) whereas there exhibits negligible impact for trap located in Region C. Specifically, at V_{dd} = 0.3 V, RTN causes 5% and 12% RSNM variations for trap located in Region C and Region A.

Fig. 19 demonstrates the leakage analysis of Ge-NW and Si-NW FETs based inverters across various V_{dd} under the influence of RTN [62]. It can be seen that for trap placed in Region A, the variation of leakage in Si-NW inverter is insensitive to the change in V_{dd} while the Ge-NW inverter shows increasing impact at lower V_{dd} (V_{dd} < 0.4 V). For trap located in Region C, significant V_{dd}

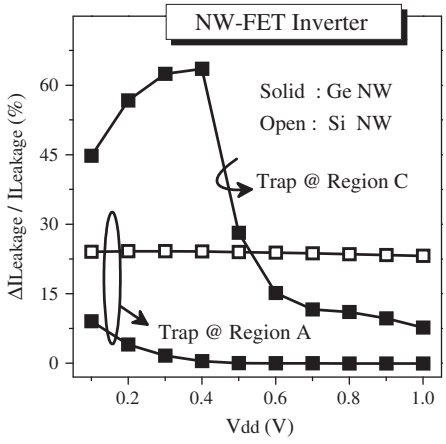


Fig. 19. Impact of RTN on the leakage of Si-NW and Ge-NW FET-based inverters with a single trap placed in Region A or Region C across various V_{dd} [62].

dependence of leakage fluctuation is observed in the Ge-NW inverter which shows the similar trend as found in Fig. 16(b). The impact of RTN on the leakage of Ge-NW inverter can reach 60% for trap located in Region C at V_{dd} ~ 0.4 V.

4. Tunnel FETs and circuits

With the scaling of device dimension and increase in chip density, the deteriorated power consumption becomes a crucial

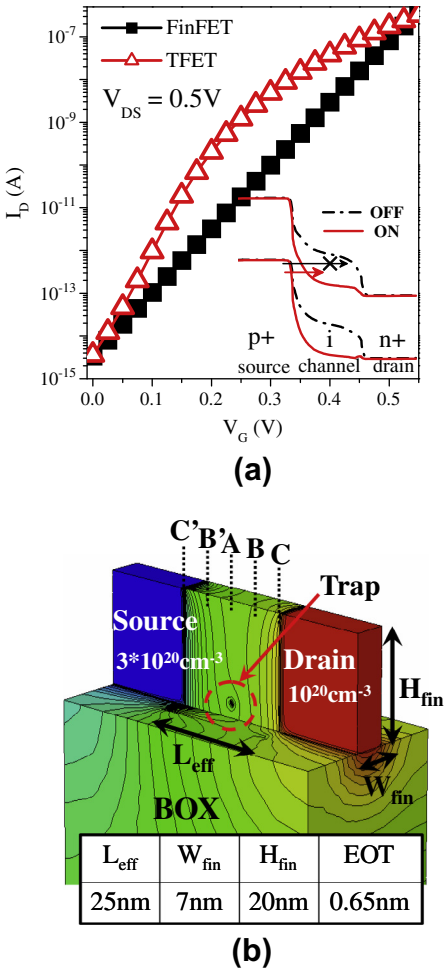


Fig. 20. (a) The I_D–V_G characteristics of TFET and FinFET under equal I_{OFF} and the associated band diagrams of TFET in ON/OFF states. The schematic of TFET with perturbed potential contour by a single charged trap is shown in (b) [63,64].

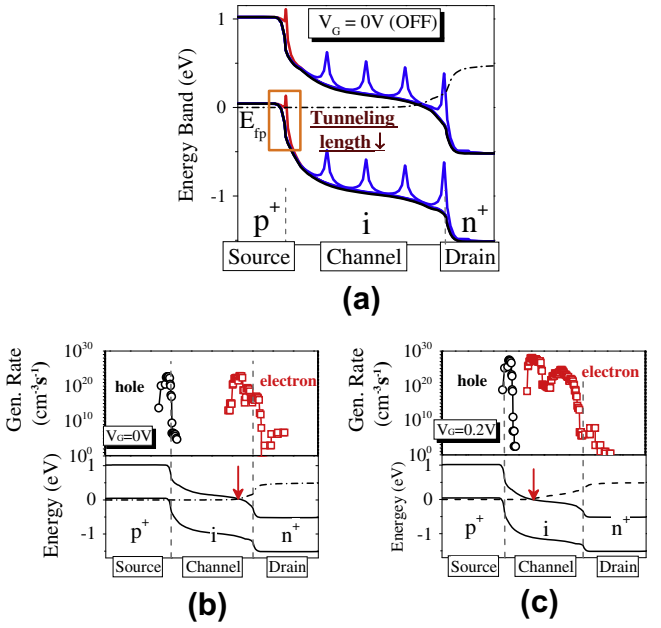


Fig. 22. TFET energy band diagrams along the channel length direction with (a) a single acceptor trap placed at various locations and the electron/hole band-to-band generation rate at (b) V_G = 0 V and (c) V_G = 0.2 V without RTN [63,64].

obstacle for state-of-the-art SoC chips and several strategies from the perspective of technology and system architecture are proposed to relieve power crisis. Voltage scaling is an effective approach to reduce the static and dynamic power consumptions. Because of its higher driving current, the use of high-mobility hetero-channel MOSFETs facilitates low-V_{dd} operation while maintaining satisfactory performance. Besides, various post-CMOS alternatives that offer excellent switching characteristics with steeper subthreshold slope are evaluated recently. Tunnel FET (TFET), which utilizes band-to-band tunneling as the major conduction mechanism (inset of Fig. 20(a)), has attracted much attention because of its capability to surmount the thermionic limitation and provide sub-60 mV/decade S.S. at room temperature [40,41]. Fig. 20(b) shows the schematic of a reversely-biased p-i-n TFET with asymmetrical and distinct source/drain dopant species and concentrations. From the band profiles showing the OFF and ON states of TFET (inset of Fig. 20(a)), the applied positive gate voltage brings down the conduction band in the channel region (intrinsically doped) below the valance band in the source side (p-type doped) and enables sufficient states for electron tunneling from the source, leading to steep/abrupt transition as shown in Fig. 20(a). As reported in [63,64], similar to the approach in FinFET, the single charged trap is strategically placed across the sidewall interface to examine the location dependence of TFET RTN.

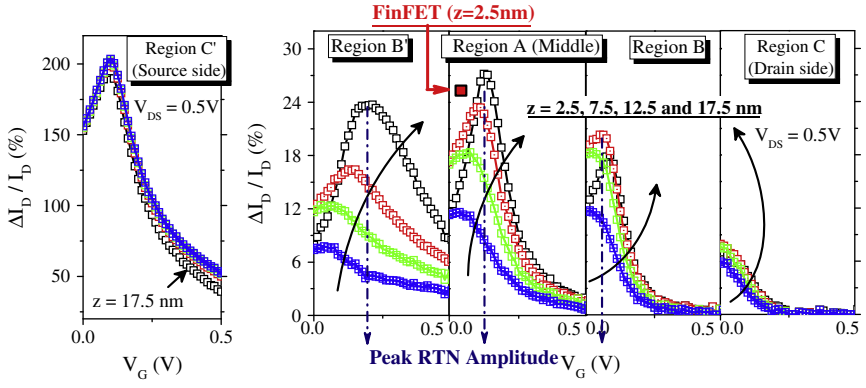


Fig. 21. Dependence of RTN amplitude on the location of a single acceptor trap across sidewall interface. The red square indicates the position of a charged trap (Region A) with the largest RTN impact for FinFET device [63,64]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

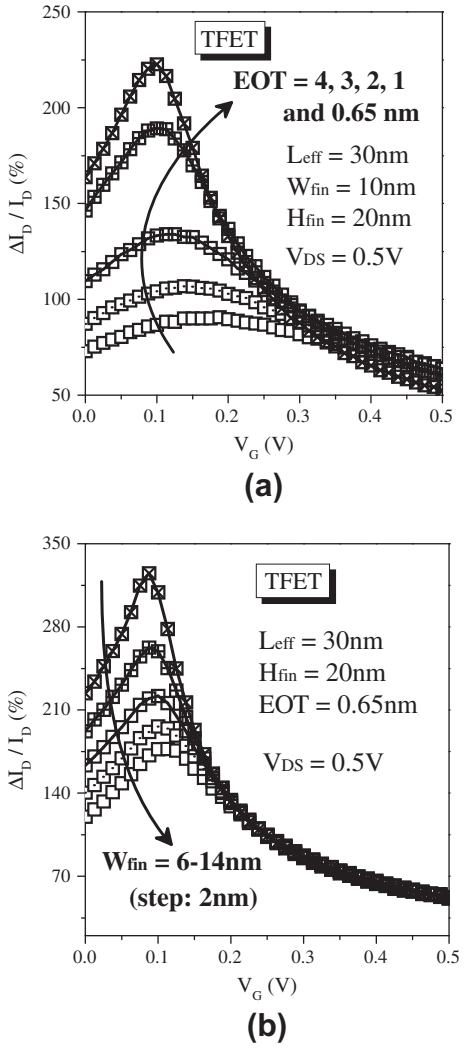


Fig. 23. Comparisons of RTN amplitude for TFET with various (a) EOT and (b) W_{fin}. The single acceptor trap is placed around the tunneling junction [63,64].

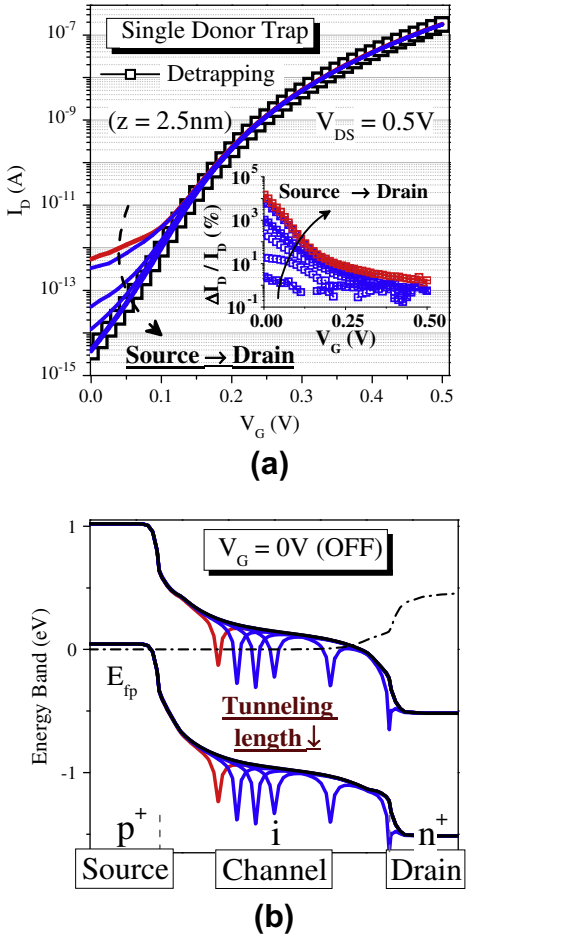


Fig. 24. Impact of a single donor-type trap placed across TFET sidewall interface along the channel length direction, and (b) the corresponding OFF-state energy band diagrams. The significant reduction in tunneling length leads to profound impact on the RTN amplitude [63].

Fig. 21 shows the position dependence of RTN amplitude for TFET across various V_G. Because of the exponential dependence of the tunneling current on critical tunneling path (near source-channel junction) [41], significant RTN impact is found for trap located in the vicinity of tunneling junction (Region C' defined in Fig. 20(b)) and the influence decreases toward the drain side [63,64]. Fig. 22(a) illustrates the corresponding energy band diagrams of TFET along the channel length direction with an acceptor-type trap at various positions. It is observed that for a negatively-charged trap near the tunneling junction, the band peaks up in the proximity of trap location, thus shortening the tunneling length and yielding larger RTN impact. For trap away from the tunneling junction, the critical tunneling length is unchanged (Fig. 22(a)) and exhibits considerably lower impact (Fig. 21). In such case, the RTN amplitude depends on the distance between the charged trap and the spot with significant electron (or hole) generation rate which is similar to the case in conventional planar MOSFET [25–28] and FinFET [48–50,57,58]. As a result, the shift of the position with noticeable electron band-to-band generation rate toward the tunneling junction at higher V_G (Fig. 22(b) and (c)) results in larger RTN amplitude closer to the tunneling junction at larger V_G. This reflects the phenomenon that the peak of RTN amplitude in different regions (indicated by the dashed arrow shown in Fig. 21) occurs at smaller V_G for trap located away from the tunneling junction. With increasing V_G, the regions with trap close to the tunneling junction show higher impact. Compared with the FinFET with largest RTN amplitude (see the red square in Fig. 21), TFET, with its stronger current dependence on the critical tunneling length, exhibits significantly higher susceptibility to RTN for a single acceptor-type trap around the tunneling junction.

In Fig. 23, the device geometry dependence of TFET is addressed with various EOT and W_{fin} for a single acceptor-type trap placed around the tunneling junction. A simple model derived to qualitatively describe the behavior of TFET RTN amplitude is shown below [63,64]:

$$\frac{\Delta I_D}{I_D} \propto \frac{\Delta V_G}{\text{S.S.}}$$

that is proportional to the trap-induced V_G shift (ΔV_G) and inversely proportional to the S.S. It can be seen in Fig. 23(a) that TFET with thinner EOT suffers severer RTN amplitude because of the significant improvement in S.S. which increases the sensitivity to the charged trap. On the other hand, scaling W_{fin} increases ΔV_G (due to closer proximity) and improves S.S. (S.S. reduction) all of which make TFET more vulnerable to the existence of an interface trap. Fig. 24 shows the I_D–V_G characteristics of TFET with a single donor-type trap (carry a positive charge in detrapped state) placed across the sidewall interface along the channel length direction [63]. As can be seen, drastic degradations in I_{OFF} and significantly

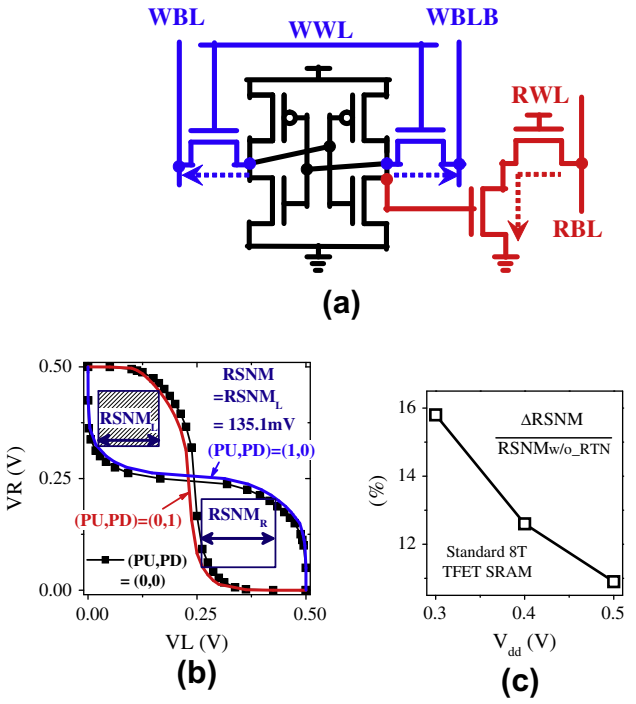


Fig. 25. (a) Schematic of standard 8T TFET SRAM cell, (b) READ butterfly curves showing the combination for maximum and minimum RSNM, and (b) the impact of RTN on RSNM at various V_{dd}. In the analysis, a single trap is placed near the tunneling junction for n-type and p-type TFET. The arrows shown in (a) represent the direction of current flow for uni-directional conducting TFET during READ (red) and WRITE (blue) operations [64]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

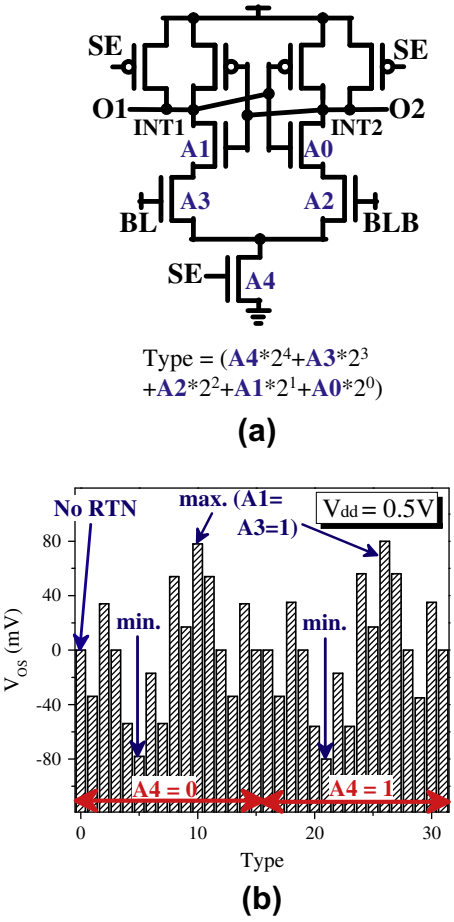


Fig. 26. (a) Definition of trapping/detrapping combinations for the RTN analysis in TFET CLSA, and (b) the 32 values of V_{OS} at V_{dd} = 0.5 V with single trap in the worst position (near tunneling junction) [64].

larger RTN amplitude (inset of Fig. 24(a)) are found. Compared with the acceptor-type trap which exhibits the highest impact around the tunneling junction, a donor-type trap gives rise to considerably larger RTN impact over broad range across the channel region. The associated energy band diagrams shown in Fig. 24(b) indicate that the noticeable decrease in critical tunneling length for the cases with a positively-charged trap inside the channel region is the cause of higher sensitivity of TFET to the donor-type trap.

In the following, the impact of RTN on TFET-based 8T SRAM cell and several sense amplifiers are described with a charged trap placed at the tunneling junction. Due to the limitation of uni-directional conduction for pass-gate TFETs [68], the functionality of conventional 6T SRAM cell is hindered and the standard 8T SRAM cell [69] (Fig. 25(a)) that decouples the READ and WRITE paths are employed for TFET applications. In such cell, RSNM is decided by the noise margin of the internal cross-coupled inverter and less depends on the OFF pass-gate transistors. Fig. 25(b) and (c) demonstrate the RSNM variations due to RTN occurring in the cell transistors of cross-coupled inverter latch [64]. As can be seen, the maximum RSNM happens in the symmetrical RTN patterns with pull-up and pull-down cell transistors in detrapped state, while the minimum RSNM is composed of the asymmetrical pairs with (PU, PD) = (0, 1) and (1, 0). With decreasing V_{dd}, the relative importance of RSNM increases and can reach 16% at V_{dd} = 0.3 V (Fig. 25(c)).

For the analysis of TFET-based sense amplifiers, two commonly used differential small-signal sense amplifiers are discussed: (1) Current Latch Sense Amplifier [70] (CLSA, in Fig. 26) and (2) Voltage Latch Sense Amplifier [71] (VLSA, in Fig. 27). For the activation of CLSA and VLSA, the Sense Enable (SE) signal goes to high to sense the bit-line differential (BL/BLB) voltage through current and voltage modulation, respectively. The voltage difference in bit-lines is amplified through the current/voltage mismatch of two branches inside CLSA and VLSA. With variations, the offset voltage (V_{OS}) is used as the indicator to quantify the robustness of differential sense amplifiers [71–73]. In the presence of RTN, the primarily symmetrical/balanced strength of two branches that connect to the BL and BLB nodes is altered and the required voltage to compensate the strength imbalance is measured as V_{OS} which should be smaller than the minimum bit-line differential voltage to ensure correct sensing operation [72,73].

To assess RTN, the binary-coded definitions of possible trapping/detrapping combinations from the most critical devices of the sense amplifiers are labeled in Figs. 26(a) and 27(a) [64]. Among the 32 V_{OS} combinations coming from the five selected transistors that are vulnerable to RTN (Fig. 26(b)), the trapping/detrapping in the devices connected to BL/BLB (A2 and A3) exhibit the highest impact on the robustness of CLSA. The maximum value of V_{OS} occurs in the RTN configuration with A1 and A3 devices in trapped state ($V_{OS} \sim 80$ mV at V_{dd} = 0.5 V). For VLSA, the RTN in pull-up (A0/A1) and A4 transistors are shown to have negligible impact on V_{OS}. It can be seen in Fig. 27(b) that the existence of trapping/detrapping in pull-down devices (A2 or A3) contributes to the maximum V_{OS} fluctuation (30 mV at V_{dd} = 0.5 V). Due to its steeper S.S. and significant modulations in drain current, TFET-based CLSA requires larger V_{OS} to compensate the impact of RTN and becomes inferior to VLSA.

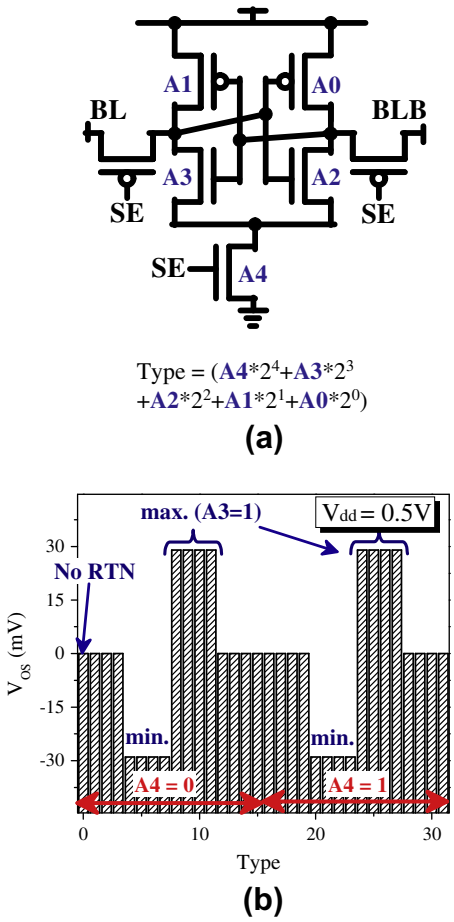


Fig. 27. (a) Definition of possible RTN combinations for TFET VLSA, and (b) the 32 combinations of V_{OS} at V_{dd} = 0.5 V with single trap around the tunneling junction [64].

5. Conclusion

This paper reviews the impact of single-trap-induced random telegraph noise on several promising devices: FinFET, Si/Ge Nanowire FETs, TFET and related circuits. In this work, the static change in drain current is the main concern and evaluated as the worst-case condition for circuit analysis.

For FinFET, the influence of RTN depends on the relative distance between the charged trap and dominant current path. As such, trap located in the middle region between source/drain and around the bottom of sidewall interface exhibits the highest impact. For Ge Nanowire FET, the position with significant RTN impact could be in the middle region between the source/drain or near the drain, depending on the drain bias and gate bias that modulate the contribution of band-to-band tunneling current. Besides, Ge-NW FET may yield current increase with an acceptor-type trap due to the distortion of band profile and enhanced electric field for trap located near the drain. For TFET, the shortening of critical tunneling length results in drastically larger RTN amplitude for trap placed around the tunneling junction and channel region. The design parameters (thinner EOT and W_{fin}) used to improve TFET subthreshold characteristics are found to increase the susceptibility to RTN. Compared with FinFET, TFET exhibits drastic I_{OFF} degradation and higher sensitivity to RTN, particularly in the presence of a donor-type trap inside the channel region. Among various materials, comparable worst-case RTN amplitude is observed for the Ge-NW and Si-NW FETs that both conduct current through the thermionic emission.

For 6T/8T SRAM cells, the possible RTN combinations, resulting from the trapping/detrapping of each cell transistor are examined for cell robustness and performance. Specifically, the limiting RTN patterns with trap placed at the worst position and the resulting impacts are demonstrated at various supply voltages. For the analysis of logic circuits, RTN causes ~24–27% and ~13–15% variations in leakage and delay at V_{dd} = 0.4 V, respectively for FinFET inverters, 2-Way NAND and 2-To-1 MUX. For Ge-NW FET based inverter, significantly larger leakage variation is observed for trap located near the drain side around V_{dd} = 0.4 V. Compared with the TFET-based VLSA, the robustness of CLSA is inferior and higher bit-line differential voltage is required to compensate larger V_{OS}.

Acknowledgements

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