A 1 Tbit/s Bandwidth 1024 b PLL/DLL-Less eDRAM PHY Using 0.3 V 0.105 mW/Gbps Low-Swing IO for CoWoS Application

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***Abstract*—A 1 Tbit/s bandwidth PHY is demonstrated through CoWoS™ platform. Two chips: SOC and embedded DRAM (eDRAM), have been fabricated in TSMC 40 nm CMOS technology and stacked on a silicon interposer chip. 1024 DQ buses operating at 1.1 Gbit/s with VDDQ = 0.3 V are proven between SOC chip and eDRAM chip in experimental results with 1 mm signal trace length on the silicon interposer. A novel timing compensation mechanism is presented to achieve a low-power and small area eDRAM PHY that excludes PLL/DLL but retains good timing margin. Another data sampling alignment training approach is employed to enhance timing robustness. A compact low-swing IO also achieves power efficiency of 0.105 mW/Gbps.**

***Index Terms*—Chip on wafer on substrate, CoWoS, DLL, eDRAM, low-swing IO, micro-bump, PHY, PLL, SII, silicon-interposer, timing compensation, 2.5D-IC.**

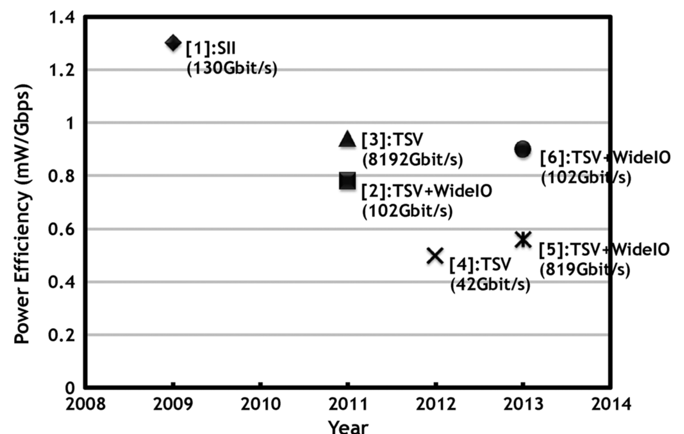

Fig. 1. Power efficiency trends of 2.5D/3D IC applications.

I. Introduction

In RECENT years, 2.5D/3D stacking processes are increasing in popularity. Relaxation of inter-connection loading is one motivator for this trend. High-speed, low-cost transceivers, and even wide data buses, are also beneficiaries. However, chip-to-chip variation and up-to-thousand-bit timing skew are critical problems for heterogeneous stacking. Therefore, we present two novel timing compensation mechanisms in this work.

Recent published works related to 2.5D/3D stacking processes are shown in Fig. 1 [1]–[6]. Power efficiency is increasing even with higher data bandwidth. 3D integrated circuits (3D-ICs) exhibit better speed performance and higher power efficiency compared with 2.5D integrated circuits (2.5D-ICs) due to lower capacitance load in through-signal-vias (TSVs) than in silicon-interposer (SII) traces. However, assembly cost overhead is significantly higher for 3D-ICs versus 2D-ICs. For this reason, we demonstrate a CoWoS platform with eDRAM ASIC that achieves high bandwidth and good power efficiency. We adopt specific techniques to achieve a low power, small area, and low latency eDRAM PHY in this work [8].

A. CoWoS Introduction

CoWoS is short for "Chip-On-Wafer-On-Substrate." The CoWoS platform allows for multiple-chip stacking on a single substrate while sharing one package. It also benefits bus density, reducing size and power, and increasing bandwidth and operation speed. Fig. 2 shows an illustration of CoWoS taking this work as an example. Two chips: an SOC and a memory chip are stacked on a silicon-interposer (SII) chip by front-side face-to-face micro-bump (ubump) bonding. High speed signals are transmitted between the SOC and memory chips through the silicon-interposer. Power, ground, and non-critical signals are accessed through backside C4 bumps of the silicon-interposer chip. TSVs are used to connect front-side ubumps to backside C4 bumps.

This paper focuses on an eDRAM PHY using CoWoS platform implementation, and is organized as follows. Section II

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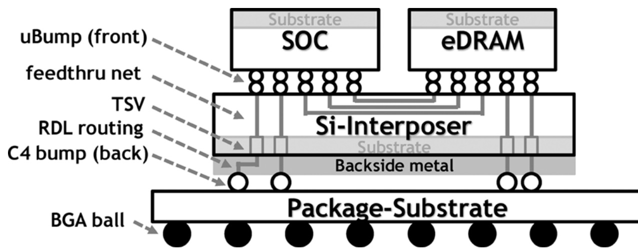


Fig. 2. Illustration of CoWoS.

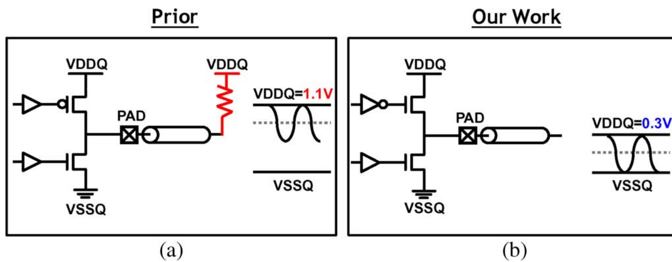


Fig. 3. Reduce IO transmitter power. (a) Prior design. (b) Low-swing IO with low VDDQ and excluding termination.

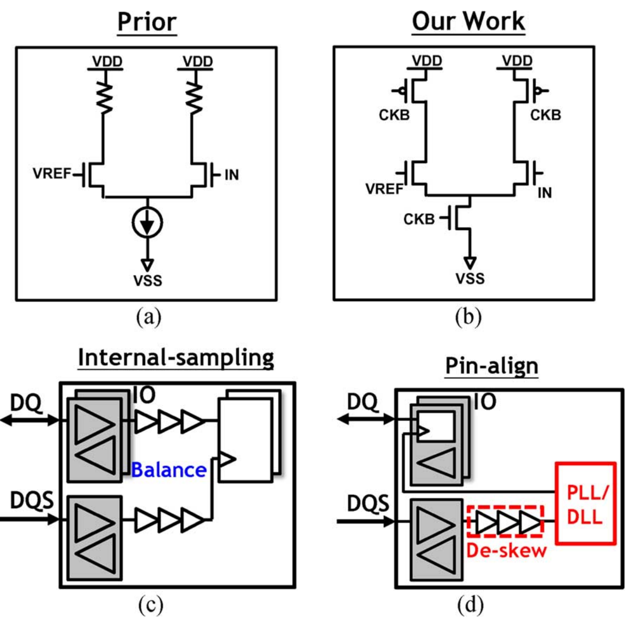


Fig. 4. Reduce IO receiver power. (a) Constant current differential amplifier. (b) Clock-based sense amplifier. (c) Internal-sampling topology. (d) Pin-align topology.

introduces the key low power design concepts. General design considerations are described in Section III. Section IV describes the system architecture. Circuit descriptions are presented in Section V. Section VI shows experimental results. Finally, conclusions are given in Section VII.

II. Low Power Design Concepts

The 2.5D-ICs may represent a compromise as an assembly solution, but low power is still a major target of this work. At least three approaches are identified below to achieve low power performance.

A. Reduce IO Transmitter Power

For wide bus applications, IO typically dominates (20–30%) power consumption of the PHY. As shown in Fig. 3(a), in order to achieve high operation speed, previous designs drive a low swing signal with nominal VDDQ by connecting an output PAD to VDDQ through a 50-Ohm pull-up termination [9]. The signal swing is driven from nominal VDDQ (e.g., 1.1 V) to "VDDQ-0.3 V." Termination guarantees good signal integrity by avoiding signal reflection. However, this topology not only consumes DC power, but also consumes DC power from nominal VDDQ through termination. In this work, the channel is replaced from the traditional PCB trace to a SII trace. Because SII has higher bump pad density compared to PCB, for this kind of wide bus application, the SII trace is much shorter (1000 μm–3000 μm back-end metal) compared to the PCB trace. The transmission line effect is minor for Gbit/s rate operation. In order to achieve low power design, we propose low swing signaling by reducing supply VDDQ and excluding DC termination [Fig. 3(b)]. Therefore the transmitter only consumes dynamic power and power from low VDDQ. The output drives rail-to-rail signal from low VDDQ to VSSQ. And we set our target VDDQ to 0.3 V in this work.

B. Reduce IO Receiver Power

As shown in Fig. 4(a), previous designs use a constant-current differential amplifier in the IO receiver for data amplification. Since the channel is replaced by the SII trace, the signal loss is minor. A low-cost receiver without DC current consumption is proposed [Fig. 4(b)].

Based on an "internal sampling topology" [Fig. 4(c)], each DQ has to be propagated with delay matching DQS clock tree latency to ensure data capture intra-chip intrinsic physical balance. However, we propose a clock-based sense amplifier and "pin-align topology" [Fig. 4(d)] to capture data on the IO pad for receiver design [10]–[12]. Typically one DQS is responsible for data capture on multiple DQ buses. Although it is much easier in pin align topology to adjust one DQS instead of multiple DQ buses, sensing data on the IO pad induces further overhead that requires a PLL or DLL block to de-skew internal clock tree latency [Fig. 4(d)]. This prompts another design concept that will be described in the next section.

C. Exclude PLL/DLL Usage in the Memory Site

A DLL block must be used to de-skew the extra clock tree latency to guarantee data capture in the "pin-align topology" [Fig. 5(a)]. However, some specific memory applications include low power, small area, and even a simple design as requirements for memory-side PHY design. We propose to exclude PLL/DLL usage in the memory site, so that we can further reduce memory site power and area. As shown in Fig. 5(b), we only implement the DLL block at the SOC site. Section V

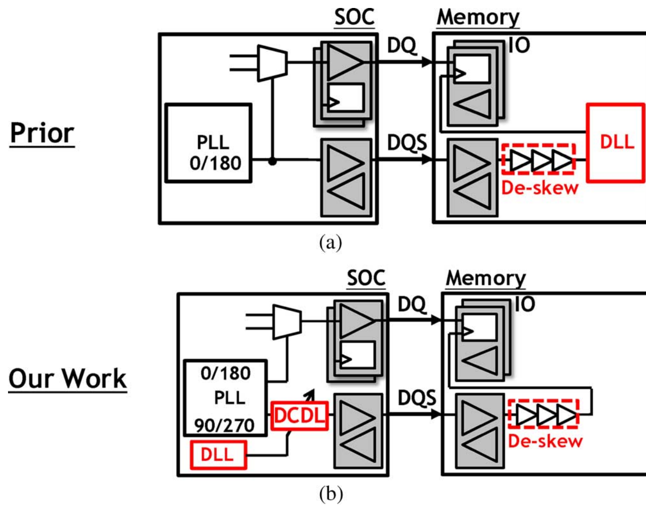


Fig. 5. Implementation of DLL to de-skew the extra clock tree latency. (a) DLL block implemented locally in memory site. (b) DLL block implemented in SOC site.

describes a mechanism for handling different process variation between the SOC and memory chip.

III. General Considerations

We demonstrate an eDRAM ASIC in CoWoS application with overall 1 Tbit/s bandwidth, which uses 1024 DQ buses each running at 1 Gbit/s based on certain design considerations.

A. Operation Speed, SII Length, and IO Power Tradeoff

Each DQ targets a 1 Gbit/s data rate while considering IO power and around a 1000 μm length SII load. The 1000 μm length SII for each DQ is decided by adequate ubump floor plan and contributes around 200 fF capacitive load. Adding in driver cell device load and ESD load at near-end and far-end sites, the IO has an overall capacitive load of about 1 pF [1], [2], [7]. Shorter SII length requires a more compact ubump floor plan, which placed a requirement for compact size on the IO.

B. Controlling the 1024-Bit DQ Skew

To relax physical design constraints for 1024-bit DQ skew, two approaches are employed in this work. First, 1024-bit DQ buses are separated into two hierarchies: "slice" and "mini-slice." Each level is composed of identical sub-macros. Each completed bottom level sub-macro (mini-slice) is considered as a hard macro and then duplicated. Second, the clock tree in the bottom sub-macro cell is designed using an analog approach to predict and control clock tree skew precisely.

C. Simultaneous Switching Output Noise

For wide bus applications, like this work, simultaneous switching output (SSO) noise is another critical problem [4]. Several approaches are adopted to mitigate the effect of SSO noise. First, good power integrity and uniform power distribution are achieved through adequate power and ground C4 numbers arranged in the ubump floor plan. Second, each mini-slice is a hard macro and time-domain simulation is performed at the mini-slice level to evaluate the overall decoupling capacitor required to reduce the SSO noise on a chip scale [13]. Third, the target impedance of package substrate design has been verified to guarantee power integrity. Most importantly, we also reserve the flexibility to adjust the reference compared voltage (VREF) for the IO receiver sense amplifier by ATE (automatic test equipment). VREF is nominally set to half VDDQ (ex: VREF = 150 mV for VDDQ = 300 mV). Any unbalanced SSO noise from power and ground can be compensated for by adjusting VREF according to shmoo test results. Note that a VREF calibration circuit is not implemented in this work.

D. Jitter Budget

A double-data rate (DDR) scheme is adopted for the data and clock structure in the silicon interposer for the data rate of 1 Gbit/s. Theoretically, center alignment between data and clock will be perfect, meaning that 500 ps are reserved for setup time and 500 ps are reserved for hold time. Taking out the setup/hold time requirement, the remaining timing margin is required to meet the jitter sources including: PLL jitter, near-pad-logic noise, clock tree skew, low-swing IO jitter, silicon-interposer mismatch, and DLL calibration/quantization error. Each jitter item should be well-defined.

IV. System Architecture

A. High-Level Architecture

Fig. 6 shows the system top architecture. 1024 DQ bus lines are arranged in two hierarchies: slice and mini-slice. The 1024 DQ bus lines are grouped into 4 slices. Each slice communicates with a single eDRAM channel. Each slice is further divided into 8 mini-slices [3]. Each mini-slice has a 32-bit DQ (SII_DQ[31:0]), two corresponding differential DQS's (SII_WDQSP/N and SII_RDQSP/N), and two corresponding data valid signals (SII_WD_VLD and SII_RD_VLD). SII_WDQSP/N is a strobe clock for the write path, whereas SII_RDQSP/N is for the read path. SII_WD_VLD is a data valid envelope signal for the write path, whereas SII_RD_VLD is for the read path. Each slice has one additional CA (command/address) mini-slice that is responsible for communicating with a single eDRAM channel through command/address codes (SII_CMD[6:0] and SII_ADR[14:0]). There is no PLL/DLL building block in the eDRAM PHY. PHYM relies on one differential clock source (SII_CKP/N) that is propagated from PHYC to PHYM and distributed into the eDRAM chip in each slice/channel. PHYC has one PLL for generating a quadrature phase clock source.

In order to perform skew compensation, four pairs of dummy differential clock trees (CAL_NDW_CKP/N, CAL_ADW_CKP/N, CAL_NDR_CKP/N, and CAL_ADR_CKP/N) are reserved in the silicon-interposer for each slice. They function with the PHYC built-in PLL/DLL to de-skew the clock tree latency in the PHYM, which has no PLL/DLL blocks. In summary, each slice has 9

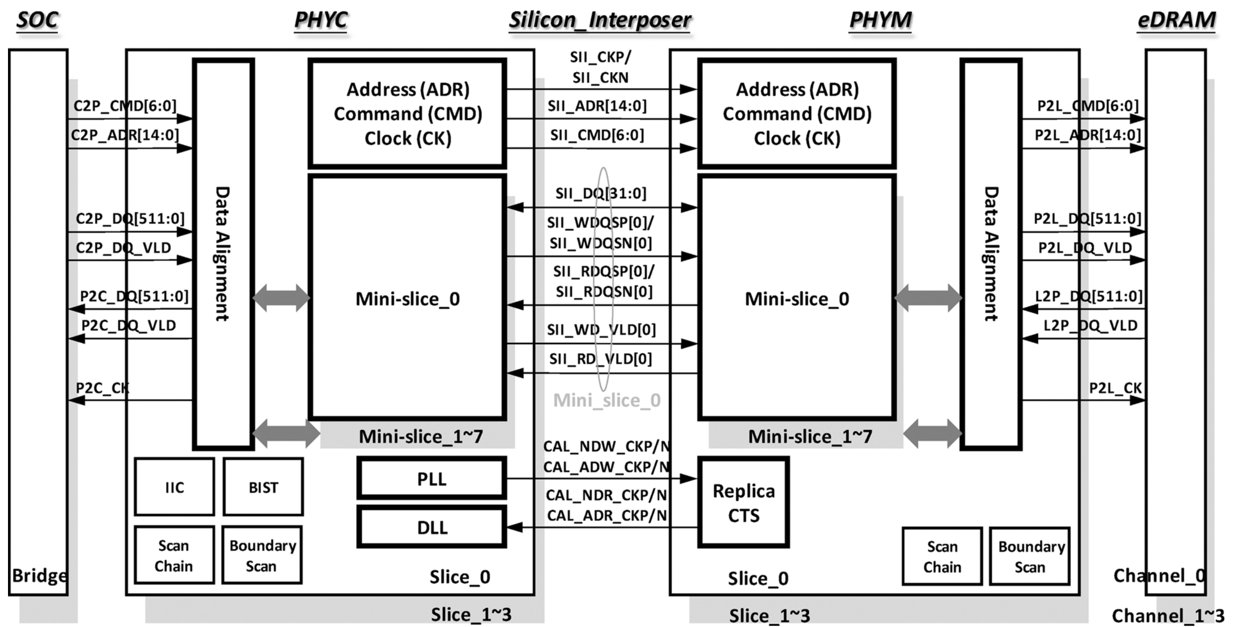


Fig. 6. System architecture.

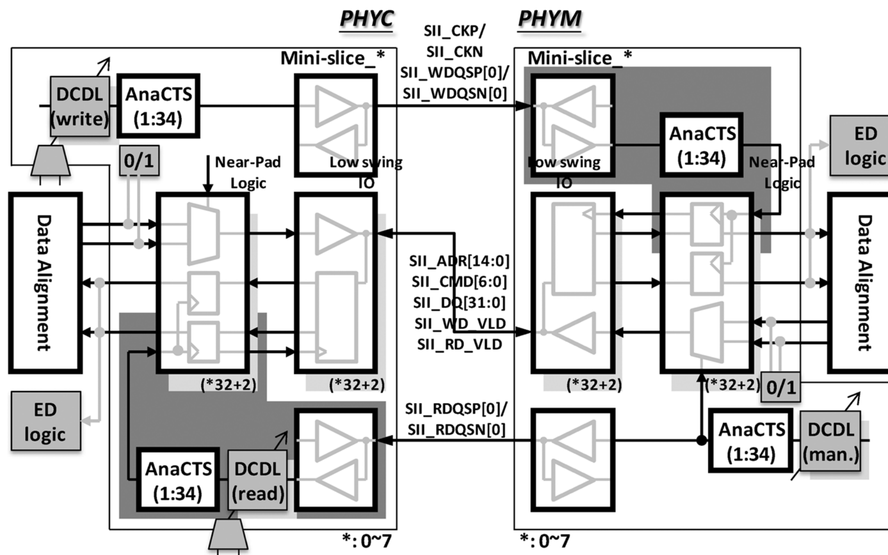


Fig. 7. Mini-slice architecture.

mini-slices. Each slice handles 256 bits of DQ. Each 256-bit DQ bus in the PHYC has its own PLL/DLL blocks.

The PHYC and PHYM are responsible for data multiplexing and de-multiplexing between 500 Mbit/s and 1 Gbit/s. We also support BIST (build-in-self-test), DFT, and boundary-scan features for yield screen at each milestone of the CoWoS process.

B. Mini-Slice Architecture

Fig. 7 shows the mini-slice architecture. Each mini-slice is designed as a hard macro and constructed using low-swing IO, near-pad-logic (NPL), and analog clock tree (AnaCTS). Low-swing IO is a key block for low power design, and near-pad-logic (NPL) is used to ensure clean timing between the IO and digital data paths, whereas analog clock tree (AnaCTS) can provide good control of skew performance. These three blocks are designed using an analog approach.

Taking the transmission data path from PHYC to PHYM as an example, in the PHYC side, 500 Mbit/s parallel data are multiplexed by NPL to 1 Gbit/s serial data and transmitted by low-swing IO. In the PHYM side, 1 Gbit/s serial data is captured by low-swing IO in the silicon-interposer and de-multiplexed at the same time. The downstream NPL aligns the timing of parallel data, and propagates the data to another digital circuit.

Data transmission between the SOC and eDRAM is now described. For SOC "write" to eDRAM, the PHYC employs a quadrature phase clock for DQ and WDQS respectively.

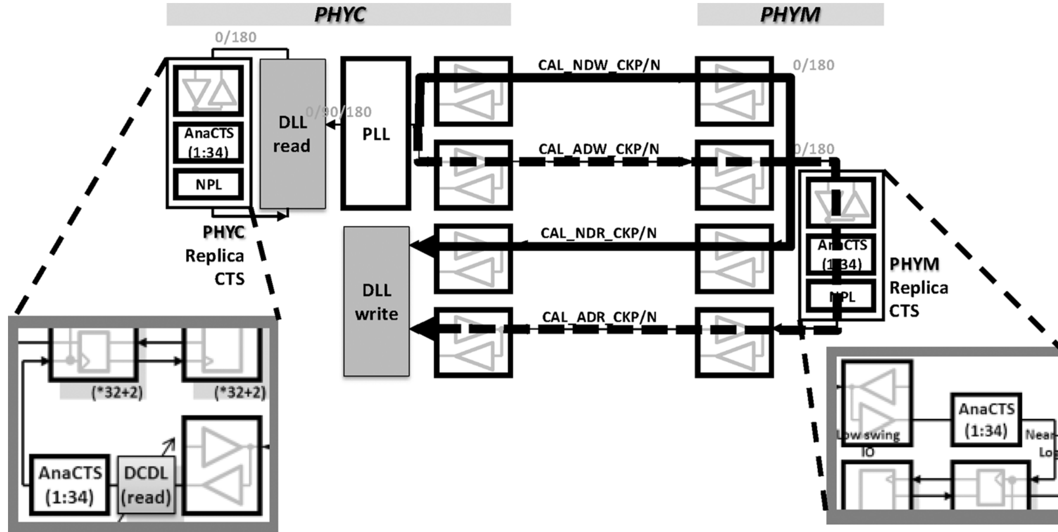


Fig. 8. Close-loop timing compensation scheme.

DQ and WDQS are intrinsically center-aligned. The extra clock tree in the PHYM as shown in Fig. 7 is de-skewed by the built-in WRITE-DLL of the PHYC. The WRITE-DLL calculates optimal delay, and outputs the delay code to control digitally controlled delay lines (DCDLs) on each WDQS. Center alignment is guaranteed in PHYM low-swing IO when data is captured. For SOC "read" from eDRAM, since the PHYM has only one differential clock source, DQ and RDQS are intrinsically edge-aligned to each other in the silicon-interposer. Another READ-DLL built in to the PHYC de-skews the additional clock tree and further provides 90-degree phase shift (Fig. 7). Center alignment is guaranteed when data is captured in PHYC low-swing IO. Note that the CMD/ADR mini-slice employs the same mini-slice design as the DQ.

V. Circuit Description

A. Closed-Loop Timing Compensation Scheme

The purpose of timing compensation is to shift the sampling clock at the far-end site to the center of data to ensure maximum timing margin for setup/hold time. DLL calculates optimal delay to control each DCDL of DQS. Fig. 8 shows the first timing compensation scheme of this work. Two pairs of dummy differential clock trees are propagated from PHYC to PHYM (CAL_NDW_CKP/N and CAL_ADW_CKP/N). One is directly fed back (CAL_NDR_CKP/N). Another is propagated through the PHYM replica clock tree and fed back to PHYC (CAL_ADR_CKP/N). The phase difference between these feedback clocks contains PHYM extra clock tree latency, and is brought back to PHYC and de-skewed by PHYC WRITE-DLL. This allows for chip variation in PHYM to be monitored in PHYC with a minimal cost of 8 pins in the silicon-interposer for each slice (per 256-bit DQ).

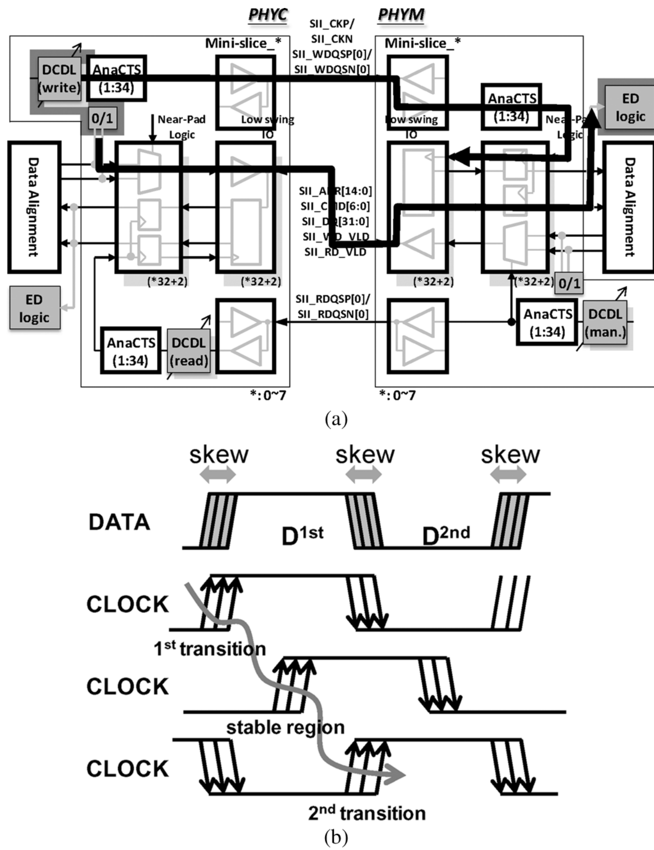
The read path uses a similar concept. The phase relationships between DQ and DQS that are transmitted from PHYM to PHYC are intrinsically edge-aligned. The same DLL is duplicated as READ-DLL. With aid of the quadrature phase clock source in the PHYC, the READ-DLL de-skews the extra clock tree latency in the PHYC when the clock propagates through another replica clock tree [Fig. 8] for the PHYC and provides an additional 90-degree phase shift to the clock. With 90-degree phase shift, center alignment is guaranteed again between DQ and DQS.

In summary, each slice in the PHYC has one PLL and two DLL blocks shared by 8 mini-slices. Each mini-slice has its own DCDL and is controlled by the same code from the DLL's adaptive result in this close-loop timing compensation scheme.

B. Data Sampling Alignment Training

The former mechanism is based on the assumption that physical balance and silicon-interposer skew are well-controlled. Unexpected skew in the close-loop timing compensation mechanism could cause data sampling failure, so a systematic "data sampling alignment training" is adopted in this design as shown in Fig. 9. Instead of transmitting a complex data pattern, a repeating 0-1-0-1 clock signal is transmitted in the original data path. The transmitted clock signals for each 32-bit DQ (ex: DQ[31:0]) contain some skew contributed by the PHYC clock tree and silicon-interposer wire mismatch. The sampling clock is moved systematically by adjusting the DCDL delay step-by-step from one transition region to a stable region, then to another transition region. Additional edge detector (ED) logic is arranged right after the output of NPL on the receiver side. Sampling status can be monitored from ED output. The ED logic outputs "1" if the clock rising edge captures all 1's or the clock falling edge captures all 0's on the data bus, which implies a "stable region." Otherwise the ED logic outputs "0," which implies a "transition region." The optimized DCDL code that ensures center alignment is derived as the middle of the codes at the two transition regions.

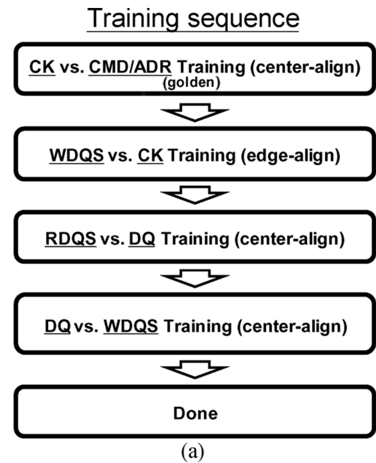
A training flow according to our clock domain is shown in Fig. 10(a). Initially, we fix the delay to the CMD/ADR's DCDL. We adjust the DCDL of CK to make CK centrally align to CMD/ADR. Capture of CMD/ADR by CK is thus guaranteed. We then adjust the DCDL of WDQS to make WDQS edge-aligned



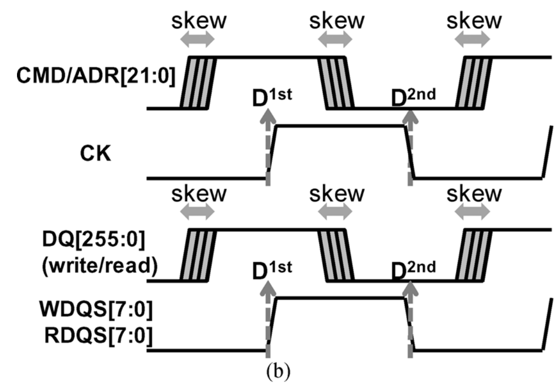
(a)

(b)

Fig. 9. Data sampling alignment training. (a) Training concept illustration (b) Adjusting sampling clock to search data boundary.



(a)



(b)

Fig. 10. (a) Data sampling alignment training. (b) Timing diagram after training is finished.

with CK. We adjust the DCDL of RDQS to make RDQS centrally align to “read” path DQ. The read path data capture is thus guaranteed. We then adjust the DCDL of DQ in the write path to make WDQS centrally align with DQ. The write path data capture is thus guaranteed. Finally the edge or center alignment relationship will be acquired as shown in the timing diagram in Fig. 10(b). In summary, each mini-slice has dedicated DCDL for WDQS[i], RDQS[i], and also for write path DQ[31:0]. As shown in Fig. 7, DCDL control can be switched to another mode in which each DCDL in each mini-slice is adjusted individually. This training scheme can also be used to characterize the horizontal timing margin of the eye in the silicon-interposer.

C. Low-Swing IO

To save power consumption in wide bus operation on 2.5D/3D IC designs, it is necessary to provide a low voltage swing signal without termination. A bidirectional compact I/O designed to sustain wide supply voltage range of VDDQ from VDD down to 0.3 V is presented.

1) Transmitter: Transmitter’s post-driver with wide range supply (VDDQ = 0.3 V-VDD) accommodation provides signal swing from ground to VDDQ [Fig. 11(a)]. Similar to the conventional push-pull driver, a PMOS pull-up driver (pull-up path 2) is designed for VDDQ closed to VDD and functions with an NMOS pull-down driver. Another NMOS pull-up (pull-up path 1) is designed for VDDQ around 0.3 V, and controlled by the inverse of the gate signal. However, VDDQ close to the middle of VDD creates a weak window. The pre-driver is supplied by core voltage (ex: 0.9 V), so the pull-up driver is intrinsically weaker than the pull-down driver. In this supply operation window, both pull-up paths 1 and 2 weakly turn on and limit the operation speed of low-swing IO. An additional pre-emphasis pull-up PMOS driver supplied by VDD is added to ensure over 2 Gbit/s operation speed. The pre-emphasis function can enhance the pull-up path in advance of a real data stream. When the pre-emphasis pull up path is enabled, the low-swing IO can operate at up to 4 Gbit/s data rate, and drive 3000 μm of SII trace in simulation results.

2) Receiver: A clock-based sense amplifier with S-R latch is chosen for the pin-align application. As shown in Fig. 11(b), in order to accommodate a wide range of input signal swing, PMOS and NMOS input stages are designed in hybrid. The sense amplifier compares data with a reference voltage (VREF) that is equal to half VDDQ. Two identical sense amplifiers in parallel function as a 1-to-2 de-mux for double data rate DQ. The receiver only consumes dynamic power during clock switching. Thus, the receiver power is reduced significantly.

D. DLL and DCDL

Two DLL calibration mechanisms are employed in the closed-loop timing compensation scheme: WRITE-DLL and

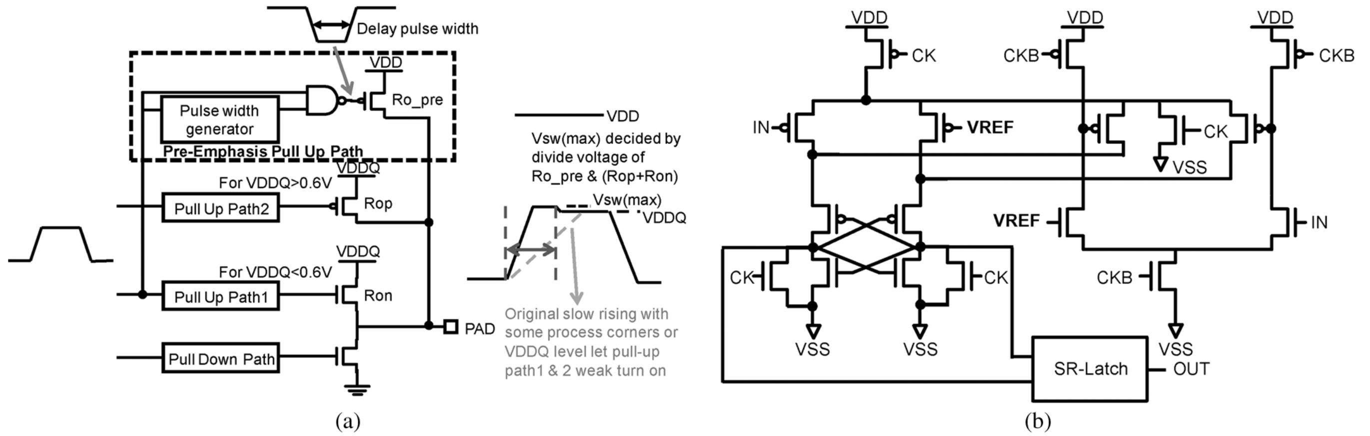


Fig. 11. Low-swing IO circuit. (a) Transmitter. (b) Receiver.

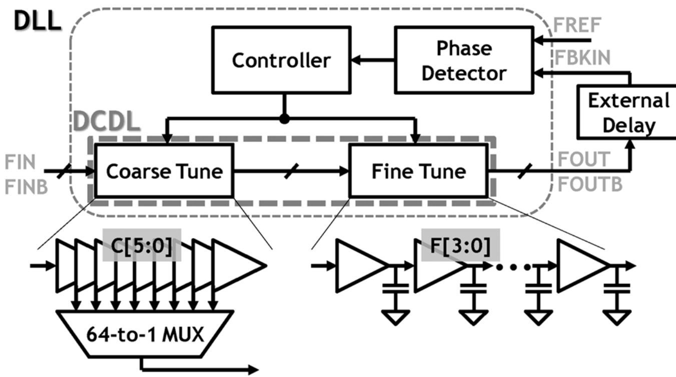


Fig. 12. DLL and DCDL architecture.

READ-DLL. Fig. 12 shows DLL and DCDL architecture. Each DLL has one embedded DCDL cell that is equivalent to all other DCDLs dedicated to DQ and DQS. Each DCDL is constructed with a 6-bit, 64-stage buffer chain as a coarse tuning stage with 40 ps resolution followed by a 4-bit 16-stage buffer chain as a fine tuning stage with 5 ps resolution. Coarse tuning delay is decided by selecting the output of the buffer chain by a MUX, whereas the fine tuning delay is decided by turning on/off the capacitive load at the output of each buffer chain. The DLL controller initiates the calibration with the coarse tuning loop first. The fine tuning loop begins calibration once the coarse tuning loop is locked. The fine tuning loop starts from the center of the fine tuning binary code, i.e., [1000]. Fine tuning delay is designed to be greater than 2 times the course tuning LSB delay in order to guarantee fine tune lock. As shown in Fig. 13, the replica clock tree latency may be greater than 1 unit interval (UI), so at least 2 ns delay line capability at fast-fast corner is maintained. Thus, the DLL algorithm can still align to the second rising edge, so that DQSP rising edges align to even bits, and DQSN rising edges align to odd bits.

E. Ubump Floor Plan/Other Considerations

A compact floor plan results in many advantages in chip implementation. Fig. 14(a) shows the slice-scale ubump floor plan. Since there are no PLL/DLL blocks, the PHYM occupies 37% less area than the PHYC. Again, each mini-slice has 32 DQ ubumps. The PHYC and PHYM have a symmetric floor plan to guarantee the same length SII for each DQ. The low-swing IO and NPL for each DQ are arranged within 2 ubump's pitch to achieve a compact floor plan. A compact floor plan results in shorter SII length, lower IO driving strength, lower IO SSO noise, less power/ground C4 bump requirement, and further reduced PHY area. Each mini-slice is designed as a hard macro and duplicated to the entire 1024-bit DQ bus. Each DQ has identical layout pattern with ground shielding and return current path included for good signal integrity [Fig. 14(b)]. Designs using as large as a 1024-bit DQ bus with 1050 μm SII wire length exhibit less than 3 ps skew in simulation results.

VI. Experimental Results

The proposed CoWoS platform with PLL/DLL-less eDRAM PHY is fabricated in TSMC CMOS technology. An estimated power consumption breakdown table for PHYC and PHYM are listed in Fig. 15(a), (b) respectively. PHYC incurs an additional 118 mW of power consumption contributed by PLL, DLL, and DCDLs.

Fig. 16 shows the layout snapshot at chip-on-wafer (CoW) scale. Four chips are stacked on one interposer. The bottom two chips are eDRAM and SOC. An eDRAM PHY (PHYM) occupies only 9792 μm $\times$ 1113 μm area with a 1024-bit DQ bus, which is 37% less area than the PHYC.

Fig. 17 shows the die photo after chip-on-wafer (CoW) process. Known-good-dies for eDRAM and SOC chips are stacked on a single silicon-interposer wafer, and another known-good-stack (KGS) CP test is then performed. Fig. 18(a) and (b) show the known-good-stack (KGS) CP shmoo test results for SOC to eDRAM READ/WRITE test. This is the most complicated test loop available between the SOC chip and the eDRAM chip. Each pass dot in the shmoo test results has passed 70 Mbit-length pattern comparison without error, which translates to at least BER of 10^{-7}. We sweep VDD versus clock frequency based on VDDQ equal to 0.3 V. The objective is to test the operation frequency versus system supply. Up to 550 MHz of clock frequency is achieved

Fig. 13. Illustration of DCDL delay capability requirement. (a) PHYM replica clock tree latency <1 ns. (b) PHYM replica clock tree latency >1 ns.

Fig. 14. Physical implementation example. (a) Per slice micro-bump/C4-bump floor plan. (b) Layout example in silicon interposer.

PHYC Blocks	Power Consumption
PLL (2.5V/1.1V)	35.2
DLL (1.1V)	10.4
DCDL (1.1V)	72.0
NPL (1.1V)	190.8
LowSwingIO (1.1V)	82.3
LowSwingIO (0.3V)	50.0
Digital (1.1V)	608.0
SUM	1048.7
	(mW)

(a)

PHYM Blocks	Power Consumption
NPL (0.9V)	362.4
LowSwingIO (0.9V)	60.7
LowSwingIO (0.3V)	46.8
Digital (0.9V)	262.8
SUM	732.7
	(mW)

(b)

Fig. 15. Power consumption breakdown. (a) PHYC part. (b) PHYM part.

TABLE I
FEATURE COMPARISON WITH RECENT WORK

	[1] 2009 JSSC	[2] 2011 ISSCC	[3] 2011 JSSC	[4] 2012 ISSCC	[5] 2013 ISSCC	[6] 2013 VLSI	This Work
CMOS (nm)	65	50	45	45	90	65	40LP/40G
Vsw (V)	1/0.5	1.2	1.05	0.3/0.4	1.2	1.2	0.3
Bus Width	12	512	512	8	4096	512	1024
Channel	SII 40mm/2mm	1*TSV	1*TSV	6*TSV	1*TSV	1*TSV	SII 1mm
Data Rate (Gb/s/pin)	8.9/10.8	0.2	16	2.0/5.2	0.2	0.2	1
Toggle Rate	PRBS7	50%	PRBS	-	100%	-	100%
IO Power Eff. (mW/Gbps)	1.9/1.3	0.78	0.94	0.2/0.5	0.56	0.9	0.105

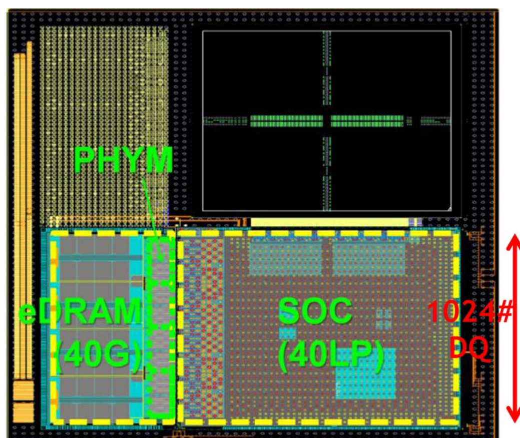


Fig. 16. Layout snapshot at CoW (chip-on-wafer) scale.

(equivalent to a 1.1 Gbit/s data rate) for ±10% VDD variation. The failed case is caused by timing violation of internal logic or out of lock of PLL. A higher supply voltage or a lower data rate induces better timing margin. We then sweep VDDQ versus clock frequency based on VDD equal to 1.1 V. This tests the low-swing IO for wide range VDDQ accommodation. Again 550 MHz clock frequency is achieved for VDDQ from nominal 0.9 V down to 0.3 V. Straight line behavior of the pass/fail results in the shmoo diagram is observed [Fig. 18(b)]. It is suspected that data capture failure in the silicon-interposer

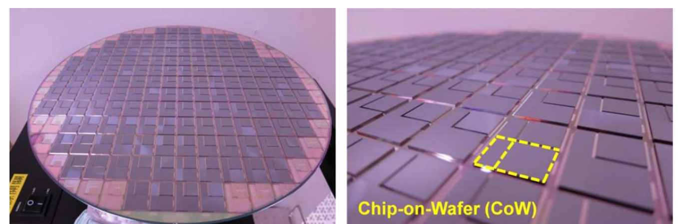


Fig. 17. Die photo after CoW (chip-on-wafer) process.

occurs when low signal amplitude conflicts with exacerbated SSO noise from power and ground.

VII. CONCLUSION

This paper presents a CoWoS eDRAM platform. Two chips: SOC and eDRAM have been fabricated in TSMC 40 nm CMOS technology and stacked on another silicon interposer chip. Adopting two novel timing compensation mechanisms, PLL/DLL function blocks can be excluded to achieve a small area PHYM. A low-swing IO accommodating wide range VDDQ supply from VDD down to 0.3 V is also presented to achieve extra low power consumption. Operation of all 1024 data buses at 1.1 Gbit/s with VDDQ = 0.3 V is proven after CoWoS manufacture in experimental results through SOC-to-eDRAM READ/WRITE test. The adopted low swing IO also achieves good power efficiency of 0.105 mW/Gbps compared with the recent works shown in Table I.

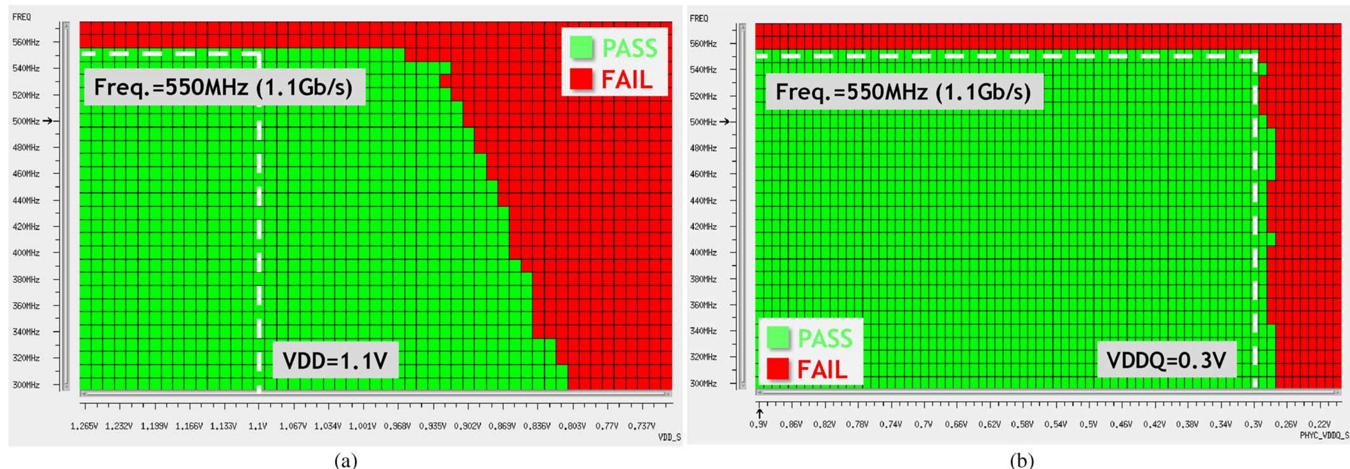


Fig. 18. SOC to eDRAM READ/WRITE measurement shmoo test. (a) VDD vs. Frequency. (b) VDDQ versus Frequency.

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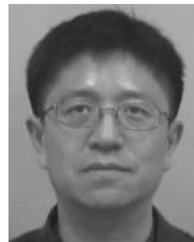

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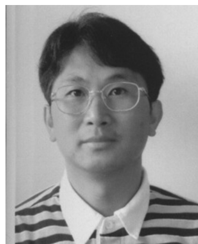

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