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Investigation of channel width-dependent threshold voltage variation in a-InGaZnO thin-film transistors

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This Letter investigates abnormal channel width-dependent threshold voltage variation in amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistors. Unlike drain-induced source barrier lowering effect, threshold voltage increases with increasing drain voltage. Furthermore, the wider the channel, the larger the threshold voltage observed. Because of the surrounding oxide and other thermal insulating material and the low thermal conductivity of the IGZO layer, the self-heating effect will be pronounced in wider channel devices and those with a larger operating drain bias. To further clarify the physical mechanism, fast IV measurement is utilized to demonstrate the self-heating induced anomalous channel width-dependent threshold voltage variation. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4868430]

Many recent consumer products require the extensive use of low power consumption IC,[1] non-volatile memory,[2–7] and thin film transistors (TFTs).[8,9] TFTs with active layers composed of transparent oxide-based semiconductors, such as ZnO and amorphous InGaZnO (a-IGZO), have attracted much attention due to their considerable potential application in flat, flexible, and transparent displays.[10–12] In particular, a-IGZO thin film transistors have been widely investigated for the next generation of the display industry owing to their good uniformity, high mobility, excellent transparency to visible light, and room temperature fabrication.[12–15] Therefore, they are very promising alternatives to replace amorphous silicon TFTs for application in active matrix liquid crystal displays (AMLCD) and organic light-emitting diode displays (AMOLED) as switching/driving devices. However, there are some difficulties which are necessary to overcome for oxide TFTs to be practical in these applications, such as instability under gate bias stress or the surrounding ambiance.[16–19] Moreover, a-IGZO TFTs can also be used for gate driver on array (GOA) technology. Conventionally, driving ICs have been fabricated through CMOS technology and mechanically attached to the sides of the panel. However, GOA technology fabricates gate driver ICs on the array itself instead of attaching them to the panel sides. As a result, GOA technology can reduce process steps and cost as well as achieving thinner panels with narrower edge.[20,21] However, mobility of driving ICs fabricated by single crystal silicon is about one hundred times that of a-IGZO. As a result, in order to achieve the same driving current, it is necessary to increase channel width of a-IGZO TFTs for GOA operation. Therefore, investigating the performance and reliability of a-IGZO TFTs with large channel width is of great importance.

The n-type a-IGZO TFTs in this work were fabricated with a bottom gate and back-channel-etching structure. The double-layer Cu/Mo (500/20 nm) gate electrodes films were deposited and then patterned via photolithography on a glass substrate. Then 300-nm-thick Si_3N_4 and 70-nm-thick SiO_2 gate dielectric films were sequentially deposited on the patterned gate electrode by plasma enhanced chemical vapor deposition (PECVD). An active layer of 30-nm-thick a-IGZO film was deposited by DC magnetron sputtering using a target of In_2O_3:Ga_2O_3:ZnO = 1:1:1 in atomic ratio at room temperature, and then patterned. The Mo/Cu (20/500 nm) source/drain electrodes were formed by DC-sputtering and then patterned. Finally, 160-nm-thick SiO_2 and 50-nm-thick Si_3N_4 were sequentially deposited as a passivation layer by PECVD. After that, the device was annealed in an oven at 300 °C for 2 h in a dark environment. In this Letter, the conventional and fast I-V measurements were performed by Agilent B1500A and Agilent B1530A semiconductor analyzers, respectively. The device dimensions of channel width/length (W/L) were 100, 500, 1000, 5000, and 10 000 μm/5.5 μm. The threshold voltage is defined as the gate voltage when the normalized drain current ($NI_D = I_D \times L/W$) reaches 1 nA, where L and W are channel length and width, respectively. All measurements were performed in a dark environment.

Figures 1(a) and 1(b) show the normalized I_D-V_G curve at $V_D = 1$, 5, 10, and 20 V, with W/L = 100/5.5 μm for Figure 1(a) and W/L = 10 000/5.5 μm for Figure 1(b). Obviously, threshold voltage increases with increasing drain voltage. Furthermore, the larger the channel width, the larger threshold voltage that can be observed. Conventionally, channel width and drain voltage do not affect threshold

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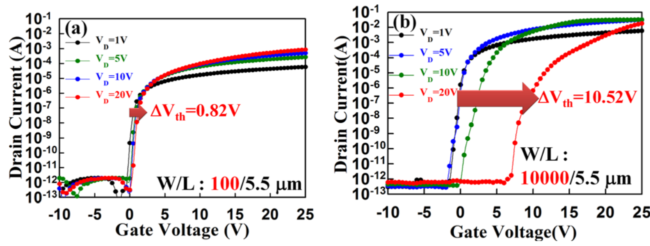

FIG. 1. I_D-V_G transfer characteristic of a-IGZO TFT operated at $V_D = 1$, 5, 10, and 20 V for (a) W/L = 100/5.5 μm. (b) W/L = 10 000/5.5 μm.

voltage in long channel devices. However, this anomalous threshold voltage variation depends on channel width and drain voltage that are observed in Figures 1(a) and 1(b).

In order to inspect this phenomenon further, Figure 2 illustrates the threshold voltage shift versus various channel width and drain voltages, with threshold voltage shift defined as V_{th}(measurement) − V_{th}(@$V_D = 1$ V). Note that at low drain voltage ($V_D = 5$ V), threshold voltage shift is negligible and unapparent, with the same being true for relatively small channel widths (W = 100 μm) at all drain voltages. As W ≧ 500 μm and V_D ≧ 10 V, a significant threshold voltage shift can be observed with increasing channel width and increasing drain voltage. Accordingly, the abnormal channel width-dependent threshold voltage variation may in fact be induced by the self-heating effect.[22] It is well known that the self-heating effect arises in silicon-on-insulator (SOI) MOSFETs and low-temperature-polycrystalline silicon (LTPS) TFTs, a situation quite similar to that in the IGZO channel layer.[23] In addition, the thermal conductivity of IGZO is much lower than Si and is comparable to SiO_2. Therefore, heat dissipation in IGZO TFTs is relatively more difficult than in Si-based TFTs.[24] Because the larger drain voltage will form a higher drain current, resulting in higher power (P = IV), the heat in channel will be higher, resulting in a more severe self-heating effect. Furthermore, because the heat will more likely accumulate at the center of the channel region and dissipate to the surrounding materials along the channel width direction, larger channel widths make heat dissipation in channel more difficult, again resulting in a more pronounced self-heating effect.[25] The inset of Figure 2 shows the energy band diagram. When the large channel width TFT is operated at high drain voltage, significant self-heating effect will occur, and channel electrons will

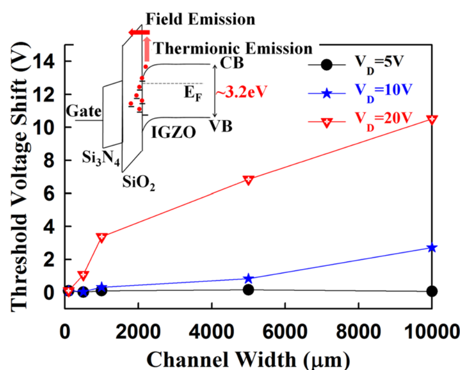

FIG. 2. Dependence of threshold voltage shift on the channel width and drain voltage. The inset illustrates the thermionic-field emission process of electron trapping.

be trapped at the IGZO/SiO_2 interface or in SiO_2 bulk through the thermionic-field emission process, resulting in a larger observed threshold voltage.[22,26,27] In addition, from Figure 1(b), note that threshold voltage shifts without obvious variation of the slope in transfer characteristics. This indicates that no additional trapping states are created at the IGZO active layer/gate dielectric interface during the trapping process, resulting in unobvious mobility and subthreshold swing degradation.[28–30]

In order to confirm that the abnormal channel width-dependent threshold voltage variation is indeed induced by self-heating effect, the I_D-V_D output characteristic is performed. Figures 3(a) and 3(b) show the I_D-V_D curve at a fixed channel length (5.5 μm) but different channel widths (100 μm and 10 000 μm, respectively). Compared to the W = 100 μm device, the W = 10 000 μm one exhibits the anomalous output characteristic. When the measurement drain voltage exceeds approximately 15 V, drain current decreases instead of saturating with an increase in drain voltage. The heat dissipation in channel will be rather difficult for the W = 10 000 μm device because of the considerably large channel width. As the large channel width device is operated at high drain voltage conditions (V_D ≧ 15 V here), a severe self-heating effect-induced charge trapping phenomenon will occur, resulting in a considerable threshold voltage shift. Because of this large threshold voltage shift, the abnormal drain current decreases as drain voltage increases when V_D ≧ 15 V.

To further confirm the proposed self-heating effect induced anomalous channel-width dependent threshold voltage variation, fast IV measurement is performed. The inset of Figure 4(a) illustrates the waveform of conventional I_D-V_G measurement in which drain voltage is fixed with gate voltage performed stepwise. Note that the time scale of each gate voltage step is on the order of milliseconds (ms). For comparison, the inset of Figure 4(b) shows the waveform of fast I_D-V_G measurement in which drain voltage is fixed with gate voltage performed in a pulse form. Significantly, the time scale of peak/base time is rather short, approximately on the order of microseconds (μs). From previous research,[21] sufficient heating time is necessary for Joule heating to take place within the channel, resulting in a pronounced self-heating effect-induced charge trapping phenomenon. This sufficient heating time is approximately on the order of ms. Because the gate pulse peak/base time in fast I-V measurement is on the order of μs, the short heating time is insufficient for Joule heating to occur. Therefore, use of the fast I-V measurement will exclude the self-heating effect induced-charge trapping

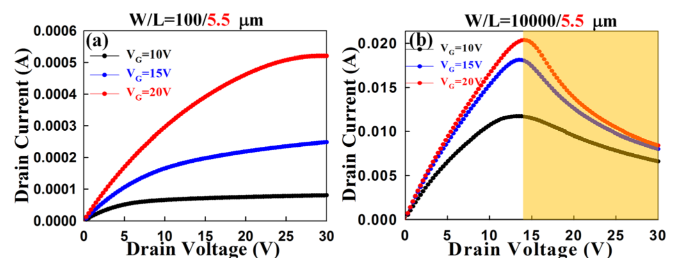

FIG. 3. I_D-V_D output characteristic of a-IGZO TFT operated at $V_G = 10$, 15, and 20 V for (a) W/L = 100/5.5 μm. (b) W/L = 10 000/5.5 μm.

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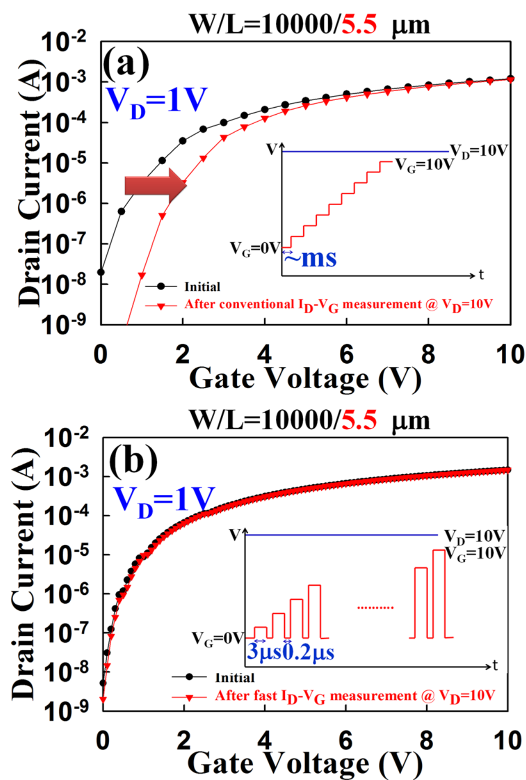

FIG. 4. The transfer characteristic of a-IGZO TFT with W/L = 10 000/5.5 μm before and after measuring at high drain voltage ($V_D = 10$ V) by (a) conventional I_D-V_G measurement. (b) Fast I_D-V_G measurement. The inset of Figure 4(a) and 4(b) illustrate the waveform of conventional and fast I_D-V_G measurement, respectively.

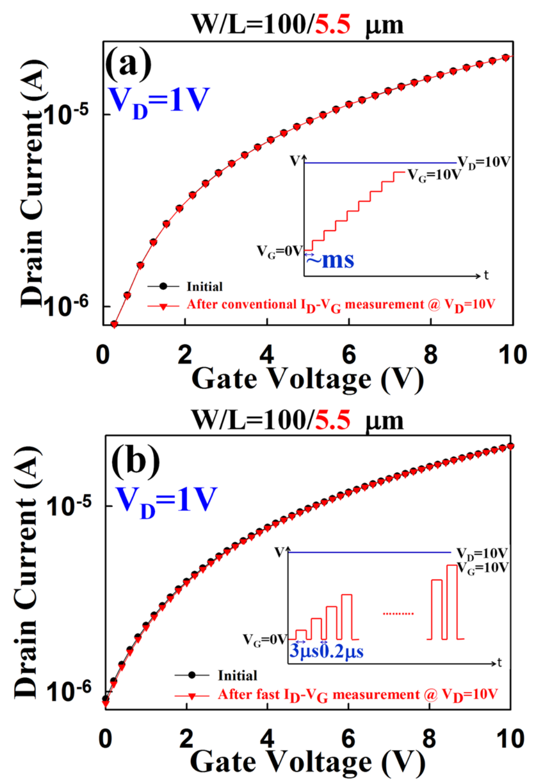

FIG. 5. The transfer characteristic of a-IGZO TFT with W/L = 100/5.5 μm before and after measuring at high drain voltage ($V_D = 10$ V) by (a) conventional I_D-V_G measurement. (b) Fast I_D-V_G measurement. The inset of Figure 5(a) and 5(b) illustrate the waveform of conventional and fast I_D-V_G measurement, respectively.

phenomenon, and therefore threshold voltage shift can also be excluded. The measurement sequences of Figures 4(a) and 4(b) are as follows. First, I_D-V_G curve is measured by conventional I_D-V_G measurement at low drain voltage ($V_D = 1$ V) to avoid the self-heating effect and act as the initial state. Second, I_D-V_G curve is measured at high drain voltage ($V_D = 10$ V) by conventional I_D-V_G measurement for Figure 4(a) and by fast I_D-V_G measurement for Figure 4(b). Finally, I_D-V_G curve is measured by conventional I_D-V_G measurement at low drain voltage ($V_D = 1$ V) to serve as the final state. Clearly, there is a positive threshold voltage shift between initial and final states after conventional I_D-V_G measurements at high drain voltage ($V_D = 10$ V), as shown in Figure 4(a). During the conventional I_D-V_G measurement ($V_D = 10$ V), there was sufficient heating time for Joule heating to occur, leading to the self-heating effect-induced charge trapping phenomenon and resulting in the threshold voltage shift between initial and final states. Conversely, during the fast I_D-V_G measurement ($V_D = 10$ V), the insufficient heating time required for Joule heating results in no threshold voltage shift being observed, as shown in Figure 4(b). The fast I_D-V_G measurement further corroborates that the abnormal channel-width dependent threshold voltage variation does in fact result from the self-heating effect-induced charge trapping phenomenon. In addition, no matter the second measurement step, which is with $V_D = 10$ V, is carried out with conventional or fast I_D-V_G measurement, there is no threshold voltage shift between initial and final states, as shown in Figures 5(a) and 5(b). This indicates that channel width is an important factor in the self-heating effect-induced charge trapping phenomenon because larger channel widths make heat dissipation in channel more difficult.

This paper has investigated the anomalous channel width-dependent threshold voltage variation in a-IGZO TFTs. Devices with larger channel widths and which are operated at higher drain voltages will produce larger threshold voltages, with the effect becoming even more pronounced as channel width or drain voltage increases. This is due to the surrounding oxide and other thermal insulating material and the low thermal conductivity of the IGZO layer. The more pronounced self-heating effect is a product of both the more difficult heat dissipation in wider channels as well as the higher drain current in devices operated at higher drain voltages. Because sufficient heating time (approximately on the order of ms) is necessary for Joule heating to take place within the channel, the fast I_D-V_G measurement is performed to confirm the proposed mechanism. Because the time scale of the peak/base time in the fast I_D-V_G measurement is shorter, on the order of μs, the heating time is insufficient for Joule heating, resulting in no observed threshold voltage shift. The fast I_D-V_G measurement confirms that the abnormal channel-width dependent threshold voltage variation is due to the self-heating effect induced-charge trapping phenomenon.

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