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# Investigation of abnormal negative threshold voltage shift under positive bias stress in input/output n-channel metal-oxide-semiconductor field-effect transistors with TiN/$HfO_2$ structure using fast I-V measurement

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This letter investigates abnormal negative threshold voltage shifts under positive bias stress in input/output (I/O) TiN/$HfO_2$ n-channel metal-oxide-semiconductor field-effect transistors using fast I-V measurement. This phenomenon is attributed to a reversible charge/discharge effect in pre-existing bulk traps. Moreover, in standard performance devices, threshold-voltage ($V_t$) shifts positively during fast I-V double sweep measurement. However, in I/O devices, $V_t$ shifts negatively since electrons escape from bulk traps to metal gate rather than channel electrons injecting to bulk traps. Consequently, decreasing pre-existing bulk traps in I/O devices, which can be achieved by adopting $Hf_xZr_{1-x}O_2$ as gate oxide, can reduce the charge/discharge effect. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4868532]

As metal-oxide semiconductor field-effect transistors (MOSFETs) continue to shrink, the scaling of $SiO_2$ gate dielectrics is reaching its critical limit of only a few atomic layers thick. This scale causes a rise in gate current, performance degradation, and an increase in power dissipation. Many years of research and development has shown that one valid way to solve these problems is by replacing conventional $SiO_2$ gate dielectric with high-k dielectric, especially with $HfO_2$ gate dielectric. $HfO_2$ gate dielectrics have been implemented at the 32 nm technology node and smaller, with manufacturer Intel using high-k/metal gate beginning with their 45 nm node. Furthermore, high-k gate dielectric can be integrated with strained-silicon,[1] silicon on insulator (SOI),[2–4] and architectures to improve device characteristics. High-k dielectric can also be combined with thin-film transistor devices[5–9] and memory devices.[10–12] $HfO_2$ dielectrics have been heavily studied in recent years to replace $SiO_2$-based dielectrics.[13,14] Simultaneously, contemporary input/output (I/O) devices were integrated into the technology. $SiO_2$ and high-k/metal gate architectures have been incorporated for these I/O devices, which face significant reliability challenges. While there have been a few studies investigating reliability in I/O devices using fast I-V measurement, this study mainly focuses on positive bias stress (PBS) in $HfO_2$ dielectric I/O n-MOSFETs using fast I-V measurement. The causes of the abnormal threshold-voltage ($V_t$) shift are explained in this letter.

The $HfO_2$/metal gate n-channel MOSFETs used in this study were fabricated with a gate first process flow. First, a high quality 1-nm or 3-nm thick thermal oxide was grown as an interlayer. Second, 3 nm of $HfO_2$ dielectrics were sequentially deposited by atomic layer deposition. Third, 10 nm-thick TiN metal gates were deposited by radio frequency physical vapor deposition because metal gates can eliminate gate depletion and resist remote phonon scattering.[15,16] Next, polycrystalline silicon was deposited as a low resistance gate electrode. Finally, the dopant activation was performed at 1025 °C. During PBS, $I_d$-$V_g$ sweep curves using fast I-V technology are measured with 30 mV drain voltage, 0.6 V ~ 1.7 V gate voltage, an integral time of $7 \times 10^{-6}$s, a step edge of $5 \times 10^{-7}$s, and step number of 10. $I_d$-$V_g$ for double sweep fast I-V curves with fixed base level voltage ($V_{base\ level}$) or fixed high level voltage ($V_{high\ level}$) were measured with 30 mV drain voltage, an integral time of $1 \times 10^{-5}$s, step edge of $1 \times 10^{-8}$s, and step number of 80. In addition, hold time and delay time were both 5 s in order to ensure the steady state in $V_{base\ level}$ and $V_{high\ level}$. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer and a Cascade M150 probe station.

Figure 1(a) shows $\Delta V_t$-log (stress time) characteristic curves with 30 mV drain voltage under PBS over 500 s in $HfO_2$ (3 mn)/$SiO_2$ (3 nm) I/O devices using fast I-V measurement. Obviously, it exhibits an abnormal $V_t$ shift in the negative direction after PBS. In addition, $V_t$ shifts more with an increase in the stress voltage ($V_{stress}$). Figure 1(b) shows subsequent $\Delta V_t$-log (recovery time) characteristic curves after these stress conditions with a recovery voltage ($V_{recovery}$) of 0 V. Clearly, $V_t$ recovers more after PBS at a larger voltage, with $V_t$ completely recovering at all voltages. Figure 1(c) shows $\Delta V_t$-time under 500 s PBS and 500 s recovery for different stress voltages and the same recovery voltage ($V_{recovery} = 0$ V). Distinctly, in conventional (slow) measurement, there is no significant $V_t$ shift for 500 s PBS and 500 s recovery. On the contrary, in fast I-V measurement, there is an apparent $V_t$ shift under these operations. This phenomenon indicates that conventional measurement detects the $V_t$ shift after complete recovery since integral time is too slow to detect $V_t$ degeneration. Figure 1(d) shows $\Delta V_t$-time with $V_{stress} = V_t + 1.3$ V and $V_{recovery} = 0$ V, 0.8 V, 1.6 V under

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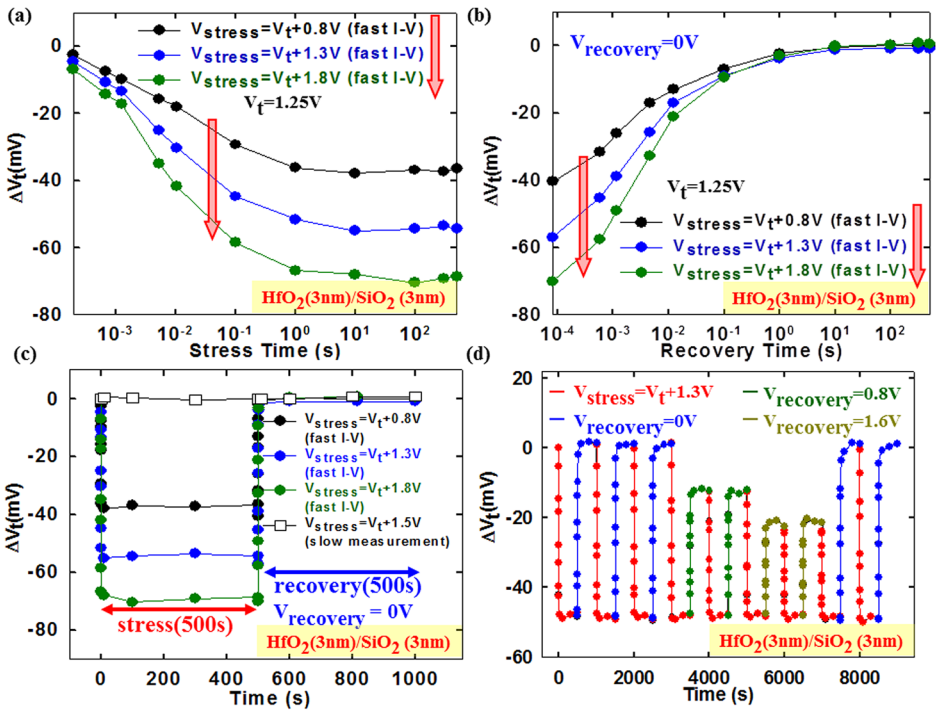


FIG. 1. (a) $\Delta V_t$-log (stress time) characteristic curves under different PBS. (b) $\Delta V_t$-log (recovery time) characteristic curves after different PBS when $V_{recovery} = 0$ V. (c) $\Delta V_t$-time under 500 s PBS and 500 s recovery with different stress voltages and the same recovery voltage ($V_{recovery} = 0$ V). (d) $\Delta V_t$-time with $V_{stress} = V_t + 1.3$ V and $V_{recovery} = 0$ V, 0.8 V, 1.6 V under 500 s PBS and 500 s recovery for nine cycles.

500 s PBS and 500 s recovery over nine cycles. With a rise in $V_{recovery}$, $V_t$ recovery decreases. Moreover, after seven stress/recovery cycles, $V_t$ entirely recovers in the eighth and ninth cycles with $V_{recovery} = 0$ V. These processes are, therefore, indeed reversible and do not cause any degeneration. Hence, these results suggest that $V_t$ shift after PBS is the consequence of the charge/discharge process in pre-existing high-k bulk traps.

Figure 2(a) shows $I_d$-$V_g$ with different $V_{high\ level}$ and fixed $V_{base\ level}$ from a fast I-V double sweep measurement with 30 mV drain voltage. Clearly, reverse sweep $V_t$ ($V_{t,reverse\ sweep}$) is smaller than forward sweep $V_t$ ($V_{t,forward\ sweep}$). Furthermore, subthreshold swings are similar. Thus, electrons escape from pre-existing high-k bulk traps to the gate or substrate rather than from interface traps. With an increase in $V_{high\ level}$, forward sweep $V_t$ is invariable while reverse sweep $V_t$ becomes smaller, as well as $|\Delta V_{t,hysteresis}|$ increasing, as shown in the right and left insets of Fig. 2(b), respectively ($\Delta V_{t,hysteresis} = V_{t,reverse\ sweep} - V_{t,forward\ sweep}$). Therefore, the higher the $V_{high\ level}$, the more electrons escape from high-k bulk traps. Figure 2(b) shows the $I_g$-$V_g$ curve at 30 °C. Obviously, gate current is insignificant since the interlayer ($SiO_2$) is too thick to tunnel through, resulting in channel electrons being unable to inject into high-k bulk traps. For the same reason, electrons in high-k bulk traps also cannot escape to the substrate, leading to only one escape route, that

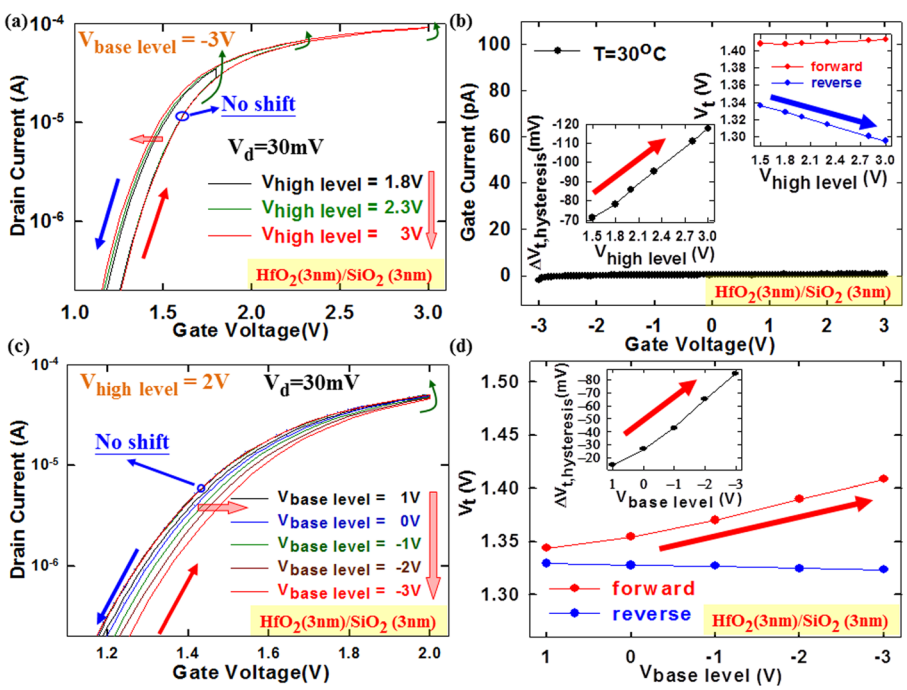


FIG. 2. (a) $I_d$-$V_g$ at different $V_{high\ level}$ and fixed $V_{base\ level}$ using fast I-V double sweep measurement with 30 mV drain voltage. (b) $I_g$-$V_g$ curve at 30 °C. The left inset shows $\Delta V_{t,hysteresis}$-$V_{high\ level}$. The right inset shows $V_t$-$V_{high\ level}$ in forward/reverse sweep. (c) $I_d$-$V_g$ with fixed $V_{high\ level}$ and different $V_{base\ level}$ using fast I-V double sweep measurement. (d) $V_t$-$V_{high\ level}$ in forward/reverse sweep. The inset shows $\Delta V_{t,hysteresis}$-$V_{base\ level}$.

of the metal gate. Figure 2(c) shows $I_d$-$V_g$ with fixed $V_{high\ level}$ and different $V_{base\ level}$ performed by fast I-V double sweep measurement. Forward sweep $V_t$ is larger than reverse sweep $V_t$, and subthreshold swings are similar. In addition, with a decrease in $V_{base\ level}$, reverse sweep $V_t$ remains the same while forward sweep $V_t$ becomes larger, and $|\Delta V_{t,hysteresis}|$ increases, as shown in Fig. 2(d) and its inset, respectively. Thus, the lower $V_{base\ level}$, the more electrons inject into high-k bulk traps. Moreover, only one inject source, the metal gate, offers electrons injecting into high-k bulk traps in $V_{base\ level}$ due to the insignificant gate current.

Combining the results above with a previous paper investigating trap energy level distribution in $HfO_2$, which are 0.5 eV, 1 eV, 1.5 eV, 2 eV below conduction band,[17] the energy band diagram of the model for charge/discharge electrons from high-k bulk traps can be acquired, as shown in Fig. 3. Figures 3(a), 3(c), 3(b), and 3(d) show energy band diagrams assuming $V_{base\ level} = -3$ V, 0 V and $V_{high\ level} = 2$ V, 3 V, respectively. Fixed $V_{base\ level}$ and varied $V_{high\ level}$ are shown in Figs. 3(a), 3(b), and 3(d). When $V_{base\ level} = -3$ V, electrons injecting from metal gate to high-k bulk traps of 1.5 eV and 2 eV energy level attain a steady state, resulting in an invariable forward sweep $V_t$. Subsequently, a comparison of Figs. 3(b) and 3(d) indicates that the higher $V_{high\ level}$, the more electrons escape from bulk traps, leading to a decrease in reverse sweep $V_t$. For the same reason, varied $V_{base\ level}$ and fixed $V_{high\ level}$ are shown in Figs. 3(a), 3(c), and 3(d). When $V_{high\ level} = 3$ V, electrons escaping from high-k bulk traps of 1.5 eV and 2 eV energy level to the metal gate attain a steady state, causing no change in reverse sweep $V_t$. At this moment when $V_{high\ level} = 3$ V, these bulk traps are empty. Next, electrons inject into bulk traps at $V_{base\ level}$. The lower $V_{base\ level}$, the more electrons inject to bulk traps, resulting in an increase in forward sweep $V_t$.

To further understand the transient charge and discharge phenomenon, fitting curves are necessary. The formula is expressed below. In a large-area device, discharge rate of carriers in the high-k bulk traps is given by[18–20]

$$Q(x,t) = qN_t(x,0)\exp\left[\frac{-t}{\tau(x)}\right], \tag{1}$$

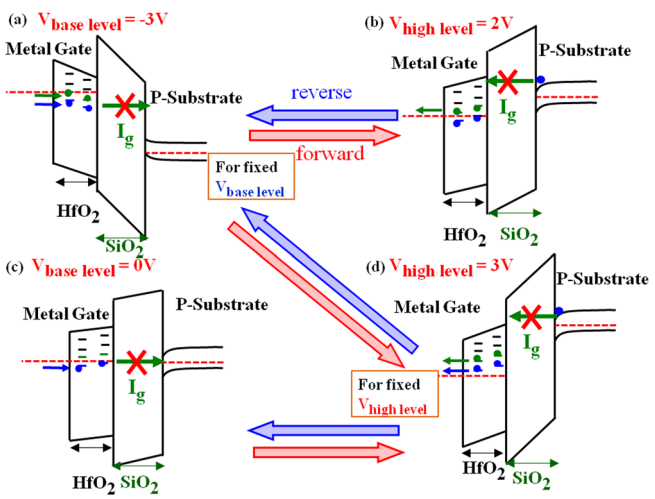


FIG. 3. The energy band diagram when (a) $V_{base\ level} = -3$ V, (b) $V_{high\ level} = 2$ V, (c) $V_{base\ level} = 0$ V, (b) $V_{high\ level} = 3$ V.

where $Q(x, t) = qN_t(x,t)$ and is the time-dependent trapped charge density, with $\tau$ (x) described in formula (3). $\Delta V_t$ induced by carrier discharge from high-k bulk traps can be expressed by

$$\Delta V_t(t) = -\int \frac{Q(x,t)}{C(x)}dx = -\int \frac{qN_t(x,0)}{\varepsilon_{HK}}x\left[1-\exp\left(\frac{-t}{\tau(x)}\right)\right]dx, \tag{2}$$

where C(x) is the corresponding capacitance for trapped charges located at x from the metal gate/high-k interface to traps and $\varepsilon_{HK}$ is permittivity for high-k dielectric. The relationship between tunneling time and distance can be approximated by[21,22]

$$\tau(x) = \tau_0 \exp(\alpha_k x), \quad \alpha_k = \frac{2\sqrt{2m^*_{HK}q\phi_B}}{\hbar}, \tag{3}$$

where $\tau_0$ is an electron tunneling characteristic time, $m_{HK}$ is carrier effective mass for high-k dielectric, and $q\phi_B$ is the effective tunneling barrier height. Then formula (3) is substituted into formula (2). Because the double exponential $\exp[-t/\tau(x)] = \exp[(-t/\tau_0)\ \exp(-\alpha_k x)]$ in the integrand changes abruptly from 0 to 1 around $x = (\alpha_k)^{-1}\ln(t/A)$, it can be approximated by a step function written as[20]

$$\exp\left[-\frac{t}{\tau_0}\exp(-\alpha_k x)\right]\begin{cases} 0 & for \quad x \le (\alpha_k)^{-1}\ln\left(\frac{t}{\tau_0}\right) \\ 1 & for \quad x \ge (\alpha_k)^{-1}\ln\left(\frac{t}{\tau_0}\right). \end{cases} \tag{4}$$

Assuming $N_t(x,o)$ uniform distribution and combining formulae (2), (3), (4), $\Delta V_t$ can be acquired by

$$\Delta V_t(t) \approx -\frac{q}{\varepsilon_{HK}}\int_0^{(\alpha_k)^{-1}\ln(\frac{t}{\tau_0})} N_t(x,0)xdx = -\frac{qN_t}{\varepsilon_{HK}}\frac{1}{2}\left[\frac{1}{\alpha_k}\ln\left(\frac{t}{\tau_0}\right)\right]^2. \tag{5}$$

With derivative of $\Delta V_t$ at t, the formula can be described by

$$\frac{d(\Delta V_t(t))}{dt} \approx -\frac{q}{\varepsilon_{HK}}\frac{1}{\alpha_k}\frac{1}{t}N_t[\frac{1}{\alpha_k}\ln(\frac{t}{\tau_0})] = -\frac{q}{\varepsilon_{HK}}\frac{1}{\alpha_k}\frac{1}{t}[x_{eff}N_t]. \tag{6}$$

Assuming that the process for electrons discharging from high-k bulk traps near the metal gate is too fast to be detected, the distance ($x_{eff}$) of high-k bulk traps discharging electrons contributing to $\Delta V_t$ is average. Variable $x_{eff}$ is the average distance from the metal gate/high-k interface to high-k bulk traps. Next, $\ln(dV_t(t)/dt)$ can be expressed by

$$\ln\left(\frac{d(\Delta V_t(t))}{dt}\right) \approx (-1)\ln(t) + \ln\left(\frac{q}{\varepsilon_{HK}}\frac{1}{\alpha_k}[x_{eff}N_t]\right). \tag{7}$$

Figures 4(a) and 4(b) show $\ln(dV_t(t)/dt)$-$\ln(t)$ fitted by formula (7) from Figs. 1(a) and 1(b), respectively. The stress/recovery

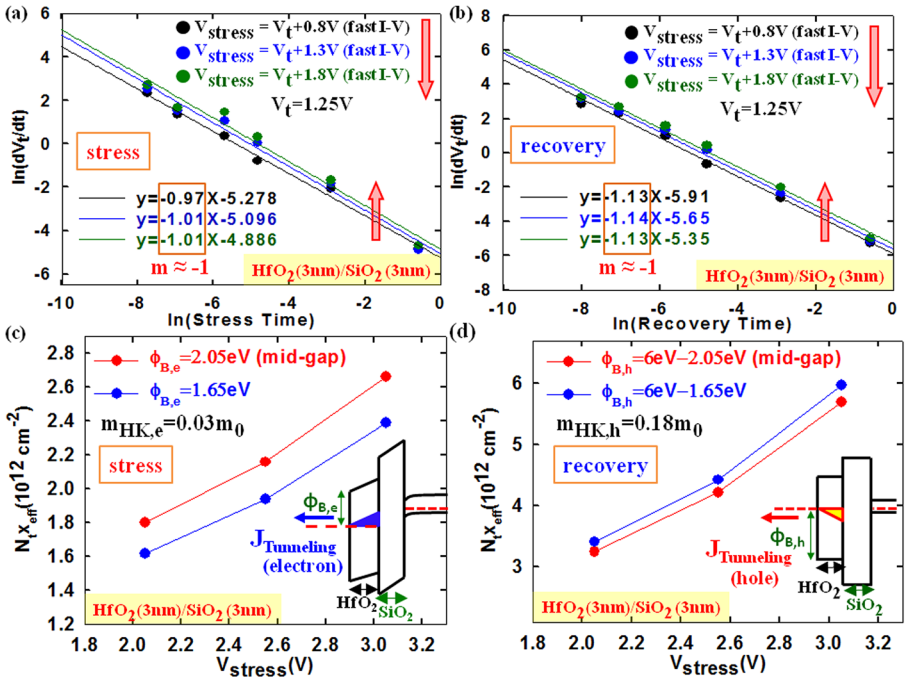


FIG. 4. (a) and (b) shows $\ln(dV_t(t)/dt)$ -ln(t) fitted by formula (7) from Figs. 1(a) and 1(b); (c) and (d) shows the $x_{eff}N$-$V_{stress}$ fitted curves from the intercept of Figs. 4(a) and 4(b) by formula (7).

time range is from $10^{-4}$s to $10^{-1}$s for fitting curves. Obviously, the slopes in Figs. 4(a) and 4(b) are about −1 for different stress voltages. This means that carriers are charged and discharged by high-k bulk traps via the tunneling mechanism. In addition, the energy levels of these high-k bulk traps are larger than 1 eV. Thus, the charge and discharge path through Frenkel-Poole mechanism can be ruled out. Figures 4(c) and 4(d) show the $x_{eff}N_t$-$V_{stress}$ fitted curves from the intercept of Figs. 4(a) and 4(b) by formula (7). The parameter for fitting curves of electrons escaping from the bulk traps under PBS in Fig. 4(c) is $m_{HK,e} = 0.03m_0$,[23,24] $\varepsilon_{HK} = 25\varepsilon_0$, and $\phi_{B,e} = \phi_{m,TiN}(4.2\,eV \sim 4.6\,eV) - \chi_{HfO2}(2.55\,eV) = 1.65\,eV$–$2.05\,eV$. $\phi_{m,TiN}$ is assumed to be from about mid-gap (4.6 eV) to minima of $\phi_{m,TiN}$ (4.2 eV) for n-channel MOSFET.[25] The parameter for fitting curves of holes escaping from the bulk traps when $V_{recovery} = 0$ V in Fig. 4(d) is $m_{HK,h} = 0.18m_0$,[26] $\varepsilon_{HK} = 25\varepsilon_0$, and $\phi_{B,h} = E_g(6\,eV) - \phi_{B,e}$. $\phi_{m,TiN}$ is the metal work function. $\chi_{HfO2}$ is the electron affinity in $HfO_2$. $\phi_{B,e}$ and $\phi_{B,h}$ are the effective tunneling barrier height for electron and hole, respectively. $m_{HK,e}$ and $m_{HK,h}$ are the high-k dielectric effective mass for electron and hole, respectively. Clearly, with an increase in $V_{stress}$, $x_{eff}N_t$ increases. In other words, the amount of carriers charged and discharged by bulk traps increases. This result conforms to the observations above. Furthermore, the amount of carriers is about $1 \times 10^{12}cm^{-2}$–$6 \times 10^{12}\,cm^{-2}$. According to previous letters,[27–29] this is reasonable. In addition, Figs. 4(c) and 4(d) indicate that with a rise in $\phi_{B,e}$, $\phi_{B,h}$,and $m_{HK}$, the amount of carriers contributing to $\Delta V_t$ increases. Therefore, the more time for carriers to escape from high-k dielectric, the more carriers can be detected in $\Delta V_t$.

Fig. 5(a) shows $I_d$-$V_g$ curves with different $V_{high\ level}$ using fast I-V double sweep measurement for the $HfO_2$(3 nm)/$SiO_2$(1 nm) device (standard performance device) when $V_{base\ level} = 0$ V. Obviously, with an increase in $V_{high\ level}$, forward sweep $V_t$ remains the same while reverse sweep $V_t$ becomes larger, and $\Delta V_{t,hysteresis}$ increases, as shown in Fig. 5(a) and its inset, respectively. This is because channel electrons inject into high-k bulk traps, as shown in previous letters.[30,31] Fig. 5(b) shows a comparison of $\Delta V_{t,hysteresis}$ − ($t_{rising\ time} = t_{falling\ time}$) for different devices with a constant electric field ($V_{base\ level} = V_{FB} - E_1EOT$, $V_{high\ level} = V_{FB} + \psi_s + E_2EOT$). $t_{rising\ time}$ and $t_{falling\ time}$ are rising time and falling time, respectively. $V_{FB}$ is the flat band voltage. EOT is the equivalent oxide thickness. $E_1$ and $E_2$ are electric fields. $\psi_s$ is surface potential at $V_t$. The $\Delta V_{t,hysteresis}$ is insignificant in the $SiO_2$(3 nm) device as the result of there being no charge/ discharge effect. The $\Delta V_{t,hysteresis}$ is negative in value in the $HfO_2$(3 nm)/$SiO_2$(3 nm) device due to electrons escaping

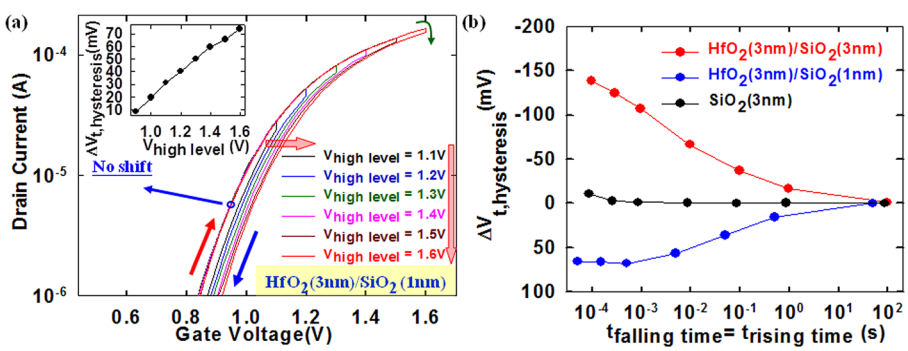


FIG. 5. (a) $I_d$-$V_g$ for different $V_{high\ level}$ and fixed $V_{base\ level}$ from fast I-V double sweep measurement in the $HfO_2$(3 nm) /$SiO_2$(1 nm) device. The inset shows $\Delta V_{t,hysteresis}$ − $V_{high\ level}$. (b) $\Delta V_{t,hysteresis}$ − ($t_{rising\ time} = t_{falling\ time}$) in a comparison of different devices with constant electric field.

from bulk traps to the metal gate, as mentioned previously. On the contrary, $\Delta V_{t,hysteresis}$ is positive in the $HfO_2$(3 nm) /$SiO_2$(1 nm) device owing to channel electrons injecting to bulk traps. Moreover, with an increase in $t_{rising\ time} = t_{falling\ time}$, $|\Delta V_{t,hysteresis}|$ becomes smaller until it disappears for all devices. In other words, $\Delta V_{t,hysteresis}$ is insignificant in conventional (slow) measurement as a consequence of $\Delta V_t$ almost wholly recovering during the measurement, as shown in Fig. 1(c).

In summary, $V_t$ shifts abnormally in the negative direction after PBS while using fast I-V measurement due to the electrons' reversible charge/discharge effect in pre-existing high-k bulk traps. In addition, the direction of $V_t$ shift in I/O device is contrary to that in the standard performance device since electrons escape from high-k bulk traps to metal gate by the tunneling mechanism in I/O device rather than channel electrons injecting to bulk traps, owing to the large interlayer thickness. According to these results, the charge/discharge effect is reduced with a decrease in pre-existing high-k bulk traps. In previous literature,[32,33] the method of Zr doping in $HfO_2$ dielectric efficiently reduced high-k bulk traps in standard performance devices. For this the same reason, the abnormal $V_t$ shift of I/O device performed by fast I-V measurement can be ameliorated by this method.

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