in air under a current density of 1.5 A/cm^2. This polarization value is less than one-tenth the value of conventional $La(Sr)MnO_3$ cathode.

This cathode shows the following reaction characteristics:

1. The interfacial conductivity has the first or higher degree of the oxygen partial pressure dependence.
2. The interfacial capacitance is very large (*e.g.*, 35 F/cm^2 in the oxygen), and has roughly linear dependence on the oxygen partial pressure.

These experimental results confirm that the change in the oxygen nonstoichiometry of the bulk near the surface makes a great contribution to the electrode reaction. However, an understanding of the entire reaction mechanism awaits further investigation.

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REFERENCES

1. K. Hirose, in *Proceedings of 2nd International Symposium on SOFC*, p. 1 (1991).
2. S. C. Singhal, *ibid.*, 25 (1991).
3. J. P. P. Huijsmans, F. H. van Heuveln, J. P. de Jong, and D. Bos, in *Proceedings of the International Fuel Cell Conference*, p. 353, *Jpn. J. Appl. Phys.* (1992).
4. O. Yamamoto, Y. Takeda, R. Kanno, Y. Tomida, *Nihon Kagakukaishi*, **8**, 1324 (1988).
5. U. B. Pal and S. C. Singhal, *This Journal*, **137**, 2937 (1990).
6. A. O. Isenberg, *Solid State Ionics*, **3/4**, 4312 (1981).
7. M. F. Carolan and J. M. Micheals, *ibid.*, **37**, 189 (1990).
8. N. J. Maskalick, in *Proceedings of 1st International Symposium on SOFC*, p. 279, *Jpn. J. Appl. Phys.*, (1989).
9. H. Sasaki, M. Suzuki, S. Otoshi, A. Kajimura, and M. Ippommatsu, *This Journal*, **139**, L12 (1992).
10. H. Sasaki, C. Yagawa, S. Otoshi, M. Suzuki, and M. Ippommatsu, *J. Appl. Phys.*, **74**, 4608 (1993).
11. Y. Takeda, R. Kanno, M. Noda, Y. Tomida, and O. Yamamoto, *This Journal*, **134**, 2656 (1987).
12. J. Mizusaki, H. Tagawa, K. Tsuneyoshi, and A. Sawata, *ibid.*, **138**, 1867 (1991).
13. B. C. H. Steele, S. Carter, J. Kajda, I. Kontoulis, and J. A. Kikner, in *Proceedings of 2nd International Symposium on SOFC*, p. 517 (1991).
14. S. Otoshi, H. Sasaki, H. Ohnishi, M. Hase, K. Ishimaru, M. Ippommatsu, T. Higuchi, M. Miyayama, and H. Yanagida, *This Journal*, **138**, 1519 (1991).

Dielectrics Degradation of α-Si/Co/SiO_2/Si Structure during Furnace Annealing

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ABSTRACT

The dielectric properties, which are highlighted on electrical characteristics, of α-Si/Co/SiO_2/Si structure after thermal annealing have been studied. A one-step high temperature ($\geq$700°C) annealing process is found to deteriorate considerably the characteristics of the masking oxide. The tetraethylorthosilicate oxide needs a high-temperature preanneal prior to the self-aligned silicided (SALICIDE) process in order to prevent crack and pit formation and severe electrical degradation during silicidation annealing. A two-step annealing process with the first annealing performed at 550°C for 30 min has proved to be a trustworthy salicide process without affecting the dielectric properties of masking oxide.

Self-aligned silicided (Salicide) process has become a very popular silicide formation technique because of its simplicity and reproducibility.[1-4] The Salicide process needs no additional mask to define the silicide layer making it a much more attractive silicide formation process than the co-deposition method in ultralarge scale integrated (ULSI) technology. However, the processing temperature must be carefully chosen so that the metal can completely react with the underlying silicon substrate or polycrystalline silicon film without attacking the masking materials. The most commonly used masking materials are thermally grown oxide, tetraethylorthosilicate (TEOS) oxide, low pressure chemical vapor deposition (LPCVD) oxide, plasma enhanced chemical vapor deposition (PECVD) oxide, and LPCVD nitride. Interaction between the masking materials and metals must be thoroughly characterized. It has been reported that some metal may react with oxide at low temperatures. For example, titanium is well known to attack the masking oxide reducing its effective thickness and thus degrade the oxide breakdown field strength and increase the oxide leakage current.[5-8] As a result, extra leakage current produces superfluous power consumption and degrades the device characteristics. Another problem that may arise in the Salicide process is the lateral growth of silicide film.[9-11] Lateral growth of silicide at spacers may cause an unacceptably high leakage current between the polycide gate electrode and source/drain regions. One must pay special attention to the lateral growth problem of those silicides whose metals are the dominant moving species during the silicide formation.

Titanium and cobalt silicides are two of the most popular metal silicides for Salicide processes because of their low resistivity and high temperature stability.[12-16] Interaction between titanium and thermally grown oxide has been extensively studied using material analysis and electrical measurements. However, investigations on cobalt and oxide interaction are still deficient and concentrate only on material analysis.[6,17,18] In this work, we studied dielectric properties of the α-Si/Co/SiO_2/Si structure after various furnace annealings in N_2 ambient. Both one-step and two-step annealing processes were evaluated. The one-step annealing process was performed at a high temperature to transform metal into silicide and reduce resistivity of the silicide simultaneously. The two-step annealing process, on the other hand, was performed first at a low temperature to transform metal into silicide followed by a high temperature anneal to reduce resistivity of the silicide. As will be confirmed later, two-step annealing is necessary to prevent degradation of dielectric properties because metal contamination arises from the one-step annealing process.

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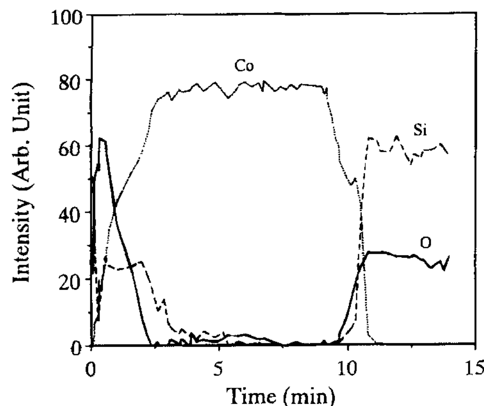

Fig. 1. AES depth profile of α-Si/Co (200 Å)/thermal oxide/Si structure annealed at 800°C for 30 min.

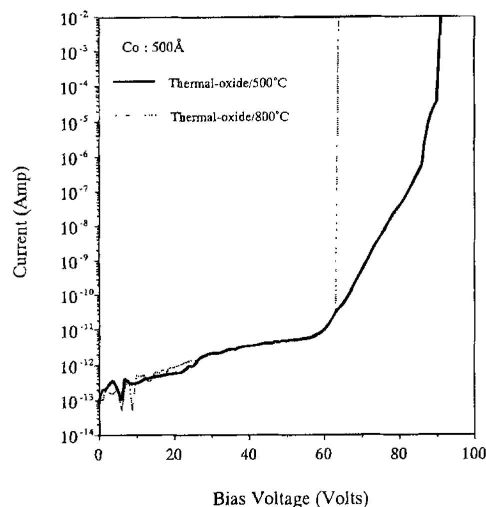

Fig. 2. Current-voltage characteristics for the α-Si/Co(500 Å)/thermal oxide/Si sample annealed at 500 and 800°C.

Experimental

Samples were fabricated on n-type <100>-oriented silicon wafers with 17 to 50 Ω-cm nominal resistivity. Silicon dioxide was prepared by two different methods to investigate their differences in their role of masking oxide. One group of samples had their oxide layer thermally grown by pyrogenic oxidation at 900°C. We refer to this oxide as thermal oxide hereafter. The thermal oxide was 900 Å in thickness, as determined by ellipsometric and capacitance-voltage (C-V) measurements. The other group of samples were deposited with chemically vapor deposited (CVD) tetraethylorthosilicate (TEOS) oxide. The chemically vapor deposited (CVD) oxide film was deposited in TEOS + O_3 ambient at 390°C to a thickness of 940 Å, as determined by ellipsometric measurement. We refer to this oxide as TEOS oxide hereafter. Some of the wafers with the TEOS oxide were further annealed at 800°C for 30 min for densification, and we refer to this oxide as TEOS (anneal) oxide hereafter. All the samples were then loaded into an E-beam evaporation system, and cobalt films of 40, 200, and 500 Å were deposited with a base pressure of less than 5×10^{-6} Torr. An α-Si film of 50 Å was subsequently deposited on top of each cobalt film without breaking the vacuum. The thin α-Si film was applied to serve as a passivation layer for the underlying cobalt to prevent the cobalt film from reacting with the residual oxygen in furnace during the subsequent thermal annealing.[9] The thermal annealing was performed in a flowing nitrogen furnace at temperatures ranging from 500 to 800°C with an annealing time of 30 min. After this annealing, the unreacted cobalt was removed by etching in 6 H_2O:1 H_2O_2:1 HCl (HCL) solution at 70 to 85°C for 5 min. Aluminum metallization and patterning were applied to the front side of the samples. The back side of the samples was also metallized by Al deposition.

The composition of the α-Si/Co/SiO_2/Si structure after thermal annealing was analyzed by Auger electron spectroscopy (AES). Scanning electron microscopy (SEM) was used to inspect the α-Si surface and the oxide surface after HCL solution etching. The breakdown field strength of the oxide was measured by a PC-controlled semiconductor parameter analyzer HP-4145B and the C-V characteristic was measured by a multifrequency LCR meter HP-4275.

Result and Discussions

AES analysis.—Cobalt is prone to oxidize in a conventional open-tube furnace; the thin α-Si capping layer is applied to circumvent this problem. Before investigating the effect of cobalt film on the underlying oxide during thermal annealing, it is necessary to make sure that the thin α-Si layer can effectively protect the cobalt film from reacting with the nitrogen and residual oxygen in the furnace during the annealing. Furthermore, we have to know if cobalt decomposes SiO_2 to form Co-O compound or other mixture. An example of AES depth profile for an 800°C annealed α-Si/Co (200 Å)/thermal oxide/Si sample is illustrated in Fig. 1. The α-Si capping layer successfully prevented the residual oxygen in the furnace from reacting

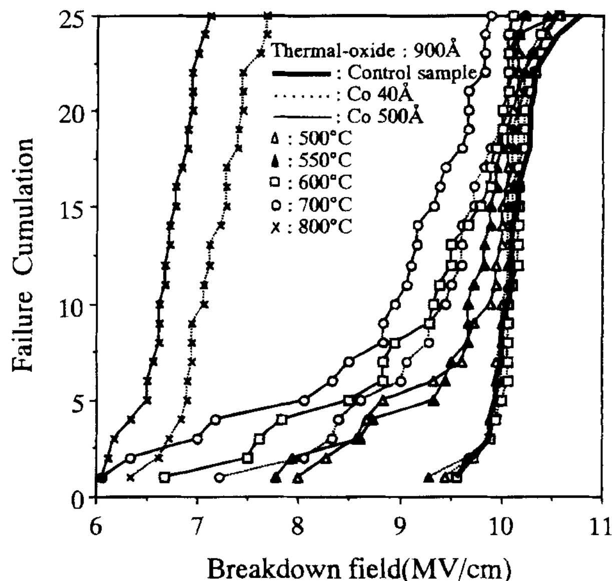

Fig. 3. Breakdown field for the α-Si/Co/thermal oxide/Si sample annealed at various temperatures. The thicknesses of cobalt films are 40 and 500 Å.

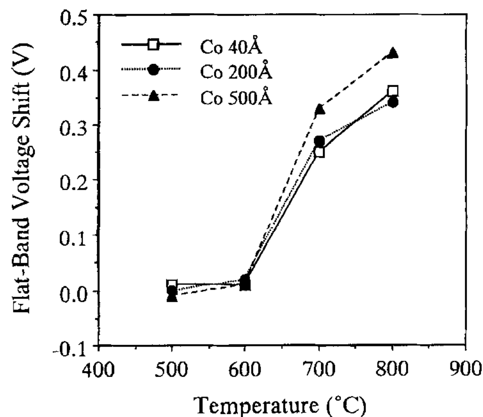

Fig. 4. Flatband voltage shift vs. annealing temperature for the α-Si/Co/thermal oxide/Si sample annealed with a one-step annealing process.

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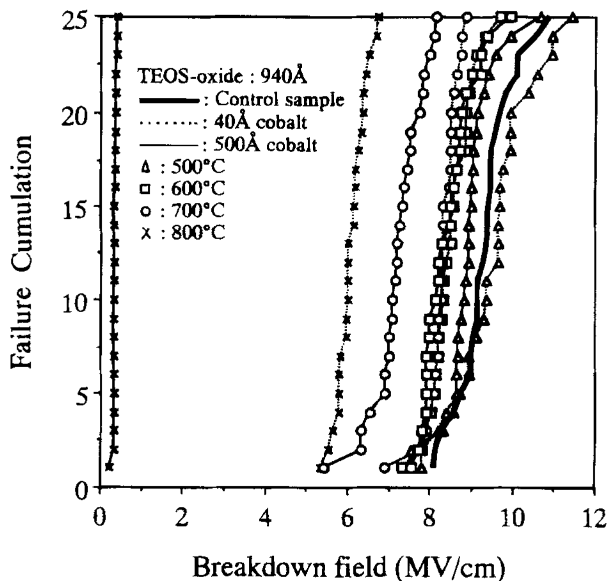

Fig. 5. Breakdown field for the α-Si/Co/TEOS oxide/Si sample annealed at various temperatures. The thicknesses of cobalt films are 40 and 500 Å.

with the underlying cobalt film during the annealing. No nitrogen signal was detected in the AES analysis. A mixture of Si-O-Co with high oxygen concentration is present at the surface, and a layer of pure cobalt is still present between the Si-O-Co mixture and the thermal oxide. A large part of the α-Si capping layer was consumed by the residual oxygen, so that only a small portion of the underlying cobalt was possible to react with the α-Si. The α-Si layer only slightly encroaches on the cobalt film, as shown in Fig. 1. Similar phenomenon was observed for samples annealed from 500 to 800°C. Because the cobalt film has no external nitrogen incorporation and may react with oxygen only in the surface layer, the effect of cobalt on the underlying oxide layer should be free from the influence of nitrogen and oxygen. The cobalt signal drops sharply at the Co/SiO_2 interface, as indicated by the AES depth profile; both the cobalt signal in the oxide and the oxygen signal in the cobalt near the Co/SiO_2 interface are beyond the AES detection limit. After removal of the unreacted cobalt by an HCL solution, the AES analysis on the SiO_2 layer still shows no detectable cobalt signal. Thus, it is reasonable to believe that cobalt does not react with oxide during annealing, which is consistent with the reports in the literature that cobalt does not react with oxide at temperatures lower than 900°C.[17,18]

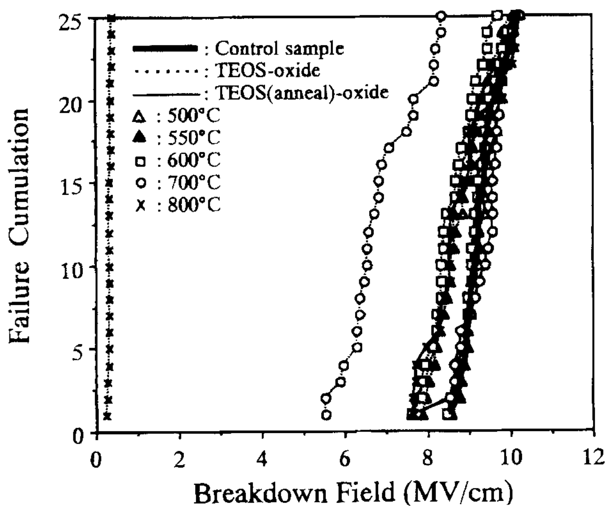

Fig. 6. Breakdown field for the α-Si/Co (200 Å)/TEOS oxide/Si and α-Si/Co (200 Å)/TEOS (anneal) oxide/Si samples annealed at various temperatures.

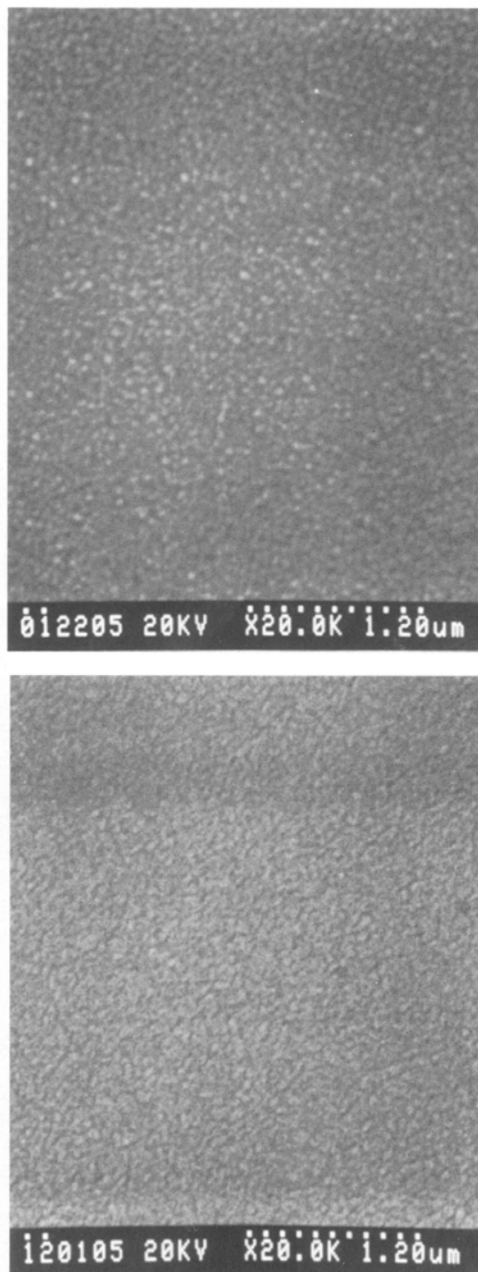

Fig. 7. SEM micrographs of (a, top) Co (surface) and (b, bottom) TEOS oxide surface for the α-Si/Co (40 Å)/TEOS oxide/Si sample annealed at 800°C.

Breakdown field of thermal oxide.—Electrical measurement may be the most effective way to examine the cobalt induced effects because microcontamination introduced into the oxide by the cobalt film is easily beyond the AES detection limit of 0.1 to 1%. Thus, the dielectric breakdown voltage and flatband voltage shift of the annealed α-Si/Co/SiO_2/Si structure were measured. The oxide breakdown voltage (V_{BD}) is defined as the voltage at which the current through the oxide is larger than 1 mA for 100 × 100 μm^2 size capacitor, and the breakdown field is equal to $(V_{BD}-V_{FB})/t_{ox}$, where V_{FB} is the flatband voltage, and t_{ox} is the oxide thickness. Figure 2 shows the current-voltage characteristics for the α-Si (50 Å)/Co (500 Å)/thermal oxide/Si sample annealed at 500 and 800°C. The higher temperature annealing apparently leads to the breakdown decrease of the thermal oxide. The breakdown field of the thermal-oxide after annealing at various temperatures is illustrated in Fig. 3. The cobalt films are 40 and 500 Å in

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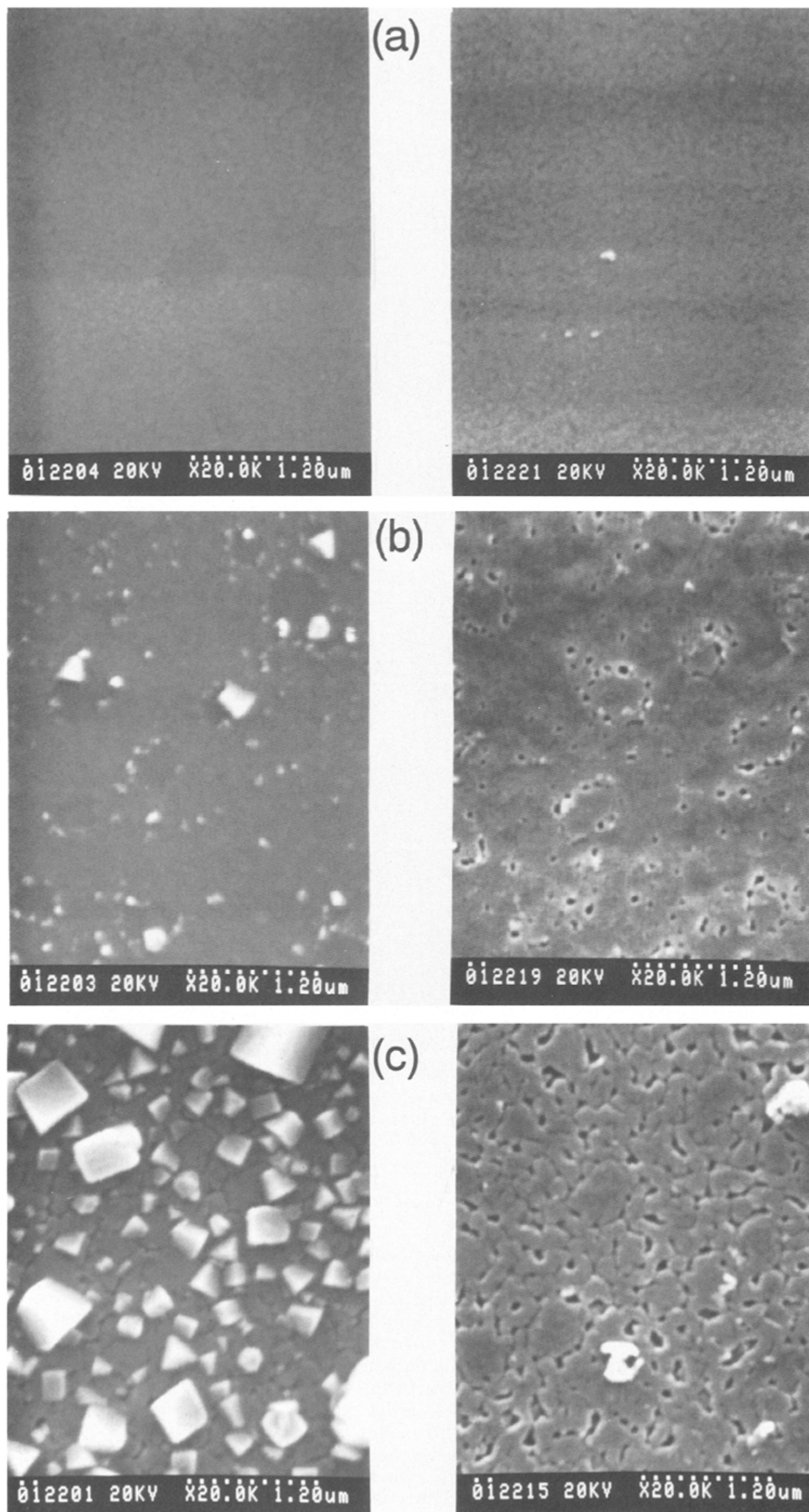

Fig. 8. SEM micrographs of Co (surface) (left) and TEOS oxide surface (right) for the α-Si/Co (500 Å)/TEOS oxide/Si sample annealed at (a) 600, (b) 700, and (c) 800°C.

thicknesses. For the samples with a 40 Å thickness of cobalt film, the breakdown field clearly remains unchanged for annealing at temperatures from 500 to 600°C. For the samples with a 500 Å thickness of cobalt film, however, the breakdown field degrades even after 500°C annealing. At the annealing temperatures of 700 and 800°C, the break-

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down field decreases with increasing annealing temperature irrespective of the cobalt film thickness. Furthermore, samples with a thicker cobalt film result in more pronounced breakdown characteristic degradation. The experimental results imply that the dielectric degradation mechanism is different for high temperature and low temperature annealing. At annealing temperatures lower than 600°C, samples with 40 Å cobalt film show no obvious degradation in breakdown field, while samples with 200 Å cobalt film reveal some degradation in breakdown characteristic, but the degree of degradation is not as serious as that of the samples with 500 Å cobalt film. In other words, the breakdown field decreases with increasing cobalt film thickness. Several factors may lead to this result: the process-induced stress, metal contamination, and pit formation. The process-induced stress may stem from a different thermal expansion coefficient between cobalt and thermal oxide, mechanical strain, and/or other unknown reasons. The thermal stress generated from the difference in the thermal expansion coefficient is independent of the cobalt film thickness.[14] Although a layer of the Si-O-Co mixture is present on the surface of the cobalt film, the thickness of the mixture layer is found to be relatively independent of the annealing temperature and the cobalt film thickness. The different thermal expansion should play a role in stress. But the observed result that thicker cobalt film leads to more serious electrical degradation implies that the mechanical strain and/or other unknown reasons may be the more important factors. Metal contamination is not observed at 600°C annealing, as is discussed in the following paragraph. As for the factor of possible pit formation, it may produce asperity at the Co/SiO_2 interface resulting in reduced effective oxide thickness and increased local electric field, which in turn decrease the breakdown field. We show that the pit formation is not observed in the thermal oxide within the resolution limit of SEM, and we infer that the possible pit formation does not play an important role in the decrease of breakdown field.

We have demonstrated in previous work[19] that the presence of the cobalt film introduces metal contamination into the silicon substrate as the annealing temperature exceeds 700°C. The cobalt contamination can be confirmed by s-pits delineation. It was observed that a large amount of s-pits scatter around in the silicon substrate as long as the α-Si/Co/SiO_2/Si structure was annealed at a temperature higher than 700°C. This observation was independent of the cobalt film thickness. Metal contamination in the SiO_2/Si system is well-known to cause degradation in dielectric properties.[20,21] For the case of 40 Å cobalt film, the annealing temperature that starts to cause degradation in the breakdown field is the same as the annealing temperature that starts to cause metal contamination to the silicon substrate. Thus, cobalt contamination is believed to be one of the major reasons for breakdown field decrease. The flatband voltage shift after annealing at an elevated temperature, as shown in Fig. 4, gives another example of metal contamination. Flatband voltage remains nearly unchanged when the annealing temperature is lower than 600°C. As the annealing temperature is raised to 700°C, a significant shift of flatband voltage is observed; a further change of flatband voltage occurs after the 800°C annealing. We also evaluated the two-step annealing process as follows: the samples were first annealed at 550°C for 30 min, and the unreacted cobalt was removed by the HCL solution followed by a second annealing at 800°C for 30 min. None of the samples showed further breakdown field decrease and flatband voltage shift. Thus, two-step annealing with the first annealing performed at a lower temperature is inevitable to ensure a reliable and practical formation process for cobalt silicide.

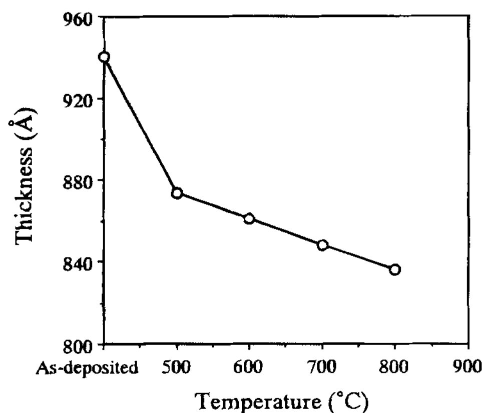

Fig. 9. TEOS oxide thickness *vs.* postdeposition annealing temperature.

Breakdown field of TEOS oxide and TEOS (anneal) oxide.—The breakdown field of the TEOS oxide after annealing at various temperatures is shown in Fig. 5. The cobalt films are 40 and 500 Å in thicknesses. The TEOS oxide has a slightly larger decrease of breakdown field compared with the thermal oxide. Due to some nonuniform property of the as-deposited TEOS oxide, the average breakdown field of the control sample varies between 9 and 10 MV/cm from wafer to wafer. Only the sample with 40 Å cobalt film annealed at 500°C was found to have a dielectric field strength comparable to that of the control sample. All other samples suffered from breakdown field degradation after annealing. The sample with 500 Å cobalt film annealed at 800°C has a very low breakdown field of about 0.3 MV/cm. From the above observations, we conclude that the as-deposited TEOS oxide is not suitable for serving as a spacer material in cobalt based Salicide process.

The TEOS (anneal) oxide, which had received a densification annealing at 800°C, exhibits a much better behavior of dielectric field strength. A comparison of the breakdown behavior of the TEOS (anneal) oxide and TEOS oxide for the samples with 200 Å cobalt film is illustrated in Fig. 6. The breakdown behavior of the TEOS (anneal) oxide is similar to that of the thermal oxide; the breakdown field only decreases about 1 MV/cm for the 800°C annealed sample. The breakdown field for the TEOS oxide, however, dramatically decreases to a very low value of about 0.3 MV/cm after an 800°C anneal. Thus, it is clear that the TEOS oxide needs a high temperature densification annealing before it is suitable for the Salicide process.

SEM inspection.—Surface morphology of the annealed α-Si/Co/oxide/Si samples was examined by SEM inspection. Figure 7a and b show, respectively, the SEM micrographs for the surface of the 800°C annealed α-Si/Co (40 Å)/TEOS oxide/Si sample and the surface of TEOS oxide after removal of the cobalt film by the HCL solution. The TEOS oxide looks nearly intact after the 800°C annealing. The surface of the α-Si/Co/TEOS oxide (or thermal oxide)/Si structure will be referred to as Co (surface) hereafter for the sake of convenience. A series of micrographs relevant to the α-Si/Co (500 Å)/TEOS oxide/Si structure annealed at various temperatures are shown in Fig. 8. For the 600°C annealed sample, Fig. 8a shows that both the surfaces of Co (surface) and TEOS oxide remain intact. After the 700°C annealing, protrusions and holes were observed on Co (surface), and small pits were observed on the TEOS oxide surface, as shown in Fig. 8b. After the 800°C annealing, the cobalt film became discontinuous and agglomerated into discrete islands of irregular shape with size ranging from several hundred to several thousand angstroms, as shown in Fig. 8c, and the underlying TEOS oxide revealed many cracks with many small pits scattered around. Careful comparison reveals that the locations of discrete islands correspond to the locations of small pits on the oxide surface. Since the 800°C annealed α-Si/Co (40 Å)/TEOS oxide/Si sample notably reveals neither crack nor pit, as shown in Fig. 7, the thickness of the cobalt film is apprarently a dominant factor for the crack and pit formation. The as-deposited TEOS oxide is actually a very loose oxide and the densification annealing shrinks the vol-

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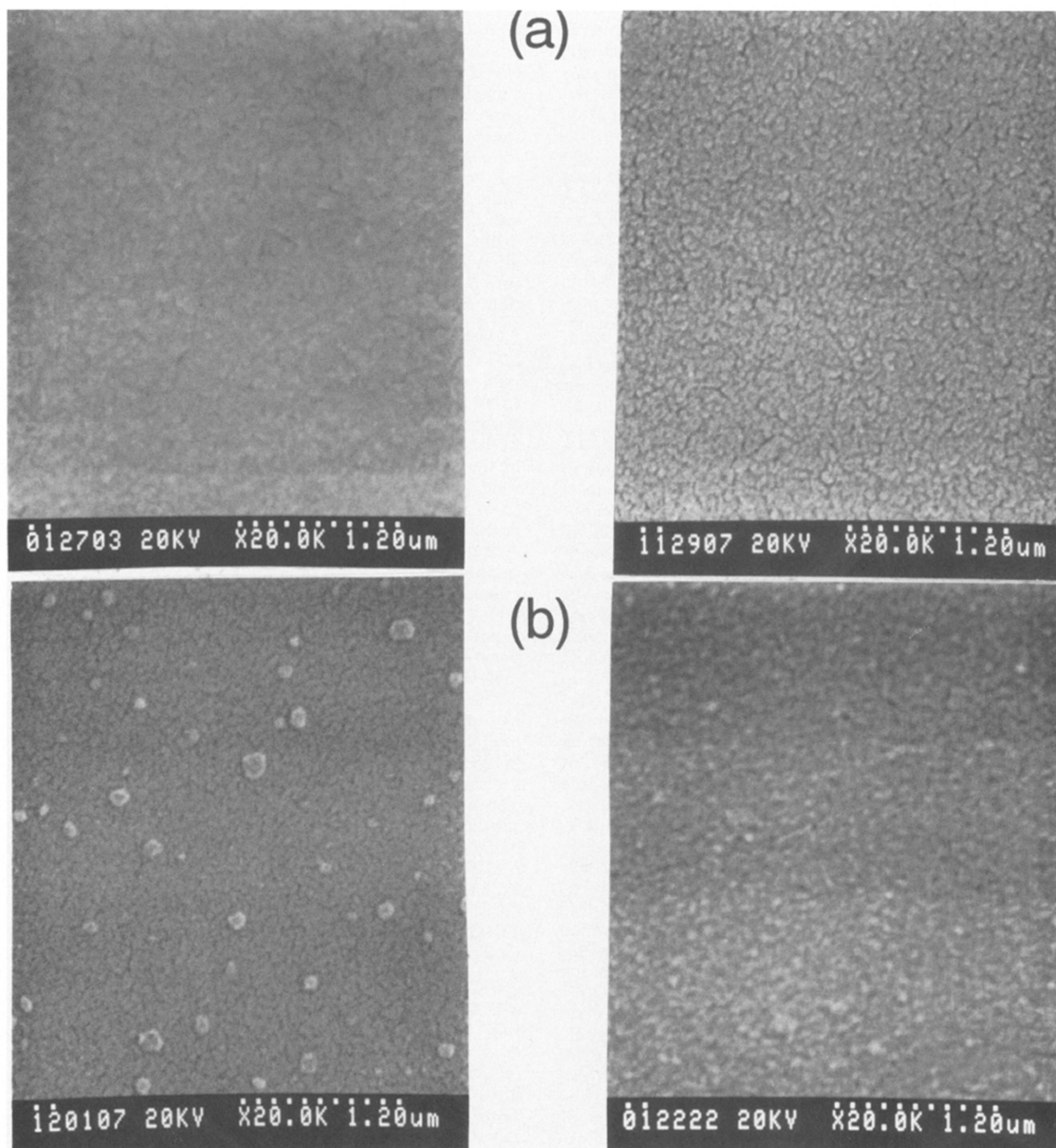

Fig. 10. SEM micrographs of Co (surface) (left) and oxide surface (right) for 800°C annealed (a) α-Si/Co (500 Å)/TEOS (anneal) oxide/Si and (b) α-Si/Co (500 Å)/thermal oxide/Si samples.

ume of the oxide and thus effectively reduces the oxide thickness. Figure 9 shows the thickness of the TEOS oxide as a function of densification annealing temperature. The oxide thickness is reduced by 7 and 12.1%, respectively, after 500 and 800°C annealing. However, the densification annealing does not affect the dielectric field strength. Because of the process-induced stress of cobalt and the significant volume shrinkage of TEOS oxide during heat-treatment, a large stress is generated between cobalt and TEOS oxide. Cobalt film consequently agglomerates into discrete islands and spikes into TEOS oxide leading to crack and pit formation in the oxide. For the sample with 40 Å cobalt film, no crack or pit is observed on the TEOS oxide because the process-induced stress, which is probably dominated by mechanical strain, originated from the thin cobalt film may be too small. Further experiments on the sample with 200 Å cobalt film confirmed that cracks and pits are generated on the TEOS oxide (not shown here). More evidence for the importance of volume shrinkage in forming the crack and pit is obtained as follows. Figures 10a and b show the SEM micrographs of the Co (surface) and oxide surface for the 800°C annealed α-Si/Co (500 Å)/TEOS (anneal) oxide/Si and α-Si/Co (500 Å)/thermal oxide/Si samples, respectively. Since both the TEOS (anneal) oxide and thermal oxide did not undergo volume shrinkage during annealing, they did not have the problem of crack and pit formation.

Degradation mechanisms.—Clearer insight into the mechanisms for breakdown field degradation can be obtained from the above discussions. The thermal oxide and TEOS (anneal) oxide do not have the problem of crack and pit formation up to the annealing temperature of 800°C, but the presence of the cobalt film introduces metal contami-

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nation into the oxide/Si structure. Thus, the breakdown field decrease was due mainly to metal contamination and process-induced stress. The process-induced stress is dependent on the thickness of cobalt film. Thicker cobalt film is observed to result in more breakdown field decrease. On the other hand, cracks and pits may be formed in the TEOS oxide depending on the cobalt film thickness. For the sample with 40 Å thickness of cobalt film, neither crack nor pit were observed, and the breakdown field decrease is due mainly to metal contamination. The process-induced stress, which is probably dominated by mechanical strain, is negligibly small for the thin cobalt film of 40 Å thickness. As the thickness of cobalt film exceeds 200 Å, crack and pit formation substantially reduces the effective thickness of the TEOS oxide. Thus, effective oxide thickness reduction, process-induced stress, and metal contamination all contribute to the severe degradation of dielectric properties. Figure 11 shows current-voltage characteristics of 800°C annealed α-Si/Co (500 Å)/TEOS oxide/Si and α-Si/Co (500 Å)/TEOS (anneal) oxide/Si samples; the degraded i-V characteristics for the α-Si/Co (500 Å)/TEOS oxide/Si sample shows an obvious rectifying nature but exhibits no Fowler-Nordheim tunneling region. Thus, we conjecture that pits penetrate the oxide layer, and the Al gate electrode makes direct contact with the silicon substrate. What we observed is not a real current-voltage characteristic of the oxide, but is the characteristic of localized Al/Si-contacted Schottky diodes. The one-step annealing process not only results in dielectric degradation, but also suffers from a silicide lateral growth problem.[9] The two-step annealing process can circumvent these problems and is believed to be a more practical and reliable processing technique for the Salicide scheme.

Conclusion

The dielectric degradation behavior of the α-Si/Co/SiO_2/Si structure with various masking oxides, including TEOS oxides, TEOS (anneal) oxides, and thermal oxides, have been investigated with respect to cobalt film thickness and Salicide processing temperature. TEOS oxide, which is often used as a spacer oxide, needs a high temperature densification annealing prior to the Salicide process in order to prevent undesirable effects resulting from volume shrinkage of the as-deposited oxide. The one-step annealing Salicide process with an annealing temperature higher than 700°C is detrimental to the performance of the masking oxide, including significant breakdown field degradation and thus is not a useful silicide formation technique. A two-step annealing Salicide process, with the first annealing performed at 550°C for 30 min, does not suffer from masking oxide degradation and has been proven to be necessary for a reliable Salicide technique.

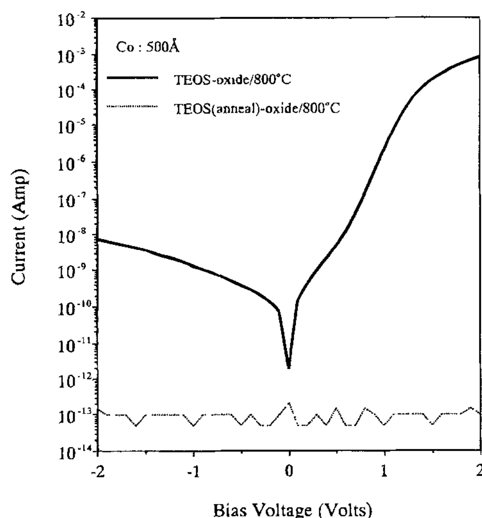

Fig. 11. Current-voltage characteristics for the α-Si/Co (500 Å)/TEOS (anneal) oxide/Si and α-Si/Co (500 Å)/TEOS oxide/Si samples annealed at 800°C.

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REFERENCES

1. S. P. Murarka, *J. Vac. Sci. Technol.*, **B4**, 1325 (1986).
2. H. Okabayashi, M. Morimoto, and E. Nagasawa, *IEEE Trans. Electron Devices*, **ED-31**, 1329 (1984).
3. M. Horiuchi and K. Yamaguchi, *ibid.*, **ED-33**, 260 (1986).
4. L. Van den Hove, R. Wolters, K. Maex, R. F. De Keersmaecker, and G. J. Declerck, *ibid.*, **ED-34**, 554 (1987).
5. C. Y. Ting, M. Wittmer, S. S. Iyer, and S. B. Brodsky, *This Journal*, **131**, 2934 (1984).
6. R. Pretorius, J. M. Harris, and M. A. Nicolet, *Solid State Electron.*, **21**, 667 (1978).
7. J. J. Sung and C. Y. Lu, *IEEE Electron Device Lett.*, **EDL-10**, 481 (1989).
8. G. J. P. Krooshof, F. H. P. M. Habraken, V. F. van der Weg, L. Van den Hove, K. Maex, and R. F. De Keermaecker, *J. Appl. Phys.*, **63**, 5110 (1988).
9. Y. S. Lou, C. Y. Wu, and H. C. Cheng, *Solid State Electron.*, **36**, 75 (1993).
10. F. M. Yang and M. C. Chen, *J. Vac. Sci. Technol.*, **B9**, 1497 (1991).
11. L. P. Hobb and K. Maex, *Appl. Surf. Sci.*, **53**, 321 (1991).
12. Y. S. Lou, C. Y. Wu, and H. C. Cheng, *IEEE Trans. Electron Devices*, **ED-39**, 1835 (1992).
13. Q. Wang, C. M. Osburn, and C. A. Canovai, *ibid.*, **ED-39**, 2486 (1992).
14. S. P. Murarka, *Silicides for VLSI Applications*, Academic Press, Inc., New York (1983).
15. F. J. Lai, J. Y. Sun, and S. H. Dhong, *IEEE Trans. Electron Devices*, **ED-33**, 345 (1986).
16. K. Shenai, *ibid.*, **ED-37**, 2207 (1990).
17. A. E. Morgan, E. K. Broadbent, M. Delfino, B. Coulman, and D. K. Sadana, *This Journal*, **134**, 925 (1987).
18. W. D. Chen, Y. D. Cui, and J. Tao, *J. Appl. Phys.*, **69**, 7612 (1991).
19. B. S. Chen and M. C. Chen, *Electron. Lett.*, **28**, 756 (1992).
20. T. H. DiStenfano, *J. Appl. Phys.*, **44**, 527 (1973).
21. H. Uchida, I. Aikawa, N. Hirashita, and T. Ajioka, *IEDM Tech. Dig.*, p. 405 (1990).

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