Layout Consideration and Circuit Solution to Prevent EOS Failure Induced by Latchup Test in a High-Voltage Integrated Circuits

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***Abstract*—This paper presented a practical industry case of electrical overstress (EOS) failure induced by the latchup test in high-voltage integrated circuits (ICs). By using proper layout modification and additional circuit, the unexpected EOS failure, which is caused by negative-current-triggered latchup test, can be successfully solved. The new design with proposed solutions has been verified in the 0.6-μm 40-V Bipolar CMOS DMOS (BCD) process to pass the test for at least 500-mA trigger current, which shows high negative-current-latch-up immunity without overstress damage, compared with the protection of only the guard ring. Such solutions can be adopted to implement high-voltage-applicable IC product to meet the industry requirement for the mass production of IC manufactures and applications.**

***Index Terms*—Electrical overstress (EOS), high-voltage CMOS, latchup, regulator.**

I. Introduction

LATCHUP is a common failure mechanism in CMOS ICs related to the occurrence of low impedance path between the supply and ground, which is triggered by overshooting/undershooting voltage or current perturbation to the parasitic PNPN structure. The trigger source can come from other place in the chip or the terminal of the PNPN structure which was distinguished to external or internal latchup, respectively [1]–[3]. When current perturbation is applied to the pin of ICs to examine the latchup immunity, it can be positive or negative direction during positive or negative current test (I-test). The specification and methodology of the examination have been specified in the JEDEC latchup test standard [4] and generally adopted by IC industry for production qualification.

As the supply voltage increases while the chip is expected to be conserved in HV IC's, the co-use of HV and LV devices becomes one of the trends for HV SOC designs. In the operation of HV environment, the high-voltage-tolerated pre-regulator is usually required to serve as the interface between HV and LV blocks and provides the necessary low supply voltage to the inner low-voltage circuits. However, certain node voltages in HV blocks as the HV pre-regulator may be abnormal since the high-voltage drift Nwell (HVNW) junctions in the HV devices are prone to the sink current brought by the parasitic bipolar transistor, especially during the negative I-test. Moreover, improper layout placement related with circuit structure may cause misconduction between HV supply and LV blocks. When voltage applied at the external supply is higher than the tolerance of LV transistors, it can even lead to ill function of ICs due to the electrical overstress (EOS) which may cause permanent damages [5], [6] at the metal connections or junctions of LV devices.

To increase the latchup immunity of the chips, guard ring protection is often used to reduce the substrate current which flows in the inner circuit blocks [7], [8]. Fabricate devices surrounding with insulating oxide layer (trench) or lightly doped epitaxial layers grown on heavily doped substrates can also eliminate the sink current by breaking the parasitic bipolar structures [9]–[11]. However, the protection of guard rings or extra layers increases the chip area or the fabrication cost. Even with the protection of guard rings, wider distance between the trigger source at I/O pin and the inner circuit or inner guard rings are still required [12], which may still be insufficient to the HV devices with deep HVNW junctions.

In this work, a practical industry case of EOS damage induced by the latchup negative I-test in a HV CMOS IC was described. The proper layout modification, the additional circuit solution, and the experimental latchup test have been verified in silicon to illustrate the improvement.

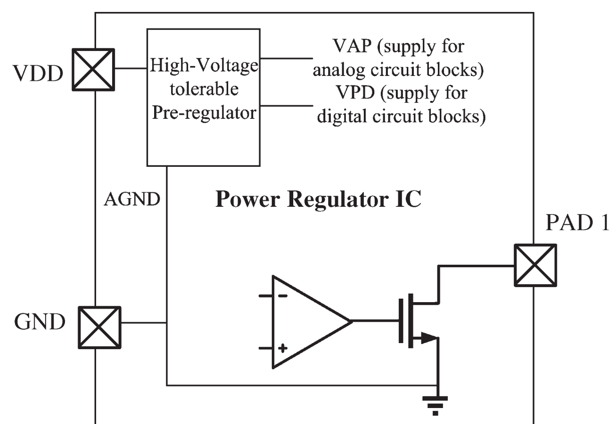

Fig. 1. Simplified circuit structure of a practical power regulator IC.

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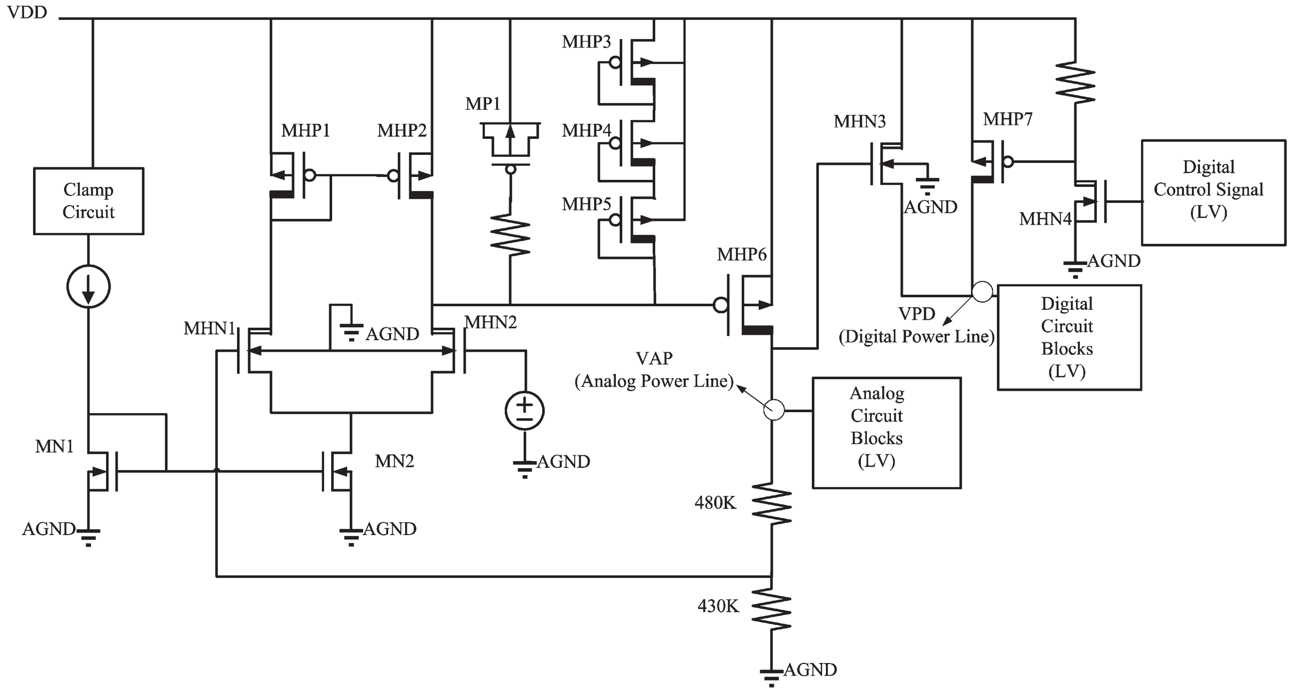

Fig. 2. Schematic of high-voltage-tolerable pre-regulator in this practical paper.

II. Negative I-Test Induced EOS Failure With Only Guard Ring Protection

To operate at HV environment but maintain the compression of chip area, a simplified structure for practical high-voltage-tolerable IC has circuit blocks shown as Fig. 1. The high-voltage-tolerable pre-regulator is composed of HV devices or both HV and LV devices, which is used to generate the necessary low supply voltage such as $\sim$3.3 V (at VAP node) or $\sim$2 V (at VPD node) to the analog or digital LV inner circuit, respectively. The high-voltage-tolerable pre-regulator in the practical work is shown in Fig. 2. MHN1 to MHN4 of the schematic in Fig. 2 are the HV NMOS transistors which can tolerate drain-to-source voltage difference ($|Vds|$) up to 40 V and MHP1 to MHP7 are the HV PMOS transistors with up to 40-V tolerance of source-to-drain voltage difference ($|Vsd|$) in a 40-V HV process. MN1, MN2, and MP1 are the 5-V LV devices used to provide the necessary bias current and the compensation for stability. The high-voltage-tolerable pre-regulator is composed of a two-stage amplifier with feedback connection as a typical LDO structure [13]. With the high-voltage-tolerable pre-regulator, the IC can operate normally under the desired HV supply such as 40 V. However, the practical packaged IC is still damaged during latchup test even guard ring protection had been placed between the HV I/O PAD and inner circuit blocks. After applying negative I-test with 100-mA sink current at some I/O PAD (as the PAD 1 shown in Fig. 1) with the high supply voltage (such as 30 V) over the tolerable range of LV devices, the practical work shows high abnormal current (up to mA) from the supply VDD to ground as depicted in Fig. 3(b) compared with the normal result (under 120 uA) before the test as shown in Fig. 3(a). The die photo of the damaged IC is shown in Fig. 4(a) and the damages apparently happened at the drain terminals of MHP6 and MHP7 which are the interfaces of high-voltage-tolerable pre-regulator to the LV digital blocks. Fig. 4(b) shows the partial layout presented with only HVNW and P+ implement layers that are nearby the PAD 1 in Fig. 4(a). The widths of the HVNW junctions in the guard ring and the transistors (including MHN1, MHN2, and MHN4) are 15.9 μm (W1) and 9.2 μm (W2), respectively, as shown in Fig. 4(b). The minimum distances between the edges from the HVNW junction at PAD 1 to the HVNW junctions in the guard ring, the transistor MHN1, and MHN4 are also shown in Fig. 4(b), which are 20 μm (D1), 118 μm (D2), and 154 μm (D3), respectively.

The reasons for the damages can be attributed to the short-through conductions from the supply voltage VDD to ground GND. Such paths are caused by the conductions of the transistor MHP6 and MHP7. The parasitic NPN structures from the I/O PAD to p-type substrate and internal HVNW layer of the HVNMOS transistors (such as the input pair of the amplifier) are shown as Fig. 5(a). With the consideration to avoid the negative impact from mismatch, HV NMOS MHN1 and MHN2 are arranged as MHN1–MHN2–MHN2–MHN1 placement in layout, and the two multipliers of MHN2 share the same drain area to make the die more compressive. The simplified cross-section view is shown in Fig. 5(b). When a large negative current is applied at the I/O PAD [as the PAD 1 depicted in Fig. 4(a)], the parasitic NPN structure attributed by the guard ring is triggered and expected to conduct the most current to the I/O PAD. However, there is still some current induced by another parasitic NPN structure. The node voltages such as the drain terminals of HV NMOS MHN1, 2, and 4 are pulled down due to the current flow induced by the sink current source, which is through the N+-HVNW junctions to the substrate as well as the I/O PAD to the source. The amount of induced current is correlated with the amount of sink current at the I/O PAD, the related location of the current source to the

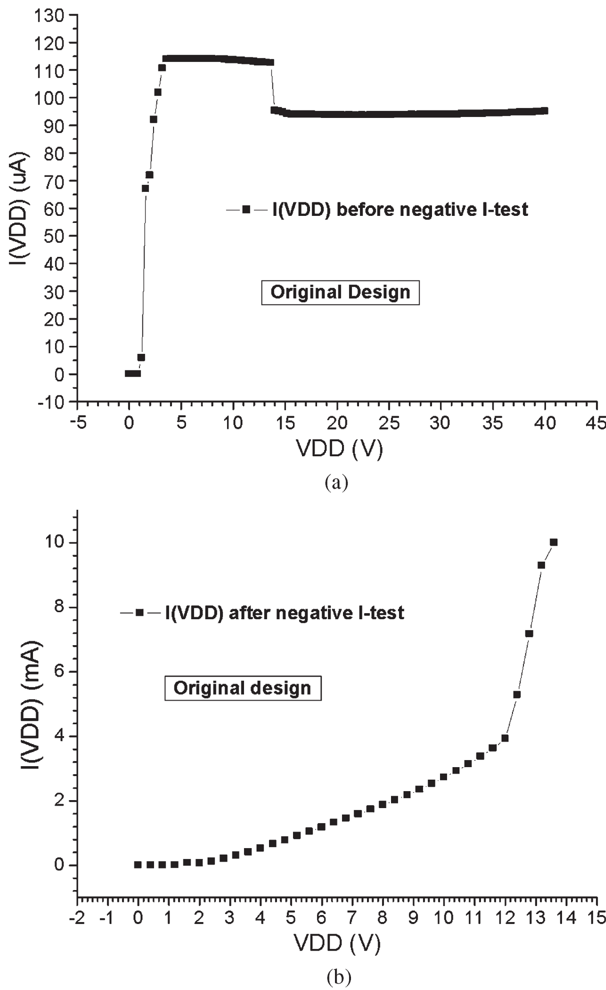

Fig. 3. Measured supply voltage and related current for the original design (without the modification) (a) before and (b) after the negative I-test applying at the PAD 1 with 100-mA sink current during the latchup test.

affected victim, and the junction area of the parasitic structure. Moreover, due to the layout structure shown in Fig. 5(a), the area of the HVNW junction connected to the drain terminal of MHN2 is double compared with that connected to the drain terminal of MHN1. Therefore, more current are sunk at the drain terminal of MHN1 and the voltage of gate terminal for MHP6 is pulled low which leads to the conduction of MHP6 to cause the overstress failure in the practical work as shown in Fig. 4(a).

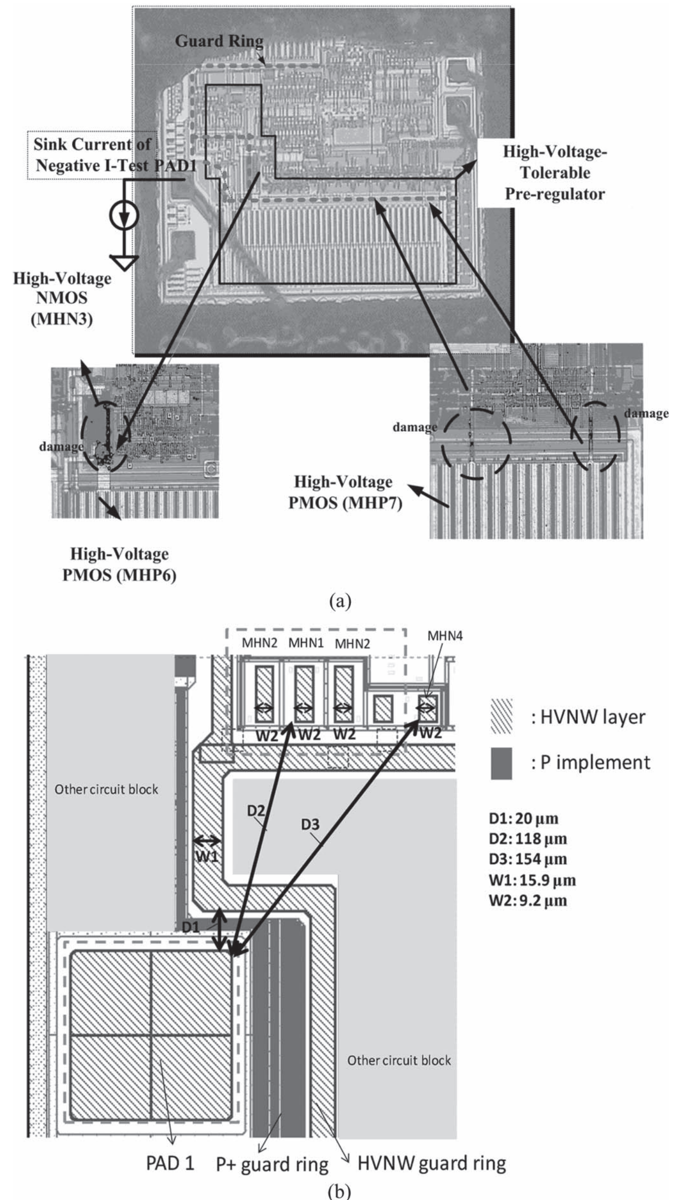

Fig. 4. (a) Die photo of the practical IC fabricated in 0.6-μm 40-V BCD process with negative I-test induced EOS damages. (dotted line) In guard ring connected to VDD. (b) The partial layout presented with only HVNW and P+ implement layers to show the widths and minimum distances of HVNW junctions from the PAD 1 to the guard ring, transistor MHN1, and MHN4.

III. Re-Design for Elimination of Latchup Test Induced EOS Failure

A. Modification of Layout Placement

To prevent such EOS problem in the above mentioned HV IC, the simplified improper layout placement for the input pair MHN1 and MHN2 of the original work is shown in Fig. 6(a). The proper modification with replacement in layout by metal re-connection is shown in Fig. 6(b). The locations of transistor MHN1 and MHN2 are exchanged so that the drain terminal of MHN1 is connected to double area of HVNW junction than that of MHN2. By such replacement, more current can be sunk at the node connected to the drain terminal of MHN1 than that of MHN2. Due to the current mirror structure, the sink current at the drain terminal of MHN1 drawn by the parasitic NPN is turned into the source current at the drain terminal of MHN2 through MHP1 to MHP2 which is also above double than the sink current. Thus, not only the sink current of the drain terminal for MHN2 can be compensated, but also the voltage at the gate terminal of MHP6 is pulled high to obstruct the conductive path caused by MHP6 from external supply VDD to inner supply VAP and VPD.

B. Modification With Additional Sensing and Compensation Circuit

Another method with circuit solution is proposed as shown in Fig. 7. The additional circuit is designed to compensate the

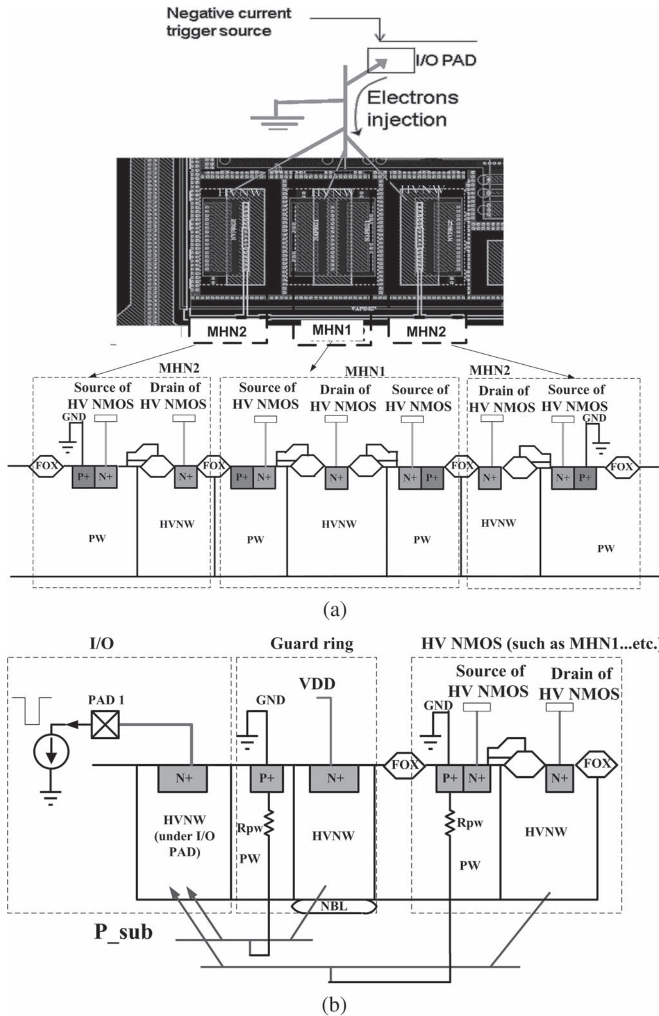

Fig. 5. (a) Parasitic NPN structures from I/O PAD to p-type substrate and internal HVNW. (b) Simplified cross-section view to show the parasitic NPN structure.

induced sink current from I/O PAD to the HVNW junction and also the drain terminal of HV NMOS transistors during latchup negative I-test. The proposed circuit contains a sensing part (implemented with HVNMOS MHN5 as well as a resistor) and a current mirror part (implemented with HVPMOS as MHP8 $\sim$ MHP10) to compensate the induced sink current. The HVNMOS MHN5 is gate grounded to turn off HVPMOS MHP8 $\sim$ 10 in the normal operation, but offers a sink current by the parasitic NPN structure when the large negative current at PAD 1 is sensed. When induced sink current is larger, the related sensing current is larger and the source to gate voltage of the diode connected HVPMOS MHP8 is also larger to produce more mirrored current at the HVPMOS MHP9 and MHP10. By connecting the drain terminals of the HVPMOS transistors as MHP9 and MHP10 to the nodes as the gate terminals of MHP6 and MHP7, the latchup-test-induced sink current can be compensated. Thus, the gate voltages of MHP6 and MHP7 were prevented from pulled low to trigger low impedance paths from external HV supply to inner LV supply. The sensing current can be used to produce a sink current through NMOS current mirror or a digital enable signal to launch protection mechanism to prevent the effect brought by the mistrigger of certain logic circuit under negative-current-triggered latchup test.

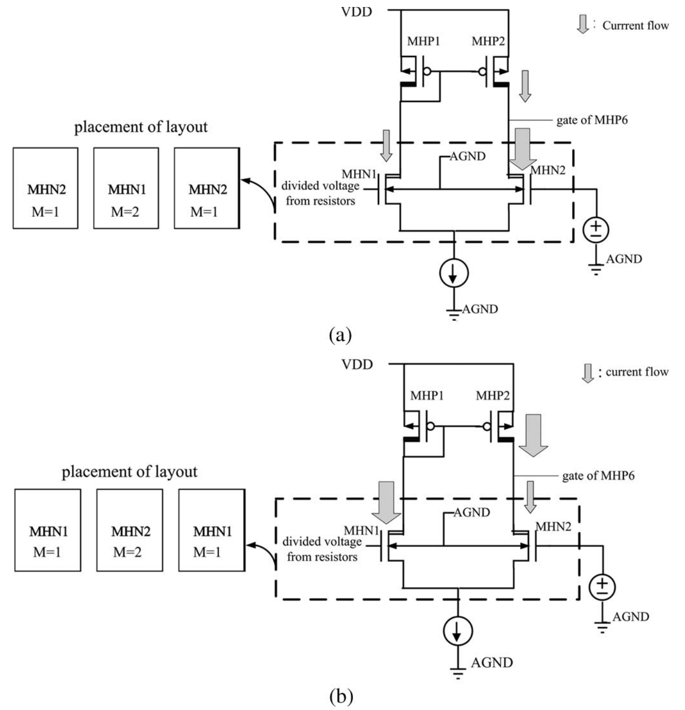

Fig. 6. (a) Improper layout placement for the input pair composed of MHN1and MHN2 in the original work. (b) Proper modification of the revised design with replacement in layout by metal re-connection.

C. Experimental Results

The proposed layout replacement and additional circuit solution have been verified with 0.6-μm 40-V BCD process in the revised version of the HV IC. Fig. 8 shows the measured results of certain signals in the original IC to depict the root cause of the EOS problem, as shown in Figs. 3(a) and 4(a). External voltage VDD is given as 6 V to perform the overstress situation without damaging the IC directly. When a 30-mA sink current is applied at the PAD 1, the inner supply voltage VAP is pulled up from the normal value ($\sim$3.3 V) to the voltage near VDD. When a larger sink current is used, the problem remains. The drain voltage of MHN1 is also shown in Fig. 8 to see the effected drain voltage of MHN1 with sink current through HVNW junction to HVNMOS devices. Since the inner supply voltage VAP from the pre-regulator is pulled up to $\sim$VDD after the negative I-test, the 5-V LV blocks or the metal line may have reliability problem with high voltage at VDD. It is even damaged directly when the applied voltage at VDD is higher than the breakdown voltage of LV junctions such as $\sim$12 V in the 0.6-μm 40-V BCD process. With the exchange of layout locations, the inner supply voltage VAP will be pulled low directly shown as Fig. 9 to prevent the damage due to the electrical overstress. The sink current at the PAD 1 is increased to examine if the solution is suitable to prevent the EOS problem for negative I-test with even large current over 500 mA.

The additional sensing and compensation circuits are also applied to the revised version to verify the results shown in Fig. 10. While current starts to be sunk at the PAD 1, the inner supply voltage (VAP) in Fig. 10 is also pulled down to prevent the overstress to the LV blocks. For the devices of the input

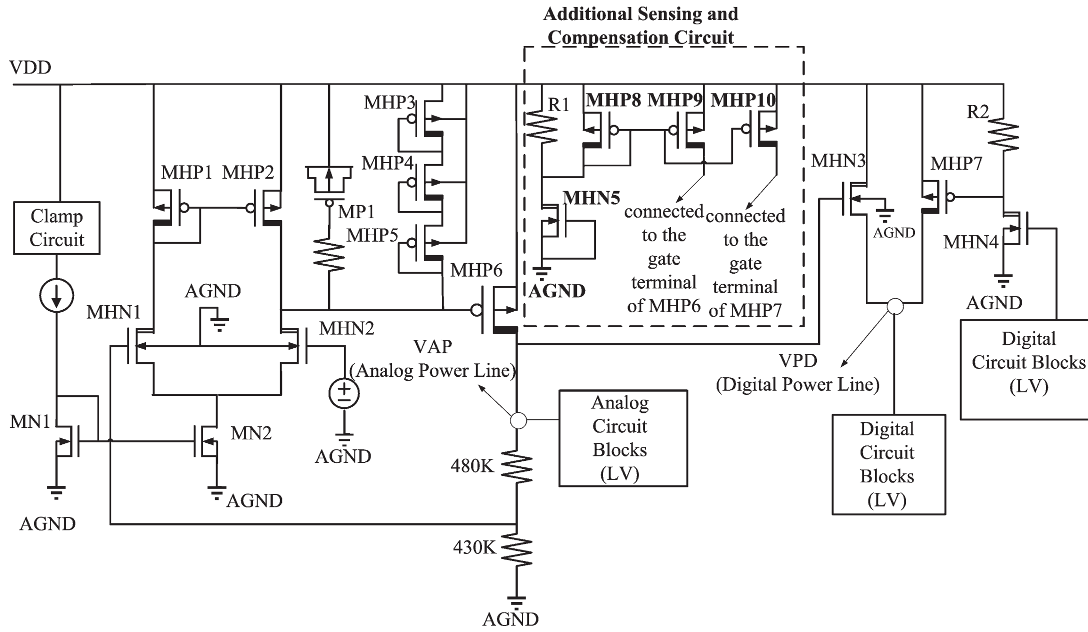

Fig. 7. Schematic of the revised design with new proposed sense and compensation circuit.

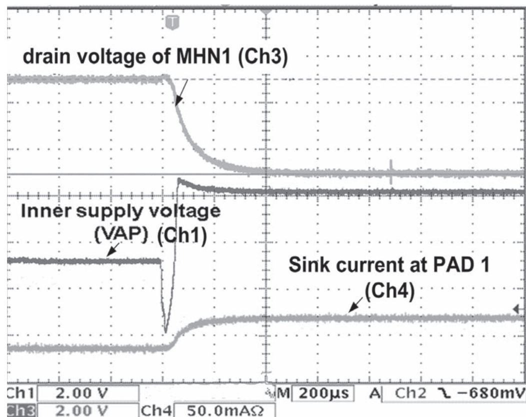

Fig. 8. Measured inner supply voltage when a 30-mA sink current is applied at the PAD 1 of the original IC without modification.

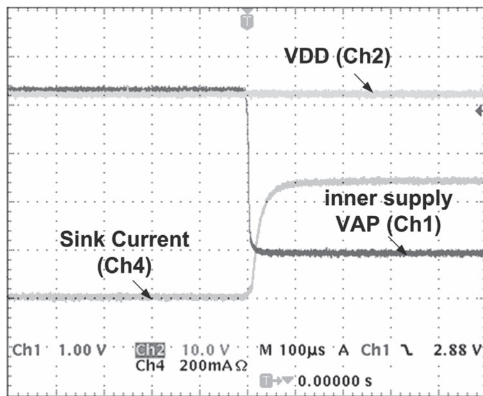

Fig. 9. Measured inner supply voltage with a 500-mA sink current at the PAD 1 of the revised design with proper layout at input pair of the pre-regulator.

pair, proper layout is already enough to eliminate the overstress problem happened at the output of the HV pre-regulator as VAP in Fig. 2. However, for the case of the damage happened at the node as VPD in Fig. 2, the solution of additional sensing and

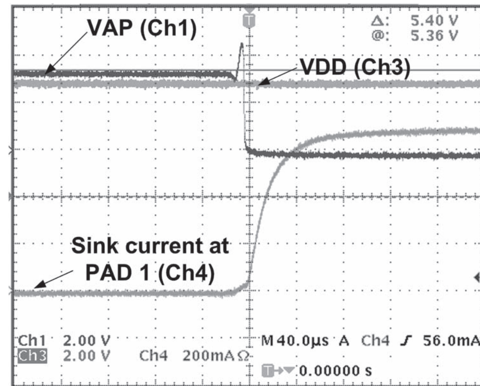

Fig. 10. Measured inner supply voltage with a 700-mA sink current at the PAD 1 of the revised design with proper layout at input pair of the pre-regulator.

compensation circuits are also required at the gate of MHP7 to prevent the conduction of MHP7 during negative I-test.

Fig. 11(a) shows the measured external supply current I(VDD) corresponding to the related supply voltage (VDD) for the revised design with both modifications before the negative I-test. Fig. 11(b) presents the measured results after 100-mA sink current is applied at VDD during negative I-test at PAD 1. As shown in these two figures, the revised design with the modifications has almost the same I–V curve before and after the test, whereas the original design without the modifications suffers large leakage at supply pin which causes the overstress damage. Therefore, both the analog and digital supply voltages of the LV circuits in the revised design can be prevented from the EOS problem to ensure qualified latch-up immunity.

IV. Conclusion

The proposed modifications to solve the EOS problem induced by the negative I-test have been verified successfully in 0.6-μm 40-V BCD process. With proper layout replacement and additional circuit, the inner power VAP and VPD are all

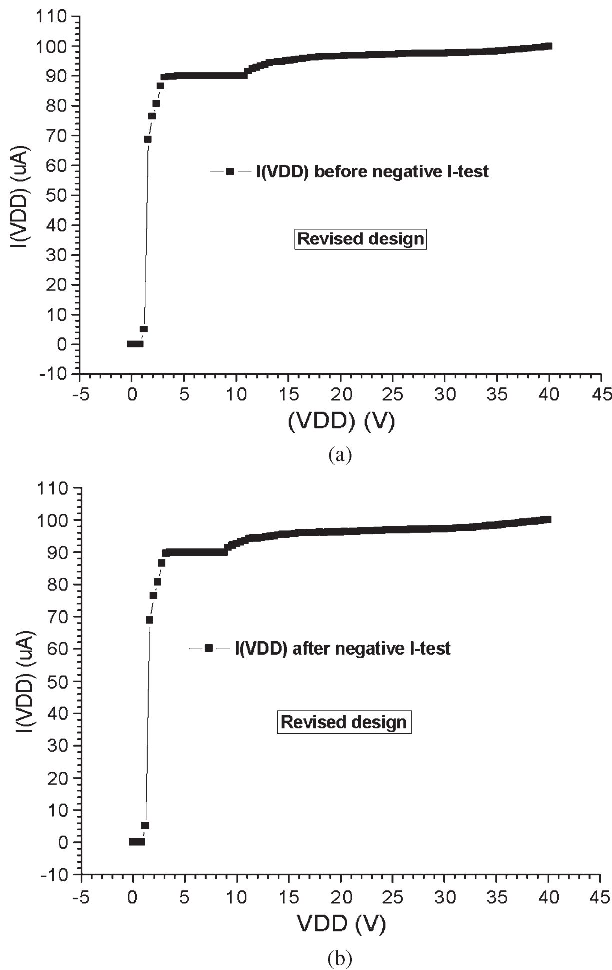

Fig. 11. Measured external supply current I(VDD) to the related supply voltage (VDD) for the revised design with the modifications (a) before and (b) after the negative I-test with 100-mA sink current at PAD 1.

prevented from conduction to the HV external supply VDD in the revised design. With the proposed solutions, the implemented chips pass at least 500-mA latchup test. The proposed solutions in this work are useful to improve the robustness of the circuit in HV environment and also remain qualified latchup immunity of HV circuits in SoC applications.

Acknowledgment

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