On the Design of Power-Rail ESD Clamp Circuits With Gate Leakage Consideration in Nanoscale CMOS Technology

Ming-Dou Ker, *Fellow, IEEE*, and Chih-Ting Yeh, *Member, IEEE*

***Abstract*—CMOS technology has been widely used to produce many integrated circuits. However, the thinner gate oxide in nanoscale CMOS technology seriously increases the difficulty of electrostatic discharge (ESD) protection design. The power-rail ESD clamp circuit has been the key circuit to perform the whole-chip ESD protection scheme. Some ESD detection circuits were developed to trigger on ESD devices across the power rails to quickly discharge ESD current away from the internal circuits. Therefore, on-chip ESD protection circuits must be designed with the consideration of standby leakage to minimize the power consumption and the possibility of malfunction to normal circuit operation. The design of power-rail ESD clamp circuits with low standby leakage current and high efficiency of layout area in nanoscale CMOS technology is reviewed in this paper. The comparisons among those power-rail ESD clamp circuits are also discussed.**

***Index Terms*—Electrostatic discharge (ESD), gate leakage, layout area, power-rail ESD clamp circuit.**

I. Introduction

ELECTROSTATIC discharge (ESD) phenomenon is a charge flow when two objects with different voltage potentials reach contact. ESD is the result of the charge balance between the two objects in a very short period of time. Such an ESD event can damage the integrated circuits (ICs). In order to protect the IC products with the required ESD specifications, such as 2 kV in human-body-model (HBM) [1] and 200 V in machine-model [2], whole-chip ESD protection scheme formed with the power-rail ESD clamp circuit had been widely used [3]. As shown in Fig. 1, the power-rail ESD clamp circuit is a vital element for ESD protection under different ESD stress modes. The ESD stress modes include VDD-to-VSS (or VSS-to-VDD) ESD stress between the rails; as well as the positive-to-VSS (PS) mode, negative-to-VSS mode, positive-to-VDD mode, and negative-to-VDD mode, from input/output (I/O) to VDD/VSS. Therefore, the power-rail ESD clamp circuit must provide low-impedance discharging path under ESD events but keep in OFF state with standby leakage current as low as possible under normal circuit operation conditions.

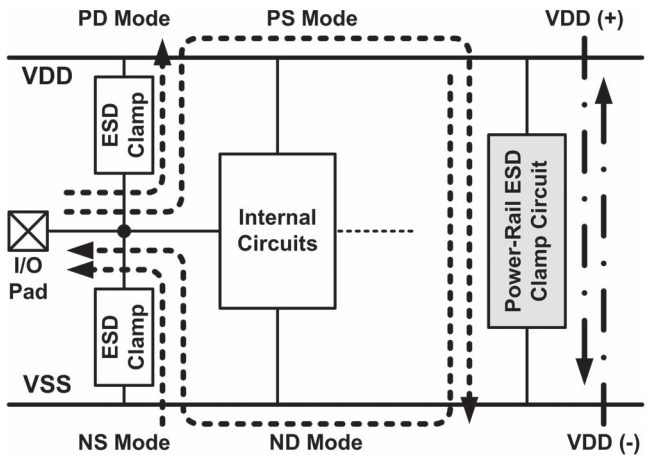

Fig. 1. Typical whole-chip ESD protection scheme with the power-rail ESD clamp circuit under different ESD stress conditions.

In advanced nanoscale CMOS technology, there are two commonly used processes provided from foundry for specific purpose. They are low-power (LP) and general-purpose (GP) processes. LP process is used for low-power product with a 1.2-V core design and 2.5- or 3.3-V I/O option. Because LP process is developed for low-power product, there is basically no serious gate leakage issue. Therefore, a large-sized MOSFET drawn in the layout style of big field-effect transistor (BigFET) is usually adopted as the ESD clamp device in the power-rail ESD clamp circuit.

GP process provides higher performance transistors for high-speed or high-frequency applications with 1-V core design and 2.5-V I/O option. In GP process, the thickness of gate oxide layer is thinner than that in LP process (or with a lower threshold voltage, i.e., Vth) to gain higher driving current. However, the thinner gate oxide seriously impacts on the ESD protection circuits due to the intolerable gate leakage and the lower breakdown voltage. A comparison of gate leakage issue on MOS capacitor $(\mathrm{W/L} = 1\ \mu\mathrm{m}/1\ \mu\mathrm{m})$ among different CMOS technologies is shown in Table I. In the 28-nm technology node, the structure of high-k/metal gate (HKMG) [4] has been adopted to reduce the gate leakage current issue and to continuously

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TABLE I
GATE LEAKAGE CURRENT OF MOS CAPACITOR IN GP PROCESSES

Generation	MOS Type	Effective Oxide Thickness	Gate Leakage Current at 1V (W/L = 1μm/1μm)
90nm (w/o HKMG)	nMOS	~ 2.3nm	~ 11nA
	pMOS	~ 2.5nm	~ 3nA
65nm (w/o HKMG)	nMOS	~ 2.0nm	~ 140nA
	pMOS	~ 2.2nm	~ 80nA
45nm (w/o HKMG)	nMOS	~ 1.9nm	~ 260nA
	pMOS	~ 2.1nm	~ 95nA
28nm (w/ HKMG)	nMOS	~ 1.35nm	~ 123nA
	pMOS	~ 1.4nm	~ 42nA

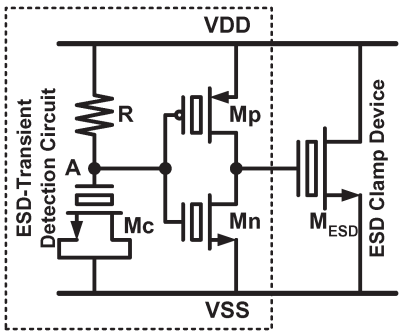

Fig. 2. Traditional RC-based power-rail ESD clamp circuit with thick gate oxide and large-sized nMOS transistor as ESD clamp device [3].

shrink the effective oxide thickness (EOT). However, the large-sized MOSFET in those advanced processes was obviously inadequate to meet the requirement of low standby leakage current. Hence, silicon-controlled rectifier (SCR) without poly-gate structure has been adopted as the main ESD clamp device in the power-rail ESD clamp circuits.

Recently, some circuit techniques have been developed to reduce the gate leakage current and layout area of the power-rail ESD clamp circuits. In this paper, those different circuit techniques are reviewed and discussed. The layout area, ESD robustness, and standby leakage current among those designs are compared.

II. PROCESS TECHNIQUES USED TO IMPLEMENT THE POWER-RAIL ESD CLAMP CIRCUIT

A. Traditional RC-Based Power-Rail ESD Clamp Circuit With Thick Gate Oxide

The traditional RC-based power-rail ESD clamp circuit was widely used to protect the core circuits [3], as shown in Fig. 2. Using the thick gate oxide can directly avoid the gate leakage issue. The RC-based ESD-transient detection circuit commands the ESD clamp nMOS transistor to turn on under ESD stress condition and to turn off under normal circuit operation condition. The turn-on time of the ESD clamp nMOS transistor can be adjusted by the RC-time constant of the RC-based ESD-transient detection circuit to meet the half-energy discharging time of the HBM ESD event [1]. To meet the aforementioned requirements, the RC-time constant of the RC-based ESD-transient detection circuit is typically designed about 0.1–1 μs to achieve the desired operations. Since the RC networks in the microsecond range are somehow large, it would occupy a significant fraction of the layout area.

B. Using the HKMG Structure

Gate dielectric has been one of the major challenges for technology scaling. With leakage and reliability constraints, high gate leakage of silicon dioxide has limited further scaling of gate dielectric thickness particularly for high performance applications. In addition, it is imperative to replace poly-Si with metal gate to eliminate poly-depletion. To continue EOT scaling, HKMG CMOS technology resumes gate dielectric scaling and is a solution to the gate leakage. However, the ideal HKMG technology needs some requirements of good performance integrity of higher k value, low leakage current, low threshold voltage, high mobility, and thermal stability for ion-implant doping activation [5]–[8].

C. Using the Parasitic Capacitance Between Metal Layer (MOM Capacitor)

MOM capacitors have been commonly used in IC design because the MOM capacitor has higher linearity, higher quality factor (Q), small temperature variation, and almost no leakage current [9]. When the dimensions keep shrinking in advanced CMOS technologies, the capacitance density of MOM is significantly increased and MOM capacitor will not occupy large chip area. Therefore, the MOM capacitor used in the ESD-transient detection circuit can solve the leakage issue.

The power-rail ESD clamp circuit with MOM capacitor is shown in Fig. 3 [10], which consists of the ESD-transient detection circuit with MOM capacitor and the p-type triggered SCR as the ESD clamp device. Without the thin gate-oxide structure, SCR has very low leakage current under normal circuit operating condition. In addition, SCR had been proven to have the highest ESD robustness under the smallest device size [11]. Moreover, SCR can be safely used without latchup danger in advanced CMOS technologies of low supply voltage.

Under normal power-on condition, the voltage level at node A can follow up the voltage level at VDD power line to keep Mp off. Simultaneously, the Mn is turned on because its gate terminal is connected to node A. As the result, no trigger current is injected into SCR and SCR can be kept off. Fig. 4 shows the

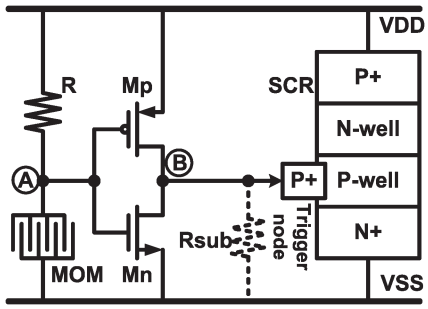

Fig. 3. Power-rail ESD clamp circuit with MOM capacitor [10].

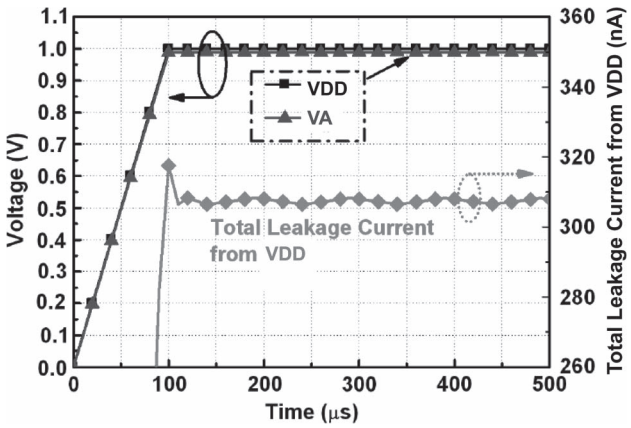

Fig. 4. Simulated transient waveforms of the ESD-transient detection circuit with MOM capacitor under normal power-on transition.

simulated transient waveforms with a rise time of 0.1 ms. With the power supply voltage of 1 V, the simulated overall leakage current of the power-rail ESD clamp circuit is only about 307 nA at 25 °C.

III. Circuit Techniques Used to Implement the Power-Rail ESD Clamp Circuit

A. Feedback-Enhanced Triggering Technique

The power-rail ESD clamp circuit with feedback-enhanced triggering was depicted in Fig. 5 [12]. A fast positive-going voltage pulse on the VDD power rail causes node A to instantaneously rise along with the VDD potential. The elevation of node A causes $\mathrm{M_{ESD}}$ to be turned on and ESD current can be discharged. Once the potential of node C has been raised to the voltage level above the threshold voltage of Mnf, Mnf begins to conduct. Current conduction in transistor Mnf further pulls the potential of node B toward ground, which further enhances current conduction in transistor Mp2, which then pulls the potential of node C closer to that of the VDD power line. This completes a feedback loop to latch $\mathrm{M_{ESD}}$ into a conductive state.

Once $\mathrm{M_{ESD}}$ has been latched into a conductive state, the time constant of the RC circuit is now free to time out. The duration of this time constant can be significantly shorter than the ESD event, which translates into an RC network with greatly reduced physical area. However, the transistors of the feedback loop and the ESD clamp device in this design need some modifications to reduce the gate leakage.

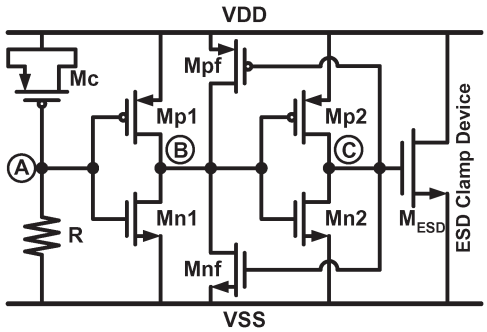

Fig. 5. Power-rail ESD clamp circuit with feedback-enhanced triggering and ESD clamp nMOS transistor [12].

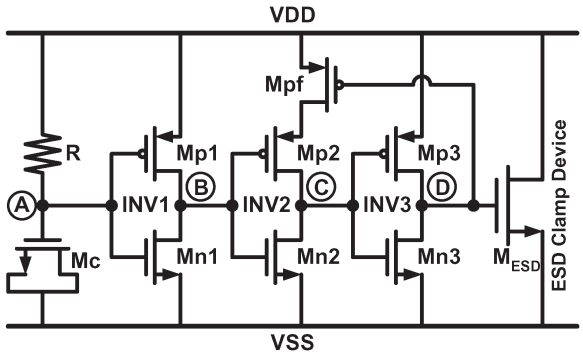

Fig. 6. Power-rail ESD clamp circuit with cascaded pMOS feedback technique and ESD clamp nMOS transistor [13].

B. Cascaded PMOS Feedback Technique

The power-rail ESD clamp circuit with cascaded pMOS feedback technique was shown in Fig. 6 [13]. This circuit uses a small capacitor in the RC timer, relative to the traditional RC-based design. One of the immediate advantages is that MOSFET-size rationing is not critical for this circuit. Of course, the cascaded pMOS should not be so small as to affect the switching speed of INV2 and subsequently INV3.

Upon initiation of a positive ESD event between VDD and VSS, the voltage at node A stays low for a time period set by the RC time constant. This low voltage at node A causes node C at 0 V. The feedback pMOS Mpf has no effect at this time because Mp2 is turned off. The low voltage at node C causes the voltage at node D to be pulled up to VDD. Thus, $\mathrm{M_{ESD}}$ is fully conducting within three inverter delays when the ESD stress is initiated. Once the voltage at node A rises above the switching threshold of INV1, Mn2 is turned off, and Mp2 is turned on. However, since the voltage at node D is VDD, Mpf is turned off, and node C remains in the low state. As long as the voltage at node C is less than the threshold voltage of Mn3, the gate voltage of $\mathrm{M_{ESD}}$ will not be perturbed and $\mathrm{M_{ESD}}$ stays in turned-on conduction beyond the time constant of the RC network. Similar to the design in Section III-A, all transistors in the ESD detection circuit and the ESD clamp device require more attention to reduce the gate leakage.

C. Reducing the Gate Area of the MOS Capacitor

A power-rail ESD clamp circuit with smaller capacitance that adopts the capacitance-coupling mechanism has been shown in

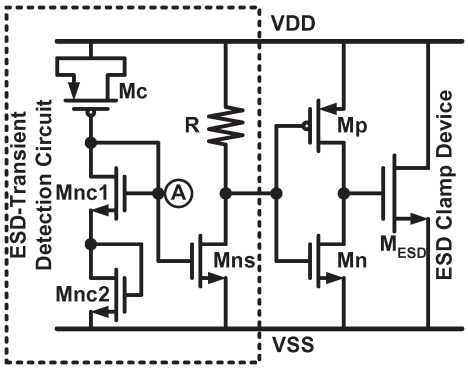

Fig. 7. Power-rail ESD clamp circuit with smaller capacitance in ESD-transient detection circuit [14].

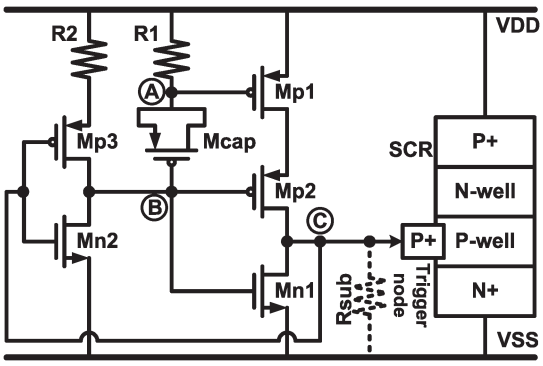

Fig. 8. Power-rail ESD clamp circuit with feedback-control inverter [16].

Fig. 7 [14]. The cascade nMOS transistors (Mnc1 and Mnc2) operated in the saturation region are used as a large resistor and combined with the smaller capacitor to construct a capacitance-coupling network. Under ESD stress condition, the potential of node A will be synchronously elevated toward a positive voltage potential by capacitance coupling of the smaller capacitor. Then, the gate terminal of the ESD clamp nMOS transistor will be promptly charged toward the positive voltage potential. Under normal circuit operation condition, the potential of node A will actually be kept at VSS through the high resistance path of the cascade nMOS transistors. Therefore, the ESD clamp nMOS transistor will be kept at the OFF state under normal circuit operation condition. For reducing the total standby leakage current of this design in nanoscale CMOS technology, the device sizes of inverter can be shrunk, and the ESD clamp device can be replaced by SCR.

D. Reducing the Voltage Drop Across the MOS Capacitor (I)

The equations of the gate-direct-tunneling current from BSIM4 MOSFET model [15] indicate that the leakage current through the MOS capacitor can be reduced by reducing the voltage across it. Based on this concept, the power-rail ESD clamp circuit with feedback-control inverter to overcome the gate leakage issue is shown in Fig. 8 [16]. In the ESD-transient detection circuit, the RC-based ESD-transient detection circuit and the feedback-control inverter are combined together, and the MOS capacitor Mcap is connected between nodes A and B. Because Mcap is not directly connected to VSS, no direct leakage path is conducted through Mcap to the ground under

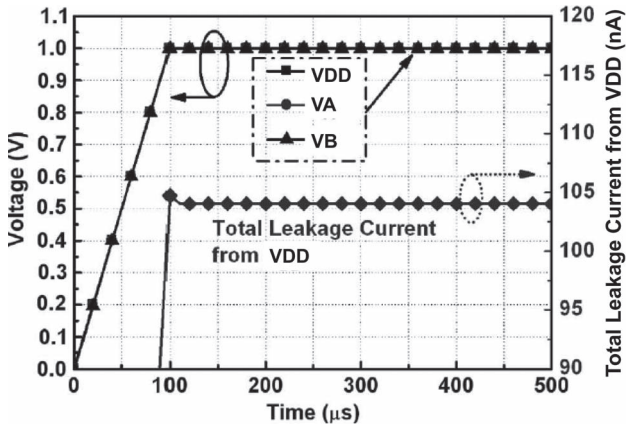

Fig. 9. Simulated transient waveforms on the node voltages in the ESD-transient detection circuit with feedback-control inverter under normal power-on transition.

normal circuit operating condition. Without the thin gate oxide, the SCR used as the main ESD clamp device is also free to the gate leakage issue as compared with a large-sized MOSFET.

With a slow rise time of the normal power-on transition, the voltage level at node A will be able to follow up the voltage level at VDD power line to keep Mp1 off. The parasitic p-substrate resistor Rsub in SCR can pull node C to VSS. Mp3 would be also turned on to drive node B to VDD. With the voltage of VDD at node B, Mp2 can be fully turned off. In addition, Mn1 is turned on because its gate terminal is connected to node B. Obviously, there is no voltage drop across Mcap, and no circuit leakage path exists in the ESD-transient detection circuit. Without a voltage drop across Mcap under normal circuit operating condition, Mcap can be realized with a large device size without suffering the leakage current. Since nodes A and B are charged to VDD, Mp1 and Mp2 can be fully turned off during the normal power-on transition. Therefore, no trigger current is injected into the SCR, and the SCR can be kept off under normal circuit operating condition.

Fig. 9 shows the simulated transient waveforms of the ESD-transient detection circuit under the normal power-on transition with a rise time of 0.1 ms. With the power supply voltage of 1 V, the overall simulated leakage current of the ESD-transient detection circuit is only about 104 nA at 25 °C.

E. Reducing the Voltage Drop Across the MOS Capacitor (II)

The power-rail ESD clamp circuit with the consideration of the gate current is shown in Fig. 10 [17]. The SCR device is used as the main ESD clamp device. Utilizing the gate current to bias the ESD-transient detection circuit and to reduce the voltage difference across the gates of the MOS capacitors, the gate leakage current through the MOS capacitor under the normal circuit operating condition can be further reduced. Therefore, the total leakage current resulted from the MOS capacitor in the ESD-transient detection circuit can be well controlled and minimized.

In the ESD-transient detection circuit, Mp1 is used to generate the triggering current into the trigger node of the SCR during the ESD stress event, but Mp1 is kept off under the normal circuit operating condition. The Mn is used to keep the voltage

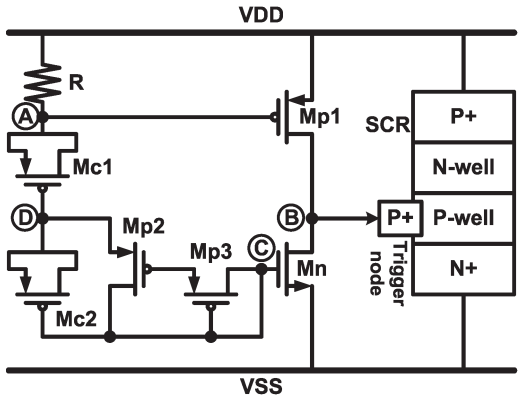

Fig. 10. Power-rail ESD clamp circuit with utilization of gate current [17].

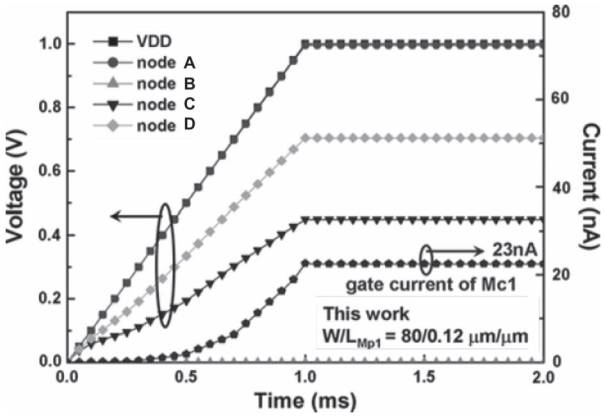

Fig. 11. Simulated voltage on the nodes and the gate current flow through the MOS capacitor Mc1 of the ESD-transient detection circuit with utilization of gate current under normal power-on transition.

level at the trigger node (node B in Fig. 10) at VSS; thus, the SCR is guaranteed to be turned off during the normal circuit operating condition. The RC time constant from R, Mc1, Mc2, and the parasitic gate capacitance of Mn is designed around the order of microsecond to distinguish ESD stress event from the normal power-on condition. The diode-connected Mp2 and Mp3 are acted as a start-up circuit with initial gate-to-bulk current from VDD into the ESD-transient detection circuit, and, in turn, to conduct some gate current of Mc1 to bias nodes C and D. After that, the voltage level at node D will be biased to reduce the voltage difference across Mc1 and to minimize the gate leakage current through the MOS capacitors.

Fig. 11 shows the simulated voltage waveforms on the nodes of the ESD-transient detection circuit and the gate current through the MOS capacitor Mc1 under the normal power-on condition with a rise time of 1 ms and VDD of 1 V (VSS of 0 V). The gate voltage of Mp1 is biased at 1 V through resistor R with a low gate current ($\sim$23 nA) of MOS capacitor Mc1, so that Mp1 can be kept off, and no trigger current is generated into the SCR device. In addition, node C is biased at 0.45 V to turn on Mn, which, in turn, keeps the trigger node of SCR grounded.

F. Capacitor-Less Design of Power-Rail ESD Clamp Circuit

The capacitor-less design of power-rail ESD clamp circuit is illustrated in Fig. 12 [18]. The power-rail ESD clamp circuit consists of the ESD-transient detection circuit with feedback

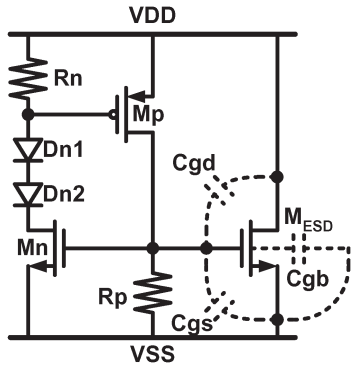

Fig. 12. Capacitor-less power-rail ESD clamp circuit with diode string in the ESD-transient detection circuit and ESD clamp nMOS transistor [18].

technique, which is realized by two transistors (Mn and Mp) and two resistors (Rn and Rp), and the ESD clamp nMOS transistor($\mathrm{M_{ESD}}$) drawn in BigFET layout style. The gate terminal of $\mathrm{M_{ESD}}$ is linked to the output of the ESD-transient detection circuit. The ESD-transient detection circuit with positive feedback mechanism is constructed by a cascode structure (Rn with Mn, and Mp with Rp), which can command $\mathrm{M_{ESD}}$ at "ON" or "OFF" state. To overcome the transient-induced latch-on issue, the ESD-transient detection circuit is added with diode string to adjust its holding voltage.

Because the ESD clamp nMOS transistor is drawn in BigFET layout style without silicide blocking, large Cgd, Cgs, and Cgb parasitic capacitances essentially exist in the ESD clamp nMOS transistor. Sufficiently utilizing these parasitic capacitances with the Rp to realize capacitance-coupling mechanism, no additional capacitor is needed in this design. Under ESD stress condition, the Mn immediately starts the ESD-transient detection circuit when the voltage of node A is elevated by capacitance-coupling. When the subthreshold current of the Mn can produce enough voltage drop on Rn to further turn on Mp, the voltage at node A would be quickly elevated to the voltage level at VDD because the ESD-transient detection circuit is turned on. Consequently, the $\mathrm{M_{ESD}}$ is turned on by the ESD-transient detection circuit with positive feedback mechanism. Although the leakage current can be reduced due to no actual capacitor device in ESD-transient detection circuit, the ESD clamp device drawn in BigFET layout style still contributes large gate leakage current. Therefore, some modifications of this design are required in nanoscale CMOS process as discussed in the following.

The modified power-rail ESD clamp circuit with p-type triggered SCR as the main ESD clamp device is shown in Fig. 13 [19]. The ESD-transient detection circuit is designed with considerations of the gate leakage current and the gate oxide reliability. In Fig. 13, Mp is used to generate the trigger current into the trigger node C of the p-type triggered SCR during the ESD stress event. Under the normal circuit operating condition, Mp is kept off and the trigger node is kept at VSS through the parasitic p-substrate resistor Rsub. Therefore, the p-type triggered SCR device is turned off during the normal circuit operating condition.

Due to lack of parasitic capacitor of BigFET, the RC-based ESD-transient detection mechanism is realized by the Rn and

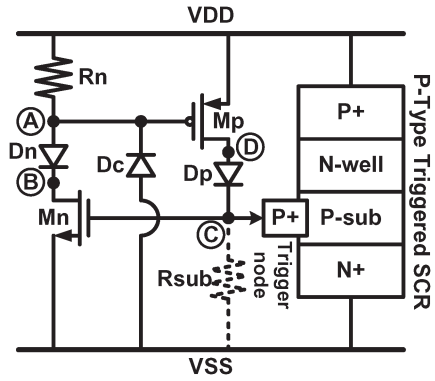

Fig. 13. Power-rail ESD clamp circuit with positive feedback [19].

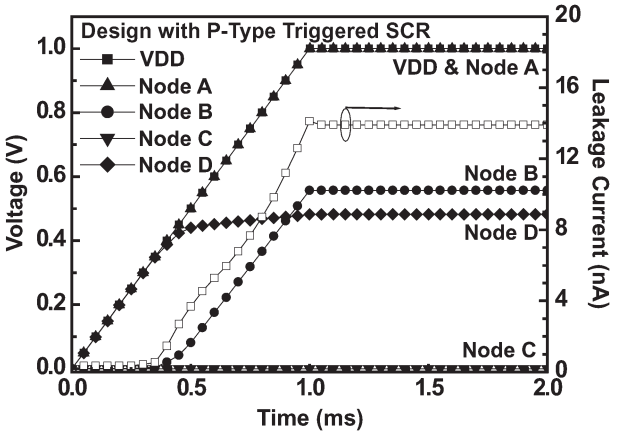

Fig. 14. Simulated voltage waveforms on the nodes and the leakage current of the ESD-transient detection circuit with positive feedback under the normal power-on transition.

the junction capacitance of the reverse-biased diode Dc. The reverse-biased diode Dc used as the capacitor can be free from the gate leakage current issue. The inserted diodes, i.e., Dn and Dp, in the ESD-transient detection circuit are used to reduce the voltage differences across the gate oxide of the transistors Mp and Mn in the ESD-transient detection circuit. Therefore, the leakage current and gate oxide reliability of Mp and Mn can be well controlled to minimize the total standby leakage current.

Under the normal circuit operation condition with VDD of 1 V and grounded VSS, the gate voltage of Mp is biased at 1 V through resistor Rn. The gate voltage of Mn is biased at 0 V simultaneously through the parasitic p-substrate resistor Rsub. Because Mp is kept off, no trigger current is generated into the trigger node of SCR. By inserting the diodes, i.e, Dp and Dn, in the ESD detection circuit, the voltages at nodes B and D can be clamped to the desired higher or lower voltage levels. Therefore, the drain-to-gate and drain-to-source voltages of Mp and Mn can be far less than 1 V to further reduce the standby leakage current.

The simulated voltage waveforms and the leakage current of the ESD-transient detection circuit during the normal power-on transition are shown in Fig. 14, where VDD is raising from 0 to 1 V with a rise time of 1 ms. In Fig. 14, the voltage differences across the gate-to-drain, gate-to-source, and drain-to-source terminals of all transistors in the ESD-transient detection circuit are only about 0.5 V. The simulated leakage current of the ESD-transient detection circuit is around 13.9 nA for the p-type triggered design.

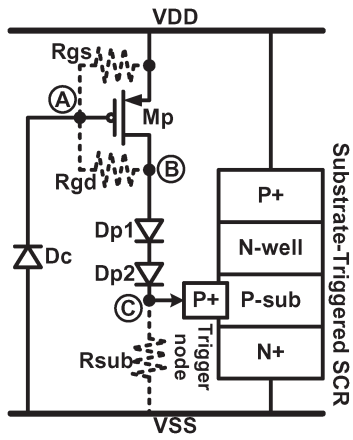

Fig. 15. Resistor-less design of power-rail ESD clamp circuit with diode string in the ESD-transient detection circuit [20].

G. Resistor-Less Design of Power-Rail ESD Clamp Circuit

The resistor-less design of power-rail ESD clamp circuit is shown in Fig. 15 with the p-type triggered SCR as the main ESD clamp device [20]. The ESD-transient detection circuit is also designed with considerations of the gate leakage current and the gate oxide reliability. The RC-based ESD-transient detection mechanism is realized by the equivalent resistors (Rgs and Rgd) of Mp and the junction capacitance of the reverse-biased diode Dc, which can distinguish the ESD stress event from the normal power-on condition. By using the gate leakage current of Mp, the induced equivalent resistors can be a part of ESD-transient detection mechanism to achieve the resistor-less design. In Fig. 15, Mp is mainly used to generate the trigger current into the trigger node C of SCR during the ESD stress event. Comparing to the thin gate oxide of MOS capacitor in the traditional RC circuit, diode Dc used as capacitor to realize the RC time constant can be free from the gate leakage current issue. The inserted diodes, i.e., Dp1 and Dp2, in the ESD-transient detection circuit are used to reduce the voltage differences across the gate oxide of Mp. Therefore, the total leakage current and gate oxide reliability of Mp can be safely relieved.

Under the normal circuit operation condition, the gate voltage of Mp is biased at VDD through resistors Rgs and Rgd induced by the gate leakage current. The cathode of Dp2 is simultaneously biased at VSS through the parasitic p-substrate resistor Rsub. Because Mp is kept off, no trigger current is generated into the trigger node of SCR. Inserting two diodes (Dp1 and Dp2) in the ESD-transient detection circuit can raise up the voltage of node B at the voltage level near to VDD. Therefore, all terminals of Mp are almost at the same voltage level of VDD to reduce its gate leakage current.

The simulated voltage waveforms and the leakage current of the resistor-less ESD-transient detection circuit during the normal power-on transition are shown in Fig. 16. In Fig. 16, the voltage of node A is successfully charged to the voltage level of VDD due to the gate leakage current. Therefore, Mp

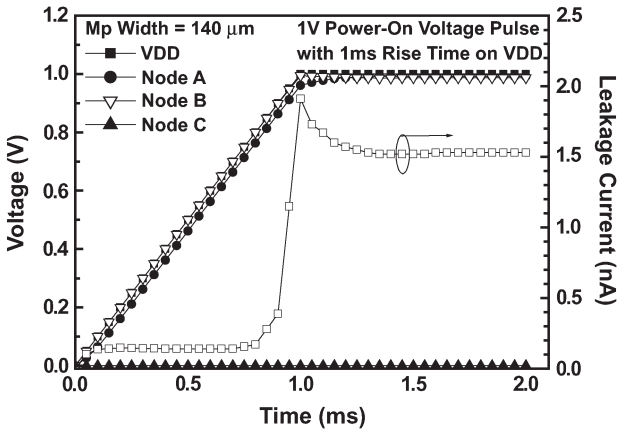

Fig. 16. Simulated voltage waveforms on the nodes and the leakage current of the resistor-less ESD-transient detection circuit under the normal power-on transition.

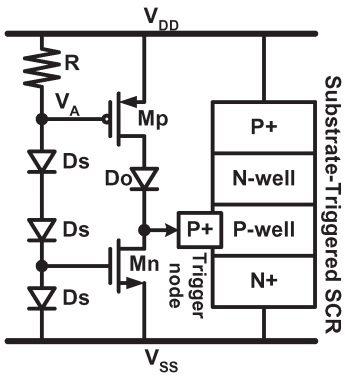

Fig. 17. Power-rail ESD clamp circuit with diode-string ESD detection [21].

is completely turned off, and the simulated standby leakage current of the ESD-transient detection circuit is only 1.53 nA.

H. Diode-String ESD Detection Circuit

The power-rail ESD clamp circuit designed with diode-string ESD detection is shown in Fig. 17 with the p-type triggered SCR as the main ESD clamp device [21]. This design was implemented with a diode string and a resistor to detect the ESD events by the high voltage level instead of the fast rise time.

Under normal circuit operation, the V_{DD} operating voltage is lower than the diode string threshold voltage. Therefore, there is no current flowing through R, and Mp is kept off. Adding a voltage drop by using a diode Do between Mp drain and the SCR trigger point (V_{TRIG}) would effectively reduce the leakage current from Mp. Under a PS ESD stress, the diode string starts to conduct some current when the V_{DD} voltage overpasses the diode string threshold voltage. That causes a voltage drop across R, thus turning Mp on to trigger the SCR.

The simulated results of this design with diode-string ESD detection during the normal power-on transition are shown in Fig. 18. In Fig. 18, the voltage (V_A) of node A is successfully charged to the voltage level of V_{DD}. Therefore, Mp is completely turned off and the simulated standby leakage current is only 52 nA.

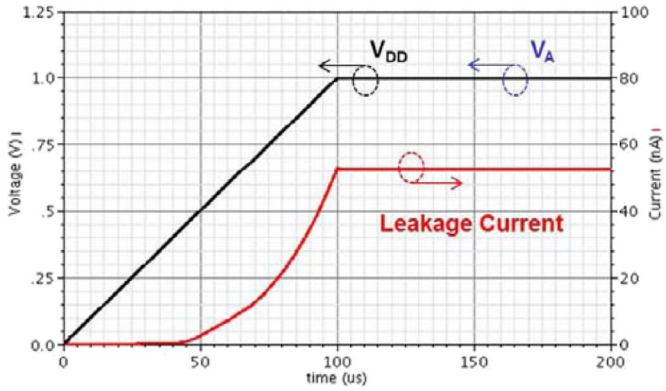

Fig. 18. Simulated voltage waveforms on the nodes and the leakage current of the diode-string ESD detection circuit under the normal power-on transition.

IV. Discussion and Comparison

The comparison among various power-rail ESD clamp circuits is summarized in Table II. Some evaluated parameters are explained as the following.

A. Standby Leakage Current

For the standby leakage current, the designs of II.A and II.C are moderate. For the design of II.C, although the MOS capacitor is replaced by MOM capacitor, the voltage difference across the transistors of inverter is not sufficiently reduced. By carefully considering the voltage difference across the gate oxide, the standby leakage current of the other designs (III.D to III.H) can be greatly reduced. In particular, for the design of III.G, the measured standby leakage current is only a few nanoamperes because all terminals of the MOSFET are biased at the same voltage level of VDD.

B. HBM ESD Robustness

In the design of III.B, the HBM ESD robustness is moderate for over 3 kV. With over 2000 μm channel width of ESD clamp device, the HBM ESD robustness of design III.A is good to be over 5 kV. For the designs of II.A and III.C, the HBM ESD robustness is better due to over 8 kV.

In designs of II.C, III.F, and III.G, the HBM ESD robustness is good for over 4 kV and 5 kV, respectively. With 120 μm SCR width in the design of III.D, the HBM ESD robustness is moderate to over 8 kV. However, the HBM ESD level of design III.E (III.H) is better to be 7 kV (6.5 kV) with only 45 μm (40 μm) SCR width.

C. Area Efficiency and Design Complexity

The area efficiency of traditional RC-based design (II.A) is poor because the RC time constant is typically designed about 0.1–1 μs. It would consume large layout area to implement resistor and capacitor, but the design complexity of traditional RC-based design is low. The layout area of design II.C with MOM capacitor is poor because the ESD-transient detection circuit is based on traditional RC-based design and still consumes large layout area to implement resistor and

TABLE II
COMPARISON AMONG POWER FAILURE CLAMP CIRCUITS

ESD Protection Design	Measured Standby Leakage Current at Normal Circuit Operation Voltage	HBM ESD Robustness	Area Efficiency	Design Complexity	Mis-Triggered
II.A – Traditional *RC*-Based	Moderate	Better	Poor	Low	No
II.C – MOM Capacitor	Moderate	Good	Poor	Low	No
III.A – Feedback Enhanced Triggering	Good	Good	Moderate	Moderate	Yes
III.B – Cascaded pMOS Feedback	Moderate	Moderate	Moderate	Moderate	Yes
III.C – Smaller Capacitance	Moderate	Better	Moderate	Moderate	No
III.D – Feedback Control Inverter	Good	Moderate	Moderate	Moderate	No
III.E – Utilization of Gate Current	Good	Better	Better	Moderate	No
III.F – Positive Feedback	Better	Good	Good	Low	No
III.G – Resistor-Less Design	Excellent	Good	Better	Low	No
III.H – Diode-String Design	Excellent	Good	Better	Low	No

MOM capacitor. Some previous designs (III.A and III.B) with feedback mechanism were presented to reduce the RC time constant and layout area. However, the reduction of layout area is limited because additional feedback circuits are required in the ESD-transient detection circuit, which increase the level of design complexity from low to moderate.

For the design of III.C, the area efficiency and the design complexity are both moderate, as compared with traditional RC-based design. The layout area of design III.D with feedback-control inverter is moderate because the resistances are reduced to consume smaller layout area. The layout areas of the other designs (III.E to III.H) are good even better because the device dimensions in ESD-transient detection circuit are greatly reduced. However, the designs of III.D and III.E require more devices to reduce the voltage difference across the gate oxide, which increase the level of design complexity as moderate.

D. Mistriggered

Some previous studies [22], [23] have demonstrated that the power-rail ESD clamp circuits with RC-based ESD-transient detection circuits were easily mistriggered or into the latch-on state under the fast power-on condition. Therefore, this issue exists in the designs of IIIA and III.B.

The designs of III.C and III.D can be safely applied to fast power-on condition without mistriggered issue. According to the circuit structure, the designs of III.F to III.H can also avoid those issues by adjusting the number of diode in diode string.

V. CONCLUSION

A comprehensive overview on the design of power-rail ESD clamp circuits in the nanoscale CMOS technology has been presented. Some process and circuit techniques used in the ESD-transient detection circuits were adopted to perform better turn-on behavior, lower standby leakage current, and higher efficiency of layout area. Generally, SCR is adopted as main ESD clamp device in the power-rail ESD clamp circuits due to no poly-gate structure. With considerations of the gate leakage current and the gate oxide reliability, the total standby leakage current in some advanced designs has been successfully reduced to the order of a few nanoamperes. Continuously, the power-rail ESD clamp circuit will still be an important design task for on-chip ESD protection as the process is further scaling down.

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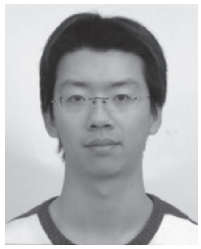

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