ECS Journal of Solid State Science and Technology, **3** (4) P86-P90 (2014)
2162-8769/2014/3(4)/P86/5/$31.00 © The Electrochemical Society

Experimental Demonstration of (111)-Oriented GaAs Metal–Oxide–Semiconductor Field-Effect-Transistors with Hetero-Epitaxial Ge Source/Drain

Tsung-Yu Han,[a] Guang-Li Luo,[b] Chao-Ching Cheng,[c] Chih-Hsin Ko,[c] Clement H. Wann,[c] Chi-Chung Kei,[d] Chien-Nan Hsiao,[d] and Chao-Hsin Chien[a,b,z]

[a]*Department and Institute of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan*
[b]*National Nano Device Laboratory, Hsinchu 300, Taiwan*
[c]*Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu 300, Taiwan*
[d]*Instrument Technology Research Center, National Applied Research Laboratories, Hsinchu 300, Taiwan*

We demonstrate source/drain (S/D) design for GaAs n-type metal-oxide-semiconductor field-effect transistor (NMOSFET) by embedding Ge into recessed S/D region to eliminate the intrinsic issues of the low solid solubility of dopants and low density of states (DOS) in GaAs material. For achieving high quality S/D epitaxy, the effects of substrate orientation and surface preparation on the quality of the epitaxial Ge film were investigated. High quality Ge film was successfully grown on the GaAs (111)A substrate by using a ultra high vacuum chemical vapor deposition (UHVCVD) tool and the significant improvement in the surface root-mean-square (RMS) roughness was observed as compared to that on the (100) substrate. The fabricated GaAs NMOSFET with hetero-Ge S/D exhibits an I_{on}/I_{off} ratio of $\sim 2.5 \times 10^2$. Even though the performance can be further improved, we think our proposed scheme sheds the light on overcoming the issues of the low solid solubility of n-dopant and low DOS in III-V MOSFETs.
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Manuscript submitted December 30, 2013; revised manuscript received February 3, 2014. Published February 13, 2014.

As CMOS technology scales into 15 nm node or beyond, various kinds of high-mobility III-V materials have being renewed as carrier transport channel for further high-speed and low-power MOS device applications.[1,2] However, III-V materials possess the lower values of n-type dopant solubility and DOS, possibly becoming the bottlenecks in outperforming the nano-scale Si devices. For GaAs, the values of DOS and the maximum n-type dopant (Si) solubility are only 4.7×10^{17} and 1×10^{19} cm^{-3}, respectively. As the devices shrink to the length-scale of 15 nm, carrier transport is approaching the ballistic regime, especially for the materials with light carrier mass. The phenomenon of "source starvation" would happen, which is the inability of the source region to sustain a large flow of carriers in 'longitudinal' velocity states in the channel, unless the momentum relaxation rate and the doping density in the source are sufficiently large.[3] Moreover, parasitic resistance in the S/D regions of the conventional MOSFET has been identified as one of the primary problems while transistor scaling. This problem can be significantly worse in the III-V NMOSFETs due to poor dopant activation in ion implanted S/D. Jenny Hu et al. demonstrated a nonalloyed MIS contact structure on InGaAs to reduce the effective barrier height of metal/semiconductor for minimal contact resistance.[4] X. Zhang et al. fabricated a new self-aligned nickel germanosilicide (NiGeSi) Ohmic contact to reduce S/D resistance.[5]

Ge has the proper values of DOS and the maximum n-type dopant activation level, which are 1×10^{19} and 6×10^{19} cm^{-3}, respectively. Heterogeneous integration of III-V and group-IV materials such as GaAs and Ge has attracted considerable attention. Thus, we propose the structure shown in Fig. 1, which could potentially tackle these critical issues and hence boost the current drive capability by using Ge as the hetero-structural S/D.

To fabricate such device, the process module of Ge epitaxial growth on GaAs substrate was utilized due to the absence of anti-phase domain (APD) defects.[6] Y. Bai et al. have concluded that the surfaces with high Ga-to-As ratio are beneficial to initiate defect-free Ge epitaxy on GaAs.[7] From the viewpoint of epitaxy, the growth of Ge on (111)A GaAs is advantageous over the growth of Ge on (100) GaAs because the former is terminated by the cations. Besides, applying (111)A substrates shows the improved electrical characteristics of GaAs NMOSFETs. In this study, high quality Ge films were successfully grown on (111)A GaAs substrates by using UHVCVD system and we demonstrated GaAs (111)A NMOSFETs with hetero-epitaxial Ge S/D showing I_{on}/I_{off} ratio of $\sim 2.5 \times 10^2$.

[z]E-mail: chchien@faculty.nctu.edu.tw

Experimental

Hetero-structure of GaAs NMOSFETs featuring embedded Ge S/D were fabricated on semi-insulator GaAs (111)A substrates. A 400-nm-thick SiO_2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) and then S/D region was recessed by etching SiO_2 and GaAs. Prior to selective growth of Ge, the wet-cleaned GaAs wafer was loaded into growth chamber of the UHVCVD system with a base pressure of less than 2×10^{-8} Torr. The wafer then went through an in-situ thermal desorption at 600°C for 10 min in H_2 ambient prior to GeH_4 flow to further removed the residual native oxide on the surface. After that, the Ge layer was grown at the same temperature with a constant GeH_4 flow rate of 10 SCCM. Throughout the entire growth process, the gas pressure was kept at 20 mTorr. In order to fabricate the Ge S/D, phosphorus (P) was implanted (1×10^{15} /cm^2, 30 keV) and activated at 600°C for 30 s with SiO_2 capping. An 8 nm aluminum oxide (Al_2O_3) dielectric film was deposited at 250°C by atomic layer dielectric (ALD) after removing the encapsulation layer and adequate surface preparation. After post deposition anneal (PDA) of 600°C in N_2 ambient, we excavated the S/D contact holes and inserted a 6 nm ALD-TiO_2 interfacial layer in an attempt to decease the contact resistivity of n-Ge S/D. Finally, Al was deposited as electrodes and the buffered oxide etch (BOE) solution was used to completely etch the exposed TiO_2/Al_2O_3 nanolaminate gate dielectric by using the Al contact as the hard mask.

Results and Discussion

Device design and band structure.— We embed Ge into the recessed S/D region in an aim to tackle the issues of poor S/D dopant and low DOS, which is the intrinsic problems for III-V materials. TCAD simulation is employed to evaluate the energy-band diagrams of Ge/GaAs heterojunction at various operation modes, as demonstrated in Figure 2, in which n^+-Ge and n^+-GaAs S/D doping were assumed to be 6×10^{19} and 1×10^{19} /cm^3, respectively. The doping profiles in the source, channel, and drain were assumed to be abrupt since the n-type dopant of Ge S/D we used in experiment is P, which obviously will not dope the GaAs channel.

It has been reported[8,9] that the high resistive contact in n-Ge is due to the high electron Schottky barrier height as a result of Fermi level pinning near the Ge valence band at the metal/Ge interfaces. Using a tunnel barrier to alleviate Fermi level pinning has been proved to be a workable way. TiO_2/Ge interface was estimated to have a nearly zero conduction band offset so that the tunneling resistance can be reduced mostly.[10] Hence, we adopted this technique to decease the

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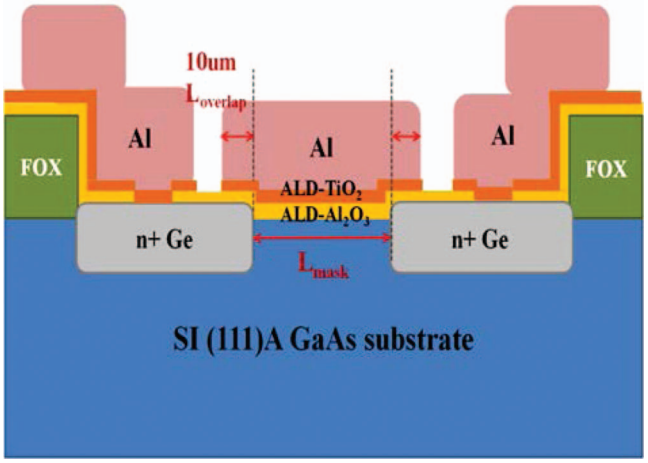

Figure 1. (Color online) Schematic representation of the enhancement-mode GaAs NMOSFET with embedded Ge S/D.

contact resistivity of epitaxial Ge S/D. We found that GaAs n-FET with TiO_2 capped Ge S/D exhibited the higher drive current I_D of $\sim 1.73 \times 10^{-2}$ μA/μm, which was corresponding to 33× enhancement against the one without TiO_2 layers (not shown). These improvements can be understood in terms of smaller S/D resistance (R_{SD}) for the n^+-Ge S/D with TiO_2 layers.

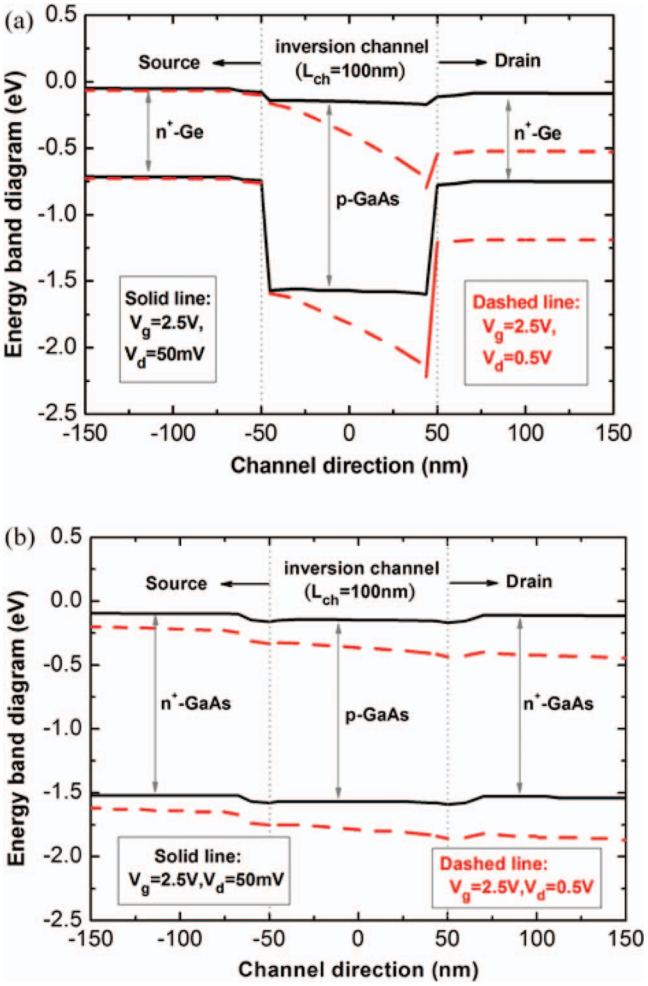

Figure 2. Energy band diagrams of GaAs NMOSFET with (a) n^+-Ge and (b) n^+-GaAs S/D, respectively (channel from the oxide surface 1 nm).

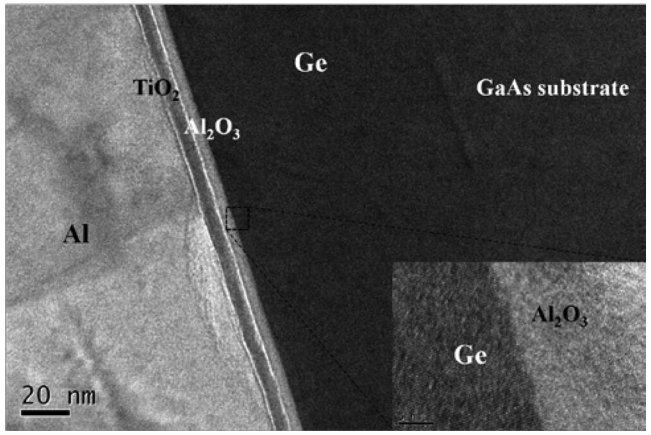

Figure 3. (Color online) Cross-sectional TEM image of selective Ge epitaxy on recessed GaAs S/D region and the overlap region of the TiO_2/Al_2O_3/Ge/GaAs gate stack. The inset is the high resolution TEM.

Material analysis of Ge epitaxy on different orientation GaAs substrates.— Fig. 3 shows the cross-sectional TEM image of Ge ($T_{dep.}$ = 35 min) selectively grown in the recessed (111)A GaAs S/D region and the overlapped region of gate stack. There are no extended defects such as stacking faults or dislocations at the Ge/GaAs interface because of nearly lattice matched. Fig. 4 plots the thickness of the epitaxial Ge film versus the growth time on (100) and (111)A GaAs substrates. The growth was the island mode at the initial stage with the slower rate; after that, the islands started to merge and it entered into the blanket mode with the accelerated rate, implying the existence of growth incubation time (T_{inc}). Here, we define incubation time (T_{inc}) as the intersection between the line corresponding to the steady growth and the growth time axis. From this diagram, the Ge growth on (111)A GaAs surface requires almost the same T_{inc} as on (100) GaAs surface since both surfaces are oxide-free after a prebake step at 600°C. Yu Bai et al. reported that the Ge growth on GaAs was initiated via the formation of a Ge-Ga bond because the Ge-As dimer has the higher formation energy than the Ge-Ga dimer. As we know, the surface stoichiometry of GaAs is strongly dependent on the wet cleaning steps, and the temperatures and pressures employed in the surface desorption and film growth, which in turn determines the resultant T_{inc}.[11] In other words, the same observed incubation time of

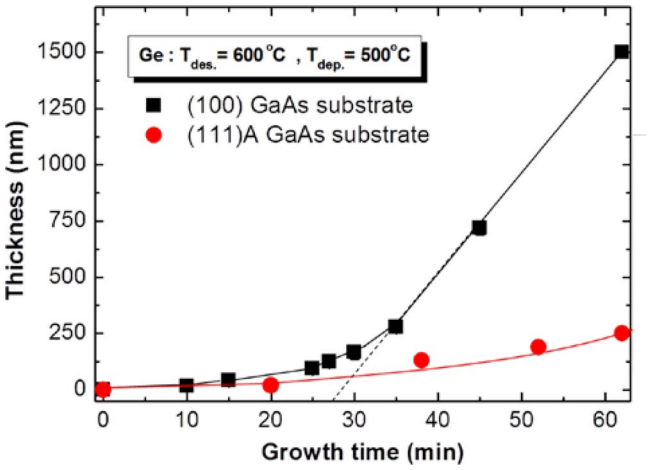

Figure 4. (Color online) Ge growth thickness vs. growth time on the different orientation GaAs surfaces. The solid lines are drawn as a guide for the eyes. The incubation times (T_{inc}) for Ge grown on GaAs (100) surface, are 28 min, consistent with grown on GaAs (111)A surface.

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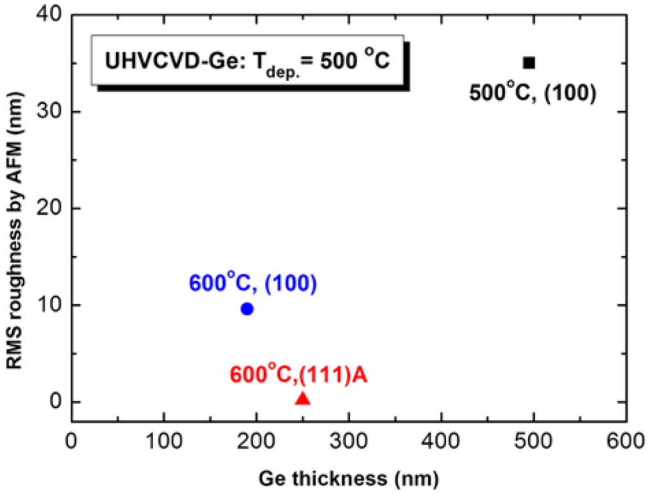

Figure 5. (Color online) The surface RMS (root-mean-square) roughness of grown Ge films versus the epitaxial thickness at different thermal desorption temperatures in H_2 ambient. (■) 500°C, (100) GaAs surface; (●) 600°C, (100) GaAs surface; (▲) 600°C, (111)A GaAs surface, respectively. The growth temperature was kept at 500°C.

(111)A and (100) GaAs surfaces means that the Ga/As ratio of both samples approach to 1/1 after a prebake step of 600°C.

Next, the effect of substrate orientation on the growth rate is studied under the condition of the fixed GeH_4 gas pressure and growth temperature. It is found that the growth rate on (100) GaAs substrate is higher than that on (111)A GaAs substrate. In the UHVCVD system, the mean free path of source molecules is sufficiently long, and the thermal conduction to gases is so low that the decomposition of source molecules happens only on the substrate surface and the decomposition in gas phase is negligible. Because of the fixed growth temperature and the fixed GeH_4 gas pressure, the restrictive process of the growth on (111)A GaAs substrate is affected neither by the decomposition of the source molecules, nor by the thermal activation process. The possible reason for the low growth rate on (111)A GaAs surfaces is attributable to the fewness of the adsorption site at the surfaces. This can be easily explained by the fact that the difference of surface density between (100) and (111)A GaAs surfaces, especially the surface density of the Ga dangling bonds. On (100) GaAs surface, the atoms surface density is equal to $2/a^2_{GaAs}$ (a_{GaAs} denotes the lattice constant of GaAs). On (111)A GaAs surface, while the atoms surface density is equal to $4/\sqrt{3}a^2_{GaAs}$, and each Ga atom on (111)A GaAs surface has 3 available dangling bonds. In contrast, each Ga atom on (100) GaAs surface has only 2 available dangling bonds. Thus, the Ga dangling bond densities on (111)A GaAs surface is obviously greater than the one on (100) GaAs surface, which leads to the slower growth rate of Ge on (111)A GaAs surfaces. In addition, the similar phenomenon has been reported by N. Sugiyama et al.[12] that the growth rate of Si and SiGe on (110) Si substrate is quite lower than that on (100) Si substrates.

In our experiment, the surface morphologies of Ge grown on the different substrate orientations and under different GaAs surface preparation conditions are investigated as in Fig. 5. The surface roughness of the sample with a prebake step of 600°C is observed to be improved relative to the one of 500°C; the corresponding RMS roughnesses were ca. 10 and 35 nm, respectively. It is known that, arsine (As) on the GaAs surface could hinder Ge atoms from bonding with Ga atoms, thus leading to seriously rough epilayer due to the Ge islands.[13] This can be easily understood by the fact that the Ge islands on the GaAs substrates are in Stranski–Krastanov mode;[14] the driving force is a reduction in the total surface energy by forming the low-energy Ge-Ga dimer at the surface. The significant improvement of the sample subject to a pre-bake at 600°C can be attributed to the almost full desorption of As before Ge deposition.

Furthermore, the samples grown with the same prebake condition but on (111)A GaAs substrate has more apparently smooth surface morphology, which RMS roughness was c.a. 0.2 nm. The corresponding SEM images are presented in Fig. 6. (111)A GaAs surface is terminated by the cations in contrast to (100) GaAs surface, indicative of a Ga-rich surface. For the samples grown on (111)A GaAs substrate, there are more available Ga sites for Ge adatoms to bond, hence resulting in a more uniform Ge epilayer.

Electrical characterization.— It has been demonstrated that adopting (111)A substrates shows the improved drain current of GaAs MOSFETs with ALD-Al_2O_3 dielectrics.[1,15] In this work, we systematically investigate the electrical properties of III-V MOSCAPs with (111)A and (100) orientations and confirm that the Fermi level (E_F) of GaAs (111)A surface is unpinned at the mid-gap with ALD-Al_2O_3 dielectric. From Fig. 7, we can observe the larger C-V stretch-out behavior and frequency dispersion presented in the depletion region for the p-GaAs (100) capacitor, indicating the existence of a higher density of interface states (D_{it}) near the mid-gap region for (100) orientation compared to the (111)A one.

In order to describe the Fermi-level pinning more accurately, the quasi-static CV (QSCV) curves of the capacitors with different substrate orientations are also shown in Fig. 7. The "inversion-like" response behavior is clearly observed for capacitor on (100) substrate which is correlated to the response of D_{it} close to the mid-gap region. On the contrary, the complete surface potential modulated by the gate voltage (accumulation → depletion → inversion) is seen for the capacitor on (111)A substrate. We utilized Berglund integration[16] to calculate the relation of surface potential and gate voltage on the different orientations as shown in Fig. 8. For (100) surface, the E_F moves from the valence band and then gradually saturates close to the mid-gap due to the existence of high D_{it} level, i.e., Fermi level pinning. This behavior is commonly observed in many early GaAs MOSCAP reports.[17–20] However, we found the surface potential on (111)A surface can almost move $2\Psi_B$ (~1.3 eV), implying the inversion caused by the gate bias.

We also estimated the D_{it} distribution in the bandgap for GaAs (100) and (111)A substrates using the high-low frequency C–V method.[16] As shown in Fig. 9, the minimum D_{it} is about 2×10^{12} (eV^{-1} cm^{-2}) and no broad peak distribution is detected at the mid-gap region of GaAs (111)A surface. Again, this is beneficial to move the

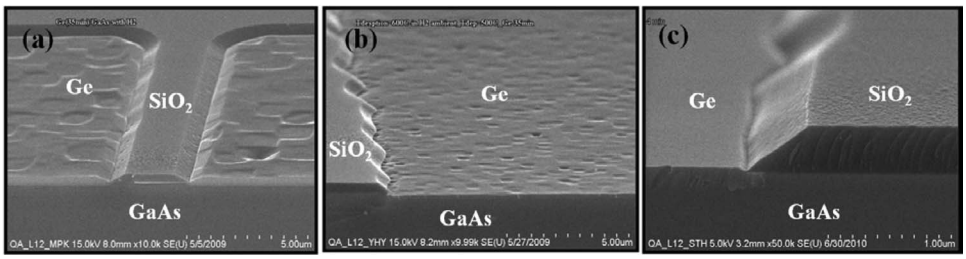

Figure 6. SEM images of the Ge/GaAs structures grown at different thermal desorption temperatures in H_2 ambient. (a) 500°C, (100) GaAs surface; (b) 600°C, (100) GaAs surface; (c) 600°C, (111)A GaAs surface, respectively. The growth temperature was kept at 500°C.

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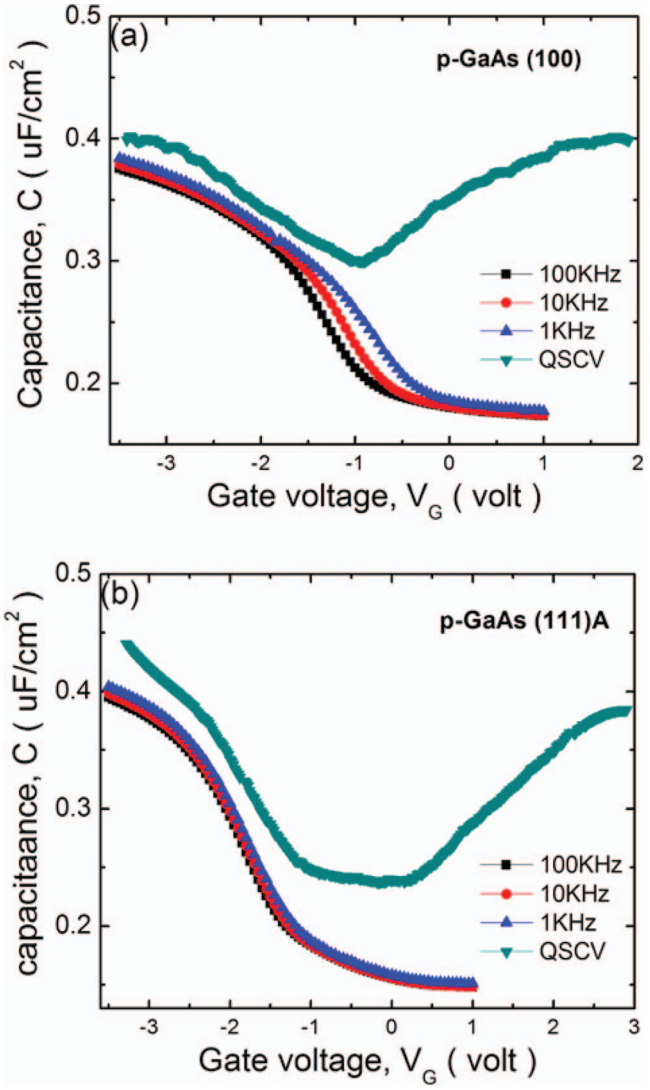

Figure 7. (Color online) Room temperature *C-V* and QSCV measurements of ALD-Al_2O_3/p-GaAs gate stacks for both (100) and (111)A substrates.

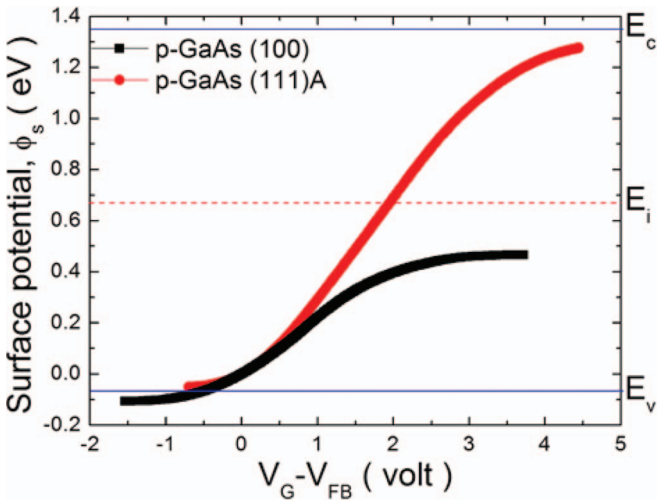

Figure 8. The surface potential movement versus gate voltage of Al/ALD-Al_2O_3/p-GaAs MOSCAPs on (100) and (111)A surfaces.

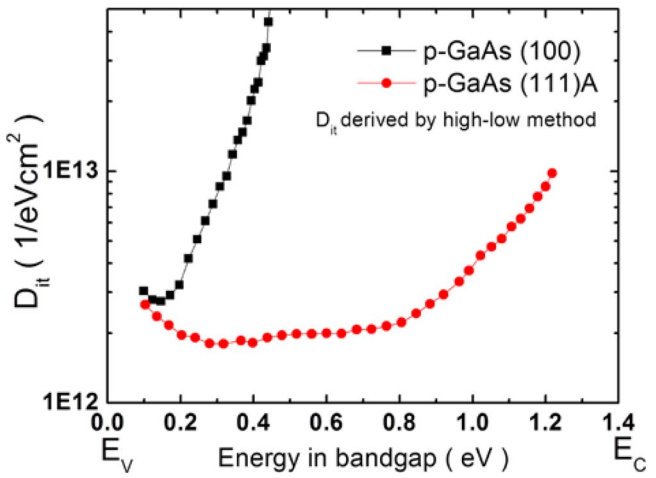

Figure 9. Comparison of interface state density (D_{it}) distribution of Al/ALD-Al_2O_3/ p-GaAs MOSCAPs on (100) and (111)A surfaces estimated by high-low frequency C–V method.

E_F of (111)A surface across the whole bandgap. However, there is a huge peak distribution for GaAs (100) surface, which is an obstacle to the surface band bending.[21] This difference in D_{it} is consistent with that in the previous C-V frequency dispersion. Even for (111)A orientation, it cannot reach strong inversion at the band edge due to a still large amount of the interface traps in the conduction band region. Further surface passivation on GaAs surface is needed. Recently, based on the high-quality epitaxial layer of high-*k* dielectric oxide, $La_{2-x}Y_xO_3$, high performance enhancement mode (E-mode) GaAs (111)A NMOSFET was implemented.[22,23]

Based on the epitaxy and electrical advantages of (111)A GaAs substrates, the GaAs nMOSFET featuring recessed Ge S/D are demonstrated. Fig. 10 displays the measured transfer characteristics I_{DS}-V_{GS} of the fabricated device (W/L = 100/10 μm and L_{OV} = 4 μm). The I_{on} (I_{DS} at V_{GS} = 2.5 V, V_{DS} = 2 V)/I_{off} (I_{DS} at V_{GS} = 1 V, V_{DS} = 2 V) ratio is ~2.5 × 10^2. The maximum drain current and the subthreshold swing (S.S.) of this device are 1.73 × 10^{-2} (μA/um) and ~270 mV/decade, respectively. The low inversion current of the fabricated hetero-structure devices might be due to the still high resistance associated with the TiO_2 dielectric layer on the Ge S/D, which could be improved by further process optimization. Moreover, an extra TiO_2

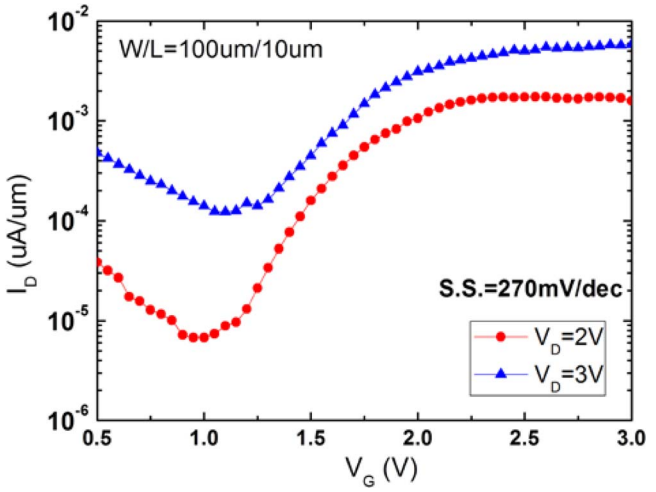

Figure 10. I_d-V_g (log-scale) characteristics of (111)A GaAs NMOSFET with n^+-Ge S/D. The L_{OV} and L_{ch} are 4 um and 10 um, respectively. The S.S. of the device is ~270mV/decade. The device performance can be further improved by optimizing the TiO_2/Ge contact resistivity.

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gate dielectric would increase the electrical oxide thickness (EOT) value, which also results in lower drive current.

Conclusions

High quality Ge film has been successfully grown at the GaAs recessed S/D regions with smooth surface using UHVCVD. Based on the grown material, the GaAs nMOSFET with hetero-Ge S/D has been fabricated and depicts an I_{on}/I_{off} ratio of $\sim 2.5 \times 10^2$. This proposed novel III-V MOSFET structure has the advantages of high electron mobility, high DOS value and high n-dopant level in S/D. For achieving high quality S/D epitaxy, Ge epitaxial growth on GaAs (100) and (111)A substrates were studied and compared. We find the film grown on (111)A GaAs substrate has significant improvement in the surface morphology, which RMS roughness was c.a. 0.2 nm. The incubation time of Ge growth on (100) and (111)A GaAs surfaces are almost the same because the Ga/As ratio of both samples approaches to 1/1 after a prebake step at 600°C. But the growth rate on (100) GaAs substrate is faster than that on (111)A GaAs substrate. The possible reason is attributable to the fewness of the adsorption site at (100) surfaces due to the lesser Ga dangling bond densities. The purpose of this work is to illustrate the concept and the potential way to cope with the intrinsic issues such as the low solid solubility of dopant and low DOS for III-V NMOSFETs.

Acknowledgment

This study was sponsored mainly by the National Science Council of Taiwan under grant NSC 101-2628-E-009-011-MY3. The authors thank dr. Chao-Ching Cheng and dr. Chih-Hsin Ko in TSMC for useful discussions.

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