Quasiresonant Control With a Dynamic Frequency Selector and Constant Current Startup Technique for 92% Peak Efficiency and 85% Light-Load Efficiency Flyback Converter

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***Abstract*—The proposed quasiresonant control scheme can be widely used in a dc–dc flyback converter because it can achieve high efficiency with minimized external components. The proposed dynamic frequency selector improves conversion efficiency especially at light loads to meet the requirement of green power since the converter automatically switches to the discontinuous conduction mode for reducing the switching frequency and the switching power loss. Furthermore, low quiescent current can be guaranteed by the constant current startup circuit to further reduce power loss after the startup procedure. The test chip fabricated in VIS 0.5 μm 500 V UHV process occupies an active silicon area of 3.6 mm^2. The peak efficiency can achieve 92% at load of 80 W and 85% efficiency at light load of 5 W.**

***Index Terms*—Constant current startup (CCS) circuit, discontinuous conduction mode (DCM), dynamic frequency selector (DFS), proportion integral compensator.**

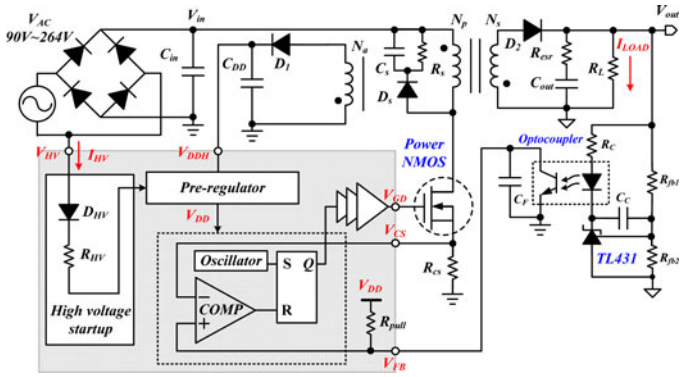

Fig. 1. Conventional flyback converter.

I. Introduction

THE public awareness about environmental issues has been raised, so there are growing concerns over energy-saving topic and green power in recent years. Nowadays, electronic equipment are widely used and developed, which brings tremendous commercial potentials about power-saving issues. Consequently, many researches put much emphasis on the power conversion efficiency and standby power losses of power converters.

Most of the electronic equipment has to take the isolation between high and low voltage (LV) into considerations for the safety concerns. Thus, flyback topology uses one transformer to terminate any straight electric connection between high input voltage and the converter's output power stage. Besides, a flyback converter can operate in continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CRM). Compared with the CCM, the CRM has the advantages of soft switching, fast transient response, smaller transformer size, and easier compensation for system's stability [1]–[3]. The conventional current-mode pulse width modulation (PWM) control flyback converter is depicted in Fig. 1; an oscillator is used to trigger the periodical switching cycle [4]. Although constant frequency control is much easier to design, it is far from green power because of high switching power loss at light loads. Besides, large power loss is dissipated due to the ON–OFF operation of the power switch if high voltage (HV) stress is across its drain and source terminals. Zero current detection (ZCD) is used to decide the turning-on timing [5], [6], which ensures system operation in DCM or CRM. However, it suffers from large switching power loss caused by the nonoptimum turning-on mechanism which lacks considering the output loading. Therefore, power efficiency is seriously decreased by extra switching power loss. For that reason, several turning-on control methods have been proposed to enhance power efficiency [7]–[15].

Quasiresonant (QC) control is one of the most popular methods to reduce switching power loss at light loads [16], [17]. Owing to the *LC* resonant tank composed of the transformer's inductance and the parasitic capacitance of the power MOSFET, the power MOSFET will be turned ON by the zero-voltage switching (ZVS) technique once the drain voltage resonates to the lowest value. Unfortunately, simply using the ZVS technique

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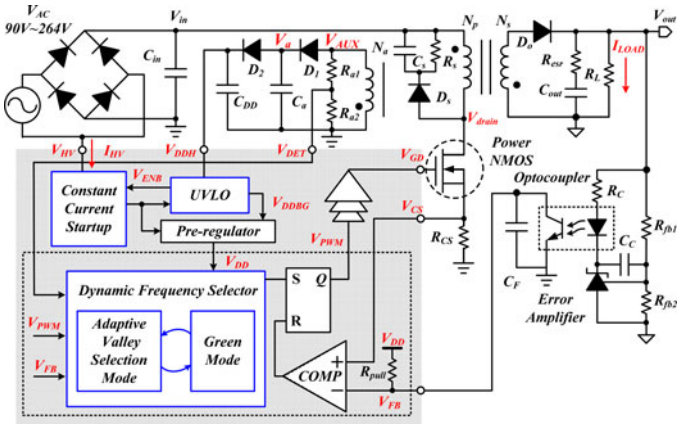

Fig. 2. Proposed flyback converter with the DFS and the CCS techniques.

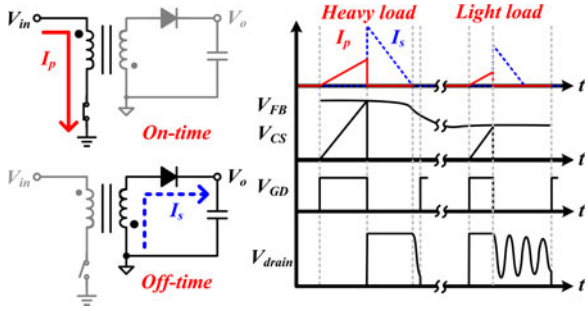

Fig. 3. Main operation of the proposed flyback converter.

still results in low efficiency and high switching frequency at light loads. The switching frequency becomes high due to small on-time duty caused by light-loading conditions. The switching power loss dominates the total power loss at light loads and further deteriorates the power conversion efficiency. To improve power conversion efficiency at light loads without being affected by the shrinking on-time length, the proposed dynamic frequency selector (DFS) technique is capable of adjusting off-time length according to the varied loading conditions. That is to say, the switching frequency is reduced with corresponding decreasing output loadings.

Moreover, the power dissipation at some passive components should be carefully considered to further reduce the standby power loss at light loads. Conventional startup circuit uses one diode followed by a high value resistor as the current source. However, diode and resistor cause serious leakage problem since they cannot be shut down after the startup period is done. Large leakage current results in low efficiency especially at light loads [18]. Thus, the proposed constant current startup (CCS) circuit replaces the diode with a depletion N-type MOSFET to generate the startup current. Thanks to the removal of the external passive components, the power consumption and the footprint area are able to be reduced effectively. Besides, the CCS circuit able to OFF the leakage path improves standby power efficiency. The aforementioned merits contribute to good power efficiency.

This paper is organized as follows. Two proposed techniques are described in Section II. The circuit implementations are illustrated in Section III. The system stability is analyzed in Section IV. Experimental results are shown in Section V. Finally, conclusions are made in Section VI.

II. System Operation of the Proposed Flyback Converter

The proposed structure of the current-mode flyback converter is depicted in Fig. 2. Similar to conventional flyback converter, the power stage contains one transformer with three windings and one optocoupler functioning as isolation between the output stage and the input stage [19]. The flyback converter uses transformer's magnetizing inductance to store energy and then to transfer it to the output.

Basically, switching power loss can be divided into two parts, conduction power loss in (1) and switching power loss in (2), including charging and discharging $C_{\rm oss}$, where I_p is the primary-side current, $R_ds,_{\rm on}$ is the on-resistance of the power switch, $C_{\rm oss}$ is the gate-source parasitic capacitance of the power MOSFET, $V_{\rm ds}$ is the drain–source voltage, and $f_{\rm sw}$ is switching frequency

$$P_{con\_{\rm loss}} = I_p^2 R_{ds,{\rm on}} \tag{1}$$

$$P_{{\rm sw}\_{\rm loss}} = C_{\rm oss} V_{ds}^2 f_{\rm sw}. \tag{2}$$

At heavy loads, the proposed flyback converter operates in the CRM, which is similar to conventional flyback with the ZCD control. Thus, the switching power loss can be ignored and the total power loss is dominated by conduction power loss. On the other side, switching power loss gradually dominates the total power dissipation at light loads due to the nonzero value of $V_{\rm ds}$. Thus, it is more important to reduce $V_{\rm ds}$ and $f_{\rm sw}$ to reduce the switching power loss. The proposed flyback converter not only detects the resonant valley voltage to minimize power loss at $V_{\rm ds}$, but also optimizes the switching frequency according to the output loading conditions. Thus, two parts of switching power loss can be effectively reduced.

Fig. 3 shows the main operation of the proposed flyback converter. The primary-side and secondary-side currents are I_p and I_s, respectively, which is in the shape of triangle waveform. The voltage $V_{\rm CS}$, across the current sensing resistor $R_{\rm CS}$, is used as a current-mode control signal when the power MOSFET turns ON. The feedback voltage $V_{\rm FB}$ determined by the feedback network composed of optocoupler and the TL431 working as an error amplifier proportional to the output loading. The on-time duty can be decided by the comparison results of $V_{\rm CS}$ and $V_{\rm FB}$. On the other hand, the off-time length is detected by the valley voltage of $V_{\rm drain}$ to achieve near-ZVS operation. To avoid increasing the switching frequency when the input voltage or the loading is low, the DFS technique can select one of the valleys accordingly to change the off time.

A. Proposed DFS Technique

The operation of the DFS technique as depicted in Fig. 4 contain two modes, the valley selection mode and the Green mode. When the input voltage or the loading gradually becomes lower to some extent, the automatic voltage stabilizer (AVS) mode accordingly decreases the switching frequency to reduce

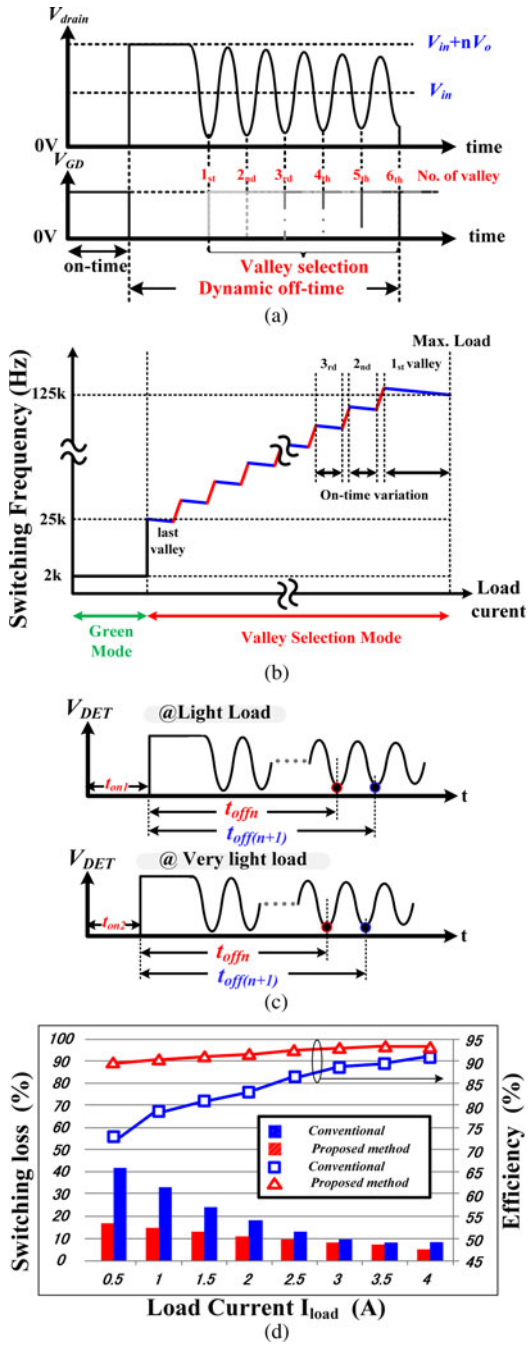

Fig. 4. (a) Operation of the DFS technique. (b) Switching frequency versus the loading current. (c) Subtle change of on time and off time along with the load changes. (d) Simulation results of efficiency and power consumption at different loads ($V_{\rm AC} = 110$ V).

switching power loss. In Fig. 4(a), the stored energy in the primary winding (N_p) is transferred to the output when $V_{\rm GD}$ changes from high to low to turn OFF the power MOSFET. Due to Lenz's law, $V_{\rm drain}$ at the drain of power MOSFET jumps from zero to $V_{\rm in}+nV_{\rm out}$. At this moment, I_p begins to decrease toward zero. When I_p is down to zero, the stored charges in the drain terminal of the power MOSFET starts to dash to the transformer side and then back to the drain side back and forth. Resonant phenomenon with a resonant frequency determined by $C_{\rm DS}$ and L_P starts and is reflected to the auxiliary side simultaneously. To reduce switching power loss, the optimum turn-on timing occurs at the valley of $V_{\rm drain}$ because the near ZVS will bring low switching power loss. Put into another words, the valley voltage detection in the resonant effect is able to determine the next turn-on timing of the power MOSFET.

In the DFS technique, dynamic off-time control can be derived by the selection of the valley at different loads as illustrated in Fig. 4(b). At heavy loads, the conduction loss dominates the energy efficiency. That is why the first valley is the optimum choice to deliver energy to the output since the minimum off-time length can be achieved. Besides, the peak value of the inductor current is also reduced to help increase the overall efficiency. On the other hand, the switching power loss dominates the energy efficiency at light loads. Consequently, the off-time length is further extended by picking up the later valley according to the load conditions to reduce the switching power loss.

If the system does not have the AVS technique, the switching frequency will gradually increase along with the decrease of the load current owing to the decrease of both the on-time and off-time length. The reason is the selection of the valley cannot continuously change from one valley to the other valley owing the quantization error at the selection of valleys. If the valley selection is changed to the next one of the sequential number, the switching frequency will decrease immediately to further reduce the switching power loss. The instant decrease of the switching frequency contributed by the adaptive valley selection can greatly improve the power conversion efficiency.

When the load gradually decreases, the on-time period also becomes shorter as depicted in Fig. 4(c). It causes both switching frequency increases as expressed in (3). Owing to the decrease in the on-time period where one valley voltage is selected, the off-time period $t_{{\rm off}\,n}$ in this case is determined

$$f_1 < f_2, \quad \text{where } f_1 = \frac{1}{t_{\rm on1} + t_{{\rm off}\,n}} \qquad f_2 = \frac{1}{t_{\rm on2} + t_{{\rm off}\,n}}, \text{ and } t_{\rm on1} > t_{\rm on2}. \tag{3}$$

Unfortunately, the switching power loss also increases. Therefore, the AVS technique is used to make the switching frequency modulated with the load condition for effectively improving efficiency. That is to say, the next valley voltage, which determines the longer off time $t_{{\rm off}\,(n+1)}$, is selected to reduce the switching frequency. As shown in (4), the new switching frequency f_2' is smaller than the f_1 due to the increase of the off-time period

$$f_1 > f_2' \quad \text{where } f_2' = \frac{1}{t_{\rm on2} + t_{{\rm off}\,(n+1)}}. \tag{4}$$

Besides, the duration between $t_{{\rm off}\,(n+1)}$ and $t_{{\rm off}\,n}$ can be predicted by the resonant inductance and capacitance. Therefore, the boundary condition can be derived as shown in

$$(t_{\rm on1} - t_{\rm on2}) < (t_{{\rm off}\,(n+1)} - t_{{\rm off}\,n}) = 1/2\pi\sqrt{LC} = 2\pi\sqrt{LC}. \tag{5}$$

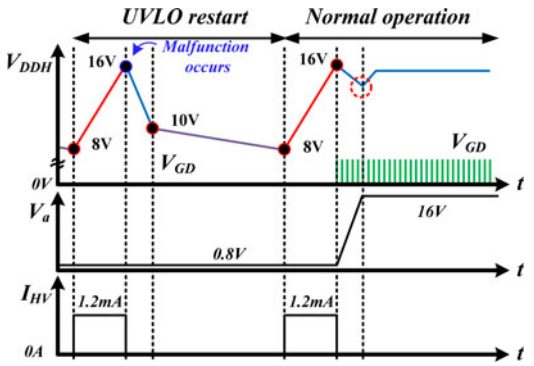

Fig. 5. Proposed CCS technique with the UVLO under different operation conditions.

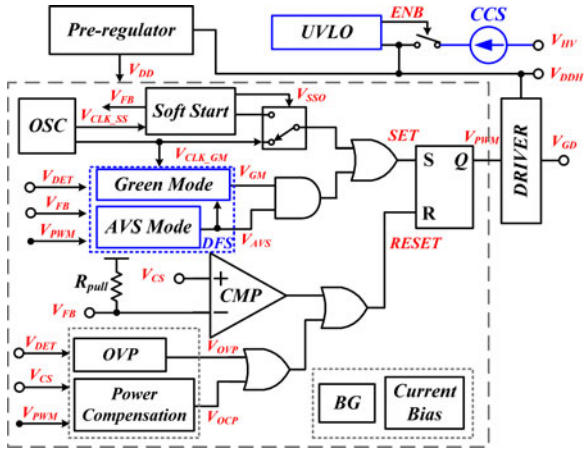

Fig. 6. Architecture of the proposed flyback convertor controller.

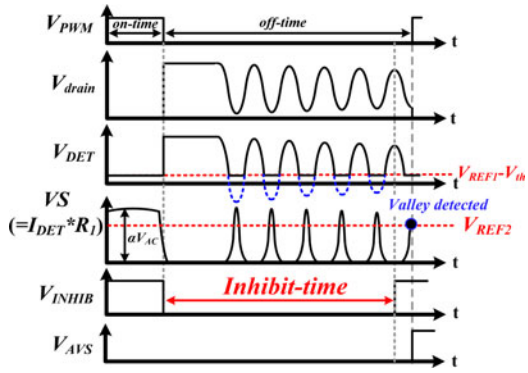

Fig. 7. Waveforms of the DFS in a switching period.

In summary, the trend of the switching frequency is decreasing when loading current decreases. Fig. 4(d) shows that the power conversion efficiency can be improved due to the reduction of the switching power loss contributed by the DFS technique. Along with the decreasing load, the resonant amplitude becomes smaller because of the parasitic resistance at the resonant path. It may fail to detect the valley voltage due to the gradually decaying valley voltage. That is, the next on-time needs to be triggered by another mechanism for correction and safety operation. Thus, the Green mode is proposed to set the off time with a constant value of 500 μs for further improving efficiency at ultralight loads and to ensure the correct operation of the converter. Furthermore, the maximum load is limited by the predefined maximum on time for system protection.

B. Proposed CCS Technique and Power-on Sequence

In the design of flyback converters, the correct power-on sequence can protect the device from damaging. The supply is provided by the auxiliary winding (N_a) of the transformer as depicted in Fig 2. Prior to the first switching of the controller, there is no power that can be delivered to auxiliary winding because the output voltage is still lower than some extent. Thus, a low quiescent startup circuit is necessary to ensure the internal supply voltage, $V_{\rm DDH}$, high enough to make the converter work correctly. Furthermore, the startup circuit is supposed to be shut down right after the end of the start-up procedure to further save power.

As depicted in Fig. 5, a constant startup current I_{HV} is designed to be around 1.2 mA to slowly ramp up $V_{\rm DDH}$ before the end of the startup period. Constant charging current can protect the ultrahigh voltage (UHV) device from breaking down by large startup current. Once the value of $V_{\rm DDH}$ reaches the expected internal voltage, the control authority of the converter is transferred to the switching control loop. The gate control signal $V_{\rm GD}$ controls the switch of the power MOSFET. Simultaneously, V_a at the auxiliary winding (N_a), depicted in Fig. 2, is charged to 16 V as an internal supply voltage for the controller. Before the switching control loop dominates, V_a is clamped to a lower level. Here, the under voltage lockout (UVLO) circuit monitors the value of $V_{\rm DDH}$. If $V_{\rm DDH}$ is smaller than 10 V, the switching control loop will be stopped to shut down the system and wait for the autorecovery mechanism. In other words, the system tries to wake up to restart the CCS circuit in the autorecovery procedure once $V_{\rm DDH}$ is smaller than 8 V.

III. Circuit Implementation

The proposed flyback controller is depicted in Fig. 6 with three parts, LV part, HV part, and UHV part. The UHV part is the CCS circuit that offers the HV supply $V_{\rm DDH}$ with a value of 16 V for the HV driver to turn ON the external power MOSFET. The HV part is composed of the UVLO circuit and the preregulator. The preregulator functions as the internal power supply 5 V for the LV circuit. Basically, the LV part includes on-time and off-time control circuits to determine $V_{\rm GD}$. In addition, internal LV bandgap can provide accurate reference voltage and biasing current to ensure a voltage with high quality for the control circuit.

A. DFS Circuit Design

The proposed DFS technique consists of two circuits. The AVS mode is in charge of all loads conditions with the exception of ultralight-load status controlled by the Green mode. The waveforms of the DFS are depicted in Fig. 7. When the power MOSFET turns ON, the sink current I_{DET} is proportional to the line voltage $V_{\rm AC}$ since V_{DET} is a reflected voltage of $V_{\rm AC}$. Here, I_{DET} offers two major functions. The first one is that

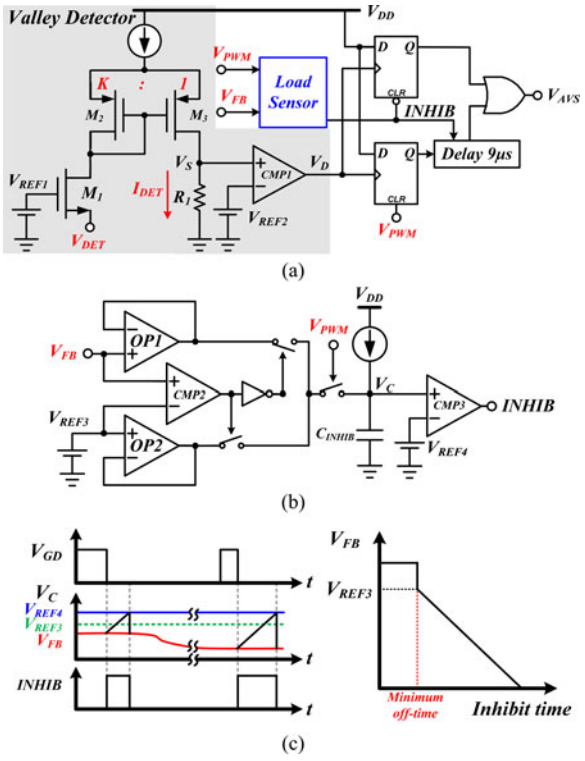

Fig. 8. (a) AVS circuit. (b) Load conditions sensor. (c) Inhibit time is controlled by $V_{\rm FB}$ and the corresponding timing diagram.

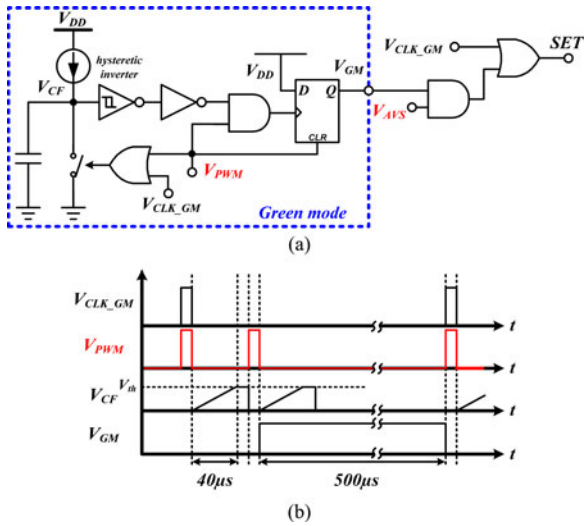

Fig. 9. (a) Green mode circuit. (b) Timing diagram of the Green mode control.

I_{DET} is capable of generating corresponding volume of current to compensate the power during the on-time period. The second one is the valley detection during the off-time period. During the off-time period, I_{DET} is inversely proportional to $V_{\rm drain}$ because the source of the transistor M_1 clamps V_{DET} to be lower than the reference $V_{\rm REF1}$ about one MOSFET threshold voltage $V_{\rm th}$ as depicted in Fig. 8(a). The lower $V_{\rm drain}$ in Fig. 2, the larger the I_{DET}. Therefore, the valley sensing signal V_S equal to the product of I_{DET} and R_1 compares with the reference $V_{\rm REF2}$ to determine each single valley of off-time periods. The inhibit time is inversely proportional to the feedback voltage $V_{\rm FB}$. The *INHIB* changes from low to high at the beginning of the off time. Then, $V_{\rm AVS}$ can be set to high to turn on the power MOSFET by the AVS circuit after the *INHIB* is triggered to low by the load sensor.

Besides, the *INHIB* in Fig. 8(a) is a load-dependent signal which indicates the corresponding minimum off-time length under a certain load condition. The lower the load, the longer the *INHIB*. The valley detector utilizes the reference voltage $V_{\rm REF1}$ and the transistor M_1 whose source connected to V_{DET} from the auxiliary winding to generate a current-dependent voltage. V_{DET} swings to a negative voltage while the power MOSFET's drain voltage has the resonance phenomenon and tends toward the valley. Therefore, the lower the drain voltage, the more the sourcing current flows from M_1. V_{DET} is clamped around 0.3 V if $V_{\rm REF1}$ is 1 V to avoid negative voltage seen by the chip from the possible hazard of the latch-up issue. In the meanwhile, the sourcing current is mirrored to flow through R_1 to produce the sensing voltage V_S. To choose a suitable reference voltage helps catch every single valley during the off time.

The load sensor depicted in Fig. 8(b) is able to convert the feedback voltage $V_{\rm FB}$ to the time duration, *INHIB*, which indicates load current information. When $V_{\rm PWM}$ changes from high to low, the current source starts to charge C from $V_{\rm FB}$ to $V_{\rm REF4}$ as shown in Fig. 8(c). Therefore, smaller $V_{\rm FB}$ indicates smaller output loading but longer inhibit time. $V_{\rm REF3}$ is set to determine the minimum off time. Once the inhibit time is over, the valley detection signal V_D is allowed to trigger the upper side flip–flop to set $V_{\rm AVS}$ high. Besides, the unpredictable value of parasitic resistances in the *LC* resonant path causes resonant amplitude decaying so much that it is hard to detect especially under light-load conditions which has longer inhibit time. In order to avoid the aforementioned situation, another path composed of the lower side flip–flop cascaded with a 9 μs delay circuit can set the maximum off time. That is to say, if the system cannot detect any valley voltages excluding the first valley voltage within 9 μs when the *INHIB* changes from high to low, $V_{\rm AVS}$ is set to high for getting a maximum off time. Therefore, if the off-time exceeds maximum setting length, the controller turns on power MOSFET to guarantee the next on-time in case of the decaying valley voltage goes as much as it could.

The proposed Green mode has two advantages. One is to avoid the undesired scenario happening when the valley voltage is decaying so much that it is hard to be detected if off time length is too long to some extent. The other advantage is to further improve the ultralight-load efficiency due to the greatly reduced switching power loss. Fig. 9 shows the Green mode circuit to determine whether the off time is longer than 40 μs or not. Once the off time is longer than 40 μs, the system will enter the Green mode and the switching frequency is down to 2 kHz. When $V_{\rm PWM}$ becomes low, $V_{\rm CF}$ starts to be charged until the hysteretic inverter changes its state. The charging period is designed around 40 μs. Thus, if the off-time period is longer than 40 μs, the Green mode signal V_{GM} will become high to block the $V_{\rm AVS}$ as shown in Fig. 9(a). Thus, the system operates

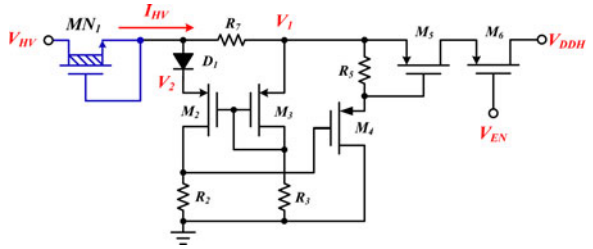

Fig. 10. CCS technique.

with the frequency of 2 kHz at the next switching period as shown in Fig. 9(b).

B. CCS Circuit and UVLO Design

To achieve the constant current from V_{HV}, the converter needs a startup circuit with the CCS technique as shown in Fig. 10. An ultrahigh-voltage depletion N-type MOSFET MN_1 is used with its gate and source shorted to function as one current source. The transistors M_2, M_3, M_4, and M_5 form a negative feedback in a closed loop. M_2 and M_3 are used as a differential pair. M_4 is used as a level shifter to ensure that M_5 can be fully turned ON. The transistors M_4 and M_5 form a negative feedback path to ensure the constant HV startup current because nearly constant voltage across D_1 is produced. I_{HV} charges one capacitor to slowly ramp up the voltage $V_{\rm DDH}$ to the system operational voltage set at the value of 16 V. Eventually, V_{EN} signal comes from the UVLO circuit to shut down the HV startup for further power reduction.

The UVLO circuit is utilized for IC's startup and autorecovery protection by detecting the supply voltage $V_{\rm DDH}$. The startup procedure using the CCS technique charges $V_{\rm DDH}$ to 16 V so that chip starts to work. Autorecovery protection protects the system against short circuit at $V_{\rm out}$, undesired open feedback loop, and any other system malfunctions. If any of the aforementioned condition occurs, the gate signal out of the controller would be ceased and $V_{\rm DDH}$ starts to decrease. Once $V_{\rm DDH}$ reaches 10 V, the HV preregulator will be shut down and no power supply would be sent to the controller. Besides, the UVLO circuit provides a hysteresis space, i.e., from 10 to 8 V, which can extend the restarting time to avoid the possibility of burning down issues caused by high temperature of whole system. The hysteresis window is determined by the time that the system needs to cool down.

Fig. 11 shows the UVLO circuit that has an ability to monitor $V_{\rm DDH}$ and based on different conditions to shut down or switch on the controller and the CCS circuit. V_{EN} is the enabled signal to switch on the controller. $V_{\rm DDBG}$ is the power supply for the HV preregulator. The stacking components include zener diodes and *NPN BJT*s to detect the 16 and 8 V. It means that as soon as $V_{\rm DDH}$ is higher than one extent, the voltage across the resistor R_1 is designed to be higher than the threshold voltage of the transistor M_1. Thus, the transistors $M_1 - M_3$ turn ON and V_{EN} becomes high to shut down the CCS circuit with a quiescent current of near 0 mA for power saving. At the same time, the transistor M_7 is turned ON and the drain voltage is

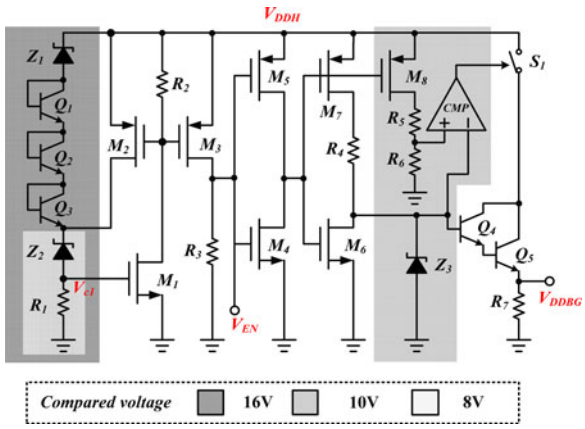

Fig. 11. Operation of the UVLO circuit.

clamped by the zener diode Z_3. Thus, $V_{\rm DDBG}$ is derived by two base–emitter voltages of bipolar subtracted from the clamping voltage for the *LV* biasing circuit.

To compare 10 V voltage, the right-side circuit of the UVLO circuit consists of M_8, R_5, R_6, Z$_3$, and the *CMP*. It utilizes R_5 and R_6 to obtain the divided $V_{\rm DDH}$. And the divided voltage compares with the voltage of Z_3. Consequently, when $V_{\rm DDH}$ is lower than 10 V, S_1 turns OFF and $V_{\rm DDBG}$ is pulled to ground, which shut down the chip. Another comparison voltage is already prepared because the turning ON M_2 causes the left-side stacking voltage becomes 8 V noted as V_{c1}. If $V_{\rm DDH}$ decreases below 8 V, the UVLO is shut down and V_{EN} is sent to the CCS circuit to restart the startup procedure. After the UHV start-up procedure, the axillary winding side supplies power to the whole chip continuously. According to the ratio between the secondary side and the axillary side, $V_{\rm DDH}$ from the axillary side is 16 V, which is around 0.8 times $V_{\rm out}$.

C. Soft Start

During the power-on period, the resonant valley voltage is too small to be detected. Therefore, it needs a soft start period modulated by the oscillator (OSC) circuit until the valley voltage is large enough. In Fig. 12(a), the soft start circuit includes a 4-bit up-counting counter which controls four current sources to build the soft start voltage V_{ST} across the resistor R_1 with a small voltage step increment. The operational amplifier (OP) functions as the unit gain buffer. That is to say, $V_{\rm FB}$ is elevated with a growing voltage step trails along V_{ST} as shown in Fig. 12(b). Here, the OP, the transistor M_1, and the compensation capacitor C_1 act like a two-stage OP. $V_{\rm PWM}$ has a switching period of 30 μs in the beginning of soft start until the valley voltage can be detected. The corresponding current sense signal $V_{\rm CS}$ tracks the variation of $V_{\rm FB}$. The soft start happens when the internal power supply 5 V is ready. V_{SSO} is a signal to show whether the soft start is over or not.

D. Power Compensation Circuit

Fig. 13 shows how the current limit signal V_{PC} is inversely proportional to the input ac source $V_{\rm AC}$. To create a signal

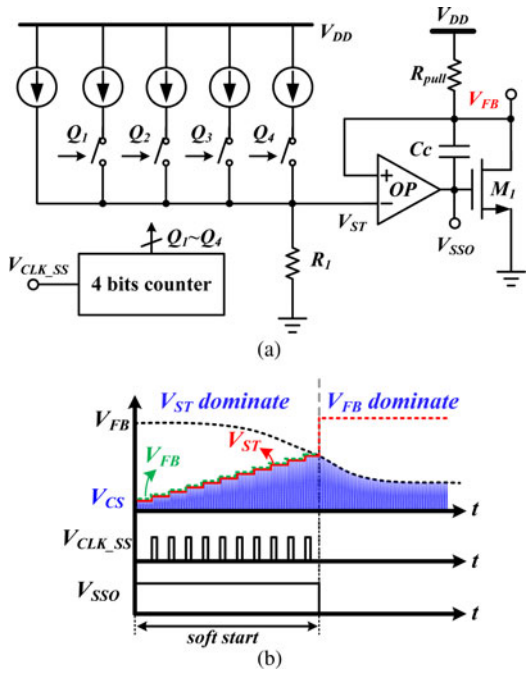

Fig. 12. (a) Soft start circuit. (b) Soft start procedure.

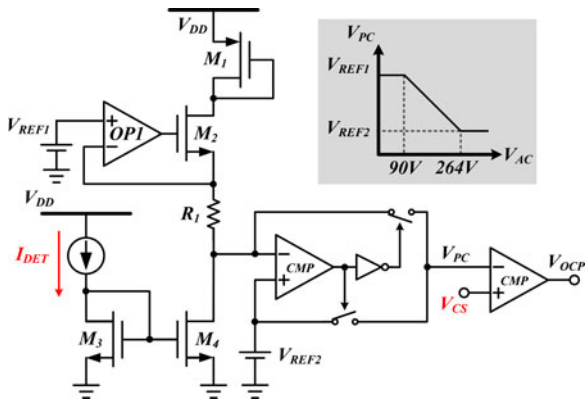

Fig. 13. Power compensation circuit.

proportional to $V_{\rm AC}$, the controller must have $V_{\rm IN}$ information in every switching cycle. Observing Fig. 2, $V_{\rm IN}$ is the root mean square value of $V_{\rm AC}$ and will be reflected to the auxiliary side when the power MOSFET turns ON. Due to the polarity between primary winding and auxiliary winding, the higher the $V_{\rm IN}$, the more negative the $V_{\rm AUX}$. It results in larger sink current of I_{DET}. The power compensation circuit also uses the current I_{DET} mirrored from Fig. 7(a) to get the input voltage information. Consequently, the increasing input ac voltage $V_{\rm AC}$ will lead the decreasing of current limit voltage V_{PC}. Besides, V_{PC} is limited between $V_{\rm REF1}$ and $V_{\rm REF2}$. The two voltages are determined by the input voltage range, the resistance of current sense, and the switching period. Finally, for ensuring that the output power can be controlled, it compares V_{PC} and the current sense voltage $V_{\rm CS}$ to limit the output current. If the overcurrent occurs, V_{OCP} will be triggered to shut down the power MOSFET.

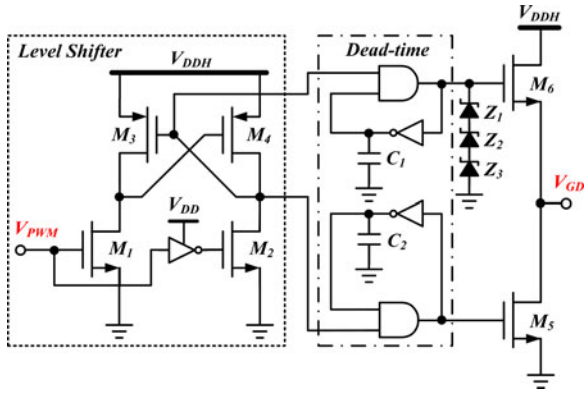

Fig. 14. Level shifter and the driver circuit.

E. Level Shifter and Driver

The driver circuit is depicted in Fig. 14. The transistors M_1–M_2 and M_3–M_4 form the level shift circuit to convert $V_{\rm PWM}$ from the lower internal supply voltage $V_{\rm DD}$ to the higher supply voltage level $V_{\rm DDH}$. The dead-time circuit can avoid the shoot-through current. The transistors M_5 and M_6 are responsible for driving the external power MOSFET. The zener diodes, $Z_1 - Z_3$, clamp the upper driver voltage at 18 V to avoid damage on the gate oxide.

IV. System Stability Analysis

Fig. 15(a) shows an equivalent small signal model based on the architecture in Fig. 2. Basically, it consists of two parts, control-to-output transfer function $G_{\rm CO}$ and output-to-control transfer function G_{OC} [20]–[24]. The output voltage $V_{\rm out}$ is the product of the averaged secondary-side current $I_{s\_\rm avg}$ and the output impedance $Z_{\rm out}$ which includes the output filter, related parasitic resistor, and output resistor R_L. As depicted in Fig. 15(b), $I_{s\_\rm avg}$ is the integral of the secondary-side current I_s within one switching cycle as shown in

$$I_{s\_\rm avg} = \frac{\frac{1}{2} \cdot (t_{\rm dis} \cdot I_{s\_\rm pk})}{1/f(V_{\rm FB})}. \tag{6}$$

$t_{\rm dis}$ is the discharging time of secondary-side current. $I_{s\_\rm pk}$ is the peak value of the secondary-side discharging current. $1/f(V_{\rm FB})$ represents that the switching frequency f is the function of $V_{\rm FB}$. The switching period, the reciprocal of the switching frequency, can be approximated to a linear function in (7) controlled by the feedback voltage $V_{\rm FB}$ in the valley selection mode as depicted in Fig. 4(b) where K is a constant value

$$f(V_{\rm FB}) = K \cdot V_{\rm FB} + C \quad \text{where } C\text{is a constant value.} \tag{7}$$

Then, $t_{\rm dis}$, $I_{s,\rm pk}$, and $t_{\rm on}$ can be expressed as

$$t_{\rm dis} = I_{s\_\rm pk} \cdot \frac{L_P}{V_{\rm out} \cdot N^2} \tag{8}$$

$$I_{s\_\rm pk} = \frac{V_{\rm in}}{L_P} \cdot t_{\rm on} \cdot N \tag{9}$$

$$t_{\rm on} = V_{\rm FB} \cdot \frac{L_P}{V_{\rm in}} \cdot \frac{1}{R_{CS}}. \tag{10}$$

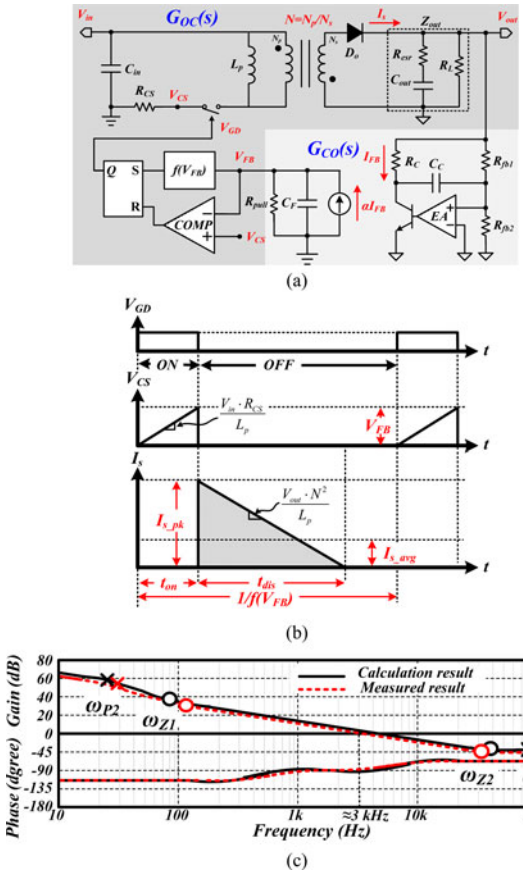

Fig. 15. (a) Equivalent small signal model of the proposed flyback converter. (b) Waveforms of the flyback converter with the DFS technique. (c) Comparison of the derived frequency response and the measured frequency response.

Substituting (8)–(10) into (6), I_{s_avg} can be expressed as the function of the output voltage V_{out}, the feedback voltage V_{FB}, the inductor L_P, and the sensing resistor R_{CS} as shown in

$$I_{s\_\mathrm{avg}} = \frac{(K \cdot V_{\mathrm{FB}}^3 + C \cdot V_{\mathrm{FB}}^2) \cdot L_P}{2 \cdot V_{\mathrm{out}} \cdot R_{CS}^2}. \tag{11}$$

The averaged secondary-side current is, in general, a nonlinear function of the converter voltages and currents. Linearization at the quiescent operating point can derive the small ac current variation of the secondary side as expressed in

$$\hat{I}_{s\_\mathrm{avg}} = a_1 \cdot \hat{V}_{\mathrm{FB}} + a_2 \cdot \hat{V}_{\mathrm{out}} \quad \text{where} \quad \begin{pmatrix} a_1 = \frac{\partial I_{s\_\mathrm{avg}}}{\partial V_{\mathrm{FB}}} = \frac{(3K \cdot V_{\mathrm{FB}}^2 + 2C \cdot V_{\mathrm{FB}}) \cdot L_P}{2 \cdot V_{\mathrm{out}} \cdot R_{CS}^2} \\ a_2 = \frac{\partial I_{s\_\mathrm{avg}}}{\partial V_{\mathrm{out}}} = \frac{-(K \cdot V_{\mathrm{FB}}^3 + C \cdot V_{\mathrm{FB}}^2) \cdot L_P}{2 \cdot V_{\mathrm{out}}^2 \cdot R_{CS}^2} \end{pmatrix}. \tag{12}$$

The small ac current variation at the secondary side flowing through the impedance Z_{out} determines the perturbation of V_{out} as expressed in

$$\hat{V}_{\mathrm{out}} = \hat{I}_{s\_\mathrm{avg}} \cdot Z_{\mathrm{out}} = \left(a_1 \cdot \hat{V}_{\mathrm{FB}} + a_2 \cdot \hat{V}_{\mathrm{out}}\right) \cdot Z_{\mathrm{out}}. \tag{13}$$

Therefore, the control-to-output transfer function $G_{CO}(s)$ is depicted in (14), which simply contains one zero and one pole

$$G_{CO}(s) = \frac{\hat{V}_{\mathrm{out}}}{\hat{V}_{\mathrm{FB}}} = \frac{Z_{\mathrm{out}} \cdot a_1}{1 - Z_{\mathrm{out}} \cdot a_2} = \frac{a_1}{1/R_L - a_2} \cdot \frac{1 + sC_{\mathrm{out}}R_{\mathrm{esr}}}{1 + \frac{sC_{\mathrm{out}}(1 + R_{\mathrm{esr}}(1/R_L - a_2))}{1/R_L - a_2}}. \tag{14}$$

C_{out} and its equivalent series resistor (ESR) R_{esr} contribute one ESR zero at high frequencies. And the pole can be seen as the combination of C_{out} and the equivalent loading resistance R_L. As illustrated in Fig. 15(a), TL431 and optocoupler acting like the error amplifier and voltage-to-current transconductance amplifier, respectively, in the feedback loop. Thus, the output-to-control transfer-function $G_{OC}(s)$ can be derived in

$$G_{OC}(s) = \frac{\hat{V}_{\mathrm{FB}}}{\hat{V}_{\mathrm{out}}} = \frac{\alpha R_{\mathrm{pull}}}{R_C} \cdot \frac{(1 + sR_{fb1}C_C)}{sR_{fb1}C_C(1 + sR_{\mathrm{pull}}C_F)}. \tag{15}$$

Hence, the proportion integral compensator with a transfer function $G_{OC}(s)$ that contains two poles and one zero ω_{Z1} can used as the compensator. One of the compensation poles is at origin and the other is at high frequencies. Besides, the compensation zero ω_{Z1} in $G_{OC}(s)$ should be close to the pole ω_{P2} in $G_{CO}(s)$ to achieve pole-zero cancellation by choosing appropriate passive components. Thus, the pole in $G_{OC}(s)$ at the origin becomes the dominant pole of the whole system. The high-frequency compensation pole ω_{P1} in $G_{OC}(s)$ is used to alleviate the effect of the high-frequency ESR zero ω_{Z2} for better high-frequency noise rejection. After the compensation, the system transfer function $T(s)$ is shown in

$$T(s) = G_{CO}(s)G_{OC}(s) = \frac{\alpha R_{\mathrm{pull}} a_1}{R_C\,(1/R_L - a_2)} \cdot \frac{1 + sC_{\mathrm{out}}R_{\mathrm{esr}}}{sR_{fb1}C_C(1 + sR_{\mathrm{pull}}C_F)}. \tag{16}$$

The bandwidth is designed about 3 kHz which is far away from the switching frequency as shown in Fig. 15(c).

V. Experimental Results

The proposed flyback converter with the DFS technique and the CCS circuit was implemented in 0.5 μm 500 V UHV process. The chip micrograph with an active area of 3.6 mm^2 is shown in Fig. 16(a). The prototype is shown in Fig. 16(b). The range of input ac source is 90–264 $\mathrm{V_{AC}}$ and V_{out} is 19 V. The primary inductance of transformer is 700 μH. The winding ratio L_p: L_s: L_a is 35T: 5T: 4T. The error amplifier and optocoupler are TL431 and PC817, respectively. Detailed design specifications are listed in Table I.

The estimated frequency response is consistent with the calculated frequency response as shown in Fig. 15(c). Fig. 17 shows ultrahigh-voltage startup mechanism provided by the CCS circuit. I_{HV} remains constant current of 1.2 mA until V_{DDH} is higher than 16 V. The autorecovery function provided by the CCS circuit with the UVLO is shown in Fig. 18 by shorting V_{out} to ground to trigger the restart protection. Fig. 5 shows the correct function of the autorecovery.

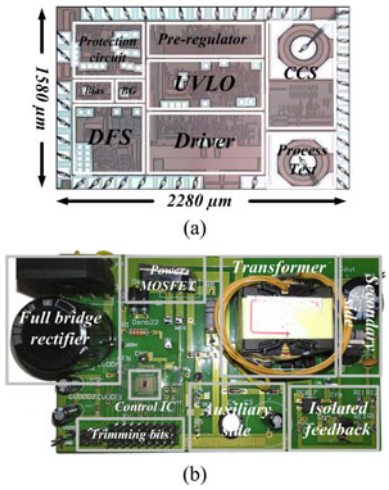

Fig. 16. (a) Chip micrograph. (b) Prototype of the QR-PWM flyback converter.

TABLE I
DESIGN SPECIFICATIONS

Technology	0.5 μm 500V UHV
Input line voltage range (V_{ac})	90~264 V (rms value)
Output voltage (V_{out})	19 V
Primary inductor (L_p)	700 μH
Primary winding turns (N_p)	35T
Secondary winding turns (N_s)	5T
Auxiliary winding turns (N_a)	4T
Output capacitor (C_{out})	1000 μF / 35 V
Minimum switching frequency (f_{SW})	2 kHz-125 kHz
Power conversion efficiency	Max 92% (80 W, V_{AC}=90 V)
Output power	100 W
Chip area (with test pads)	1580 μm × 2280 μm

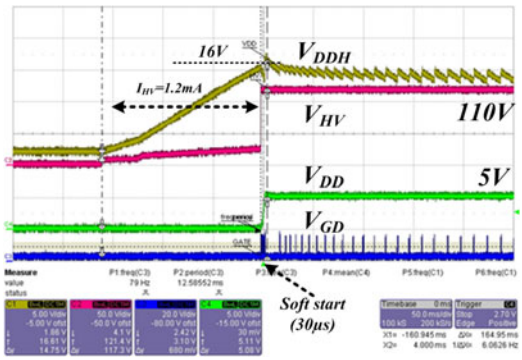

Fig. 17. Waveforms of the CCS circuit with the UVLO circuit. (at $V_{\rm AC}$ = 110 V).

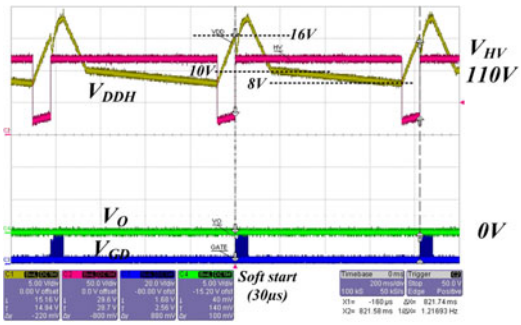

Fig. 18. Waveforms of the autorecovery function (at $V_{\rm AC}$ = 110 V).

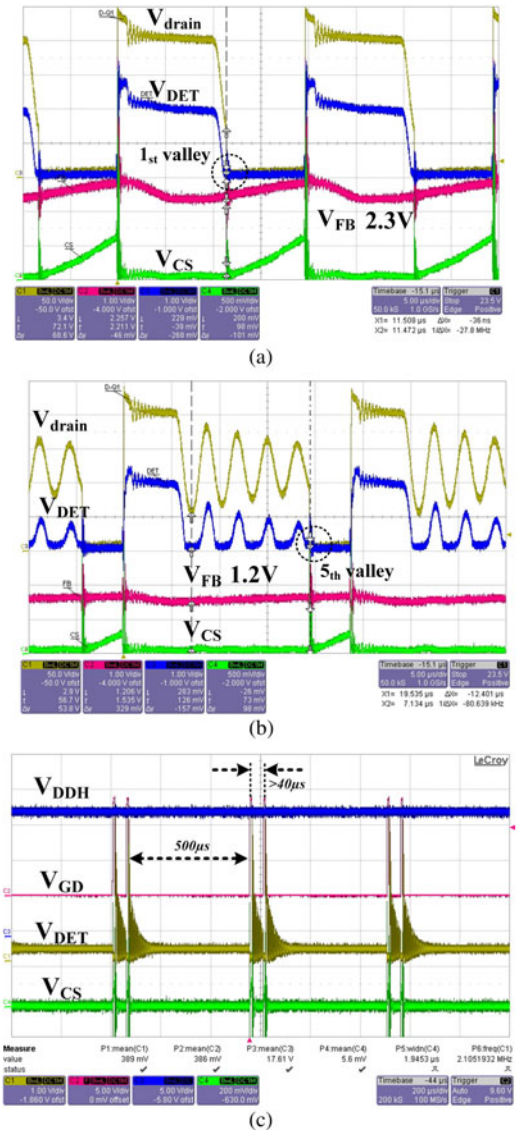

Fig. 19. Measurement results of the DFS under different load conditions (at $V_{\rm AC}$ = 110 V and $V_{\rm out}$ = 19 V). (a) $I_{\rm LOAD}$ = 5 A. (b) $I_{\rm LOAD}$ = 1 A. (c) $I_{\rm LOAD}$ = 100 mA.

The proposed DFS that operates with different loads is depicted in Fig. 19. Fig. 19(a) shows the first valley turns on the power MOSFET at the heavy load of 5 A. The fifth valley is chosen to turn ON the power MOSFET at the load of 2 A in Fig. 19(b). Obviously, the decreased switching frequency can effectively improve the efficiency. Once the system has an ultralight load, the system enters the Green mode with an off time of 500 μs as shown in Fig. 19(c). Comparison of conversion efficiency between conventional and proposed methods is shown in Fig. 20. The performances make great strides especially at light loads. The efficiency can achieve about 85% at light load of 5 W when $V_{\rm AC}$ is 90 V, and peak efficiency is near 92% at load of 80 W when $V_{\rm AC}$ is 264 V.

The comparisons between the proposed flyback converter and prior arts are listed in Table II. The efficiency is improved especially at light load because of the proposed DFS and CCS

TABLE II
COMPARISONS BETWEEN THE PROPOSED FLYBACK CONVERTER AND PRIOR ARTS

	This work	[13]	[25]	[26]
Input voltage (V_{rms})	AC 90-264	AC 90-230	DC 100	DC 100
Operating Mode	DCM/CRM/GM	DCM/CCM	DCM/CCM	DCM
Output capacitance (F)	1000 μ	470 μ	940 μ	470 μ
Output voltage (V)	19	19	15	12
Maximum Output power (W)	100	140	150	150
Switching frequency (Hz)	2-125 k	60 k	50 k	80 k
Circuit Implement	Fully Integrated	System Level	System Level	System Level
Efficiency (Power>80W)	92% (90 V, 80 W)	90.5% (115 V, 80 W)	89.7% (100 V, 80 W)	85% (100 V, 80 W)
Efficiency (Power<15W)	85% (90 V, 5 W)	N/A	71%(100 V,15 W)	65%(100 V, 15 W)

*GM stands for Green mode.

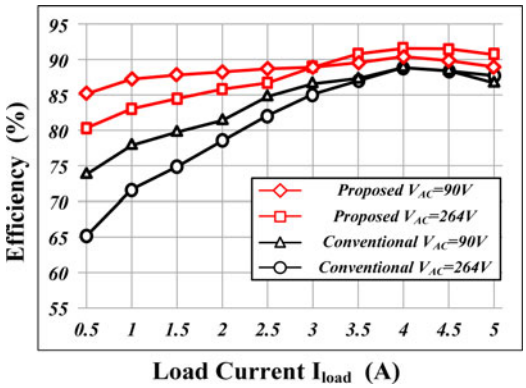

Fig. 20. Power conversion efficiency of the proposed and conventional methods with the input ac source $V_{\rm AC} = 90$ and 264 V.

methods. Consequently, the conversion efficiency is better than those of the prior arts.

VI. CONCLUSION

To achieve a high efficiency flyback converter with minimized external components, the proposed DFS technique dynamically chooses one suitable valley voltage in the resonance to extend the switching period. Therefore, the converter automatically switches to the DCM operation and thus reduces the switching frequency for higher efficiency at light loads. Especially, the system operating in the Green mode can further reduce power loss at ultralight loads. Besides, the CCS circuit can improve efficiency since the leakage path of the startup circuit can be completely turned OFF. The test chip fabricated in VIS 0.5 μm 500 V UHV process occupies an active silicon area of 3.6 mm^2. The peak efficiency and the light-load efficiency are 92% and 85%, respectively.

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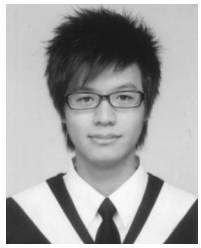

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