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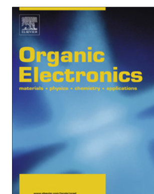

Achieving good bias stress reliability in organic transistor with vertical channel

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ABSTRACT

Unlike organic field-effect transistor with accumulated channel at dielectric/semiconductor interface, vertical organic transistor exhibits bulk channel current and hence performs good bias stress reliability. Adding self-assemble-monolayer to treat vertical channel can further modulate the charge-trapping surrounding the base electrode and hence influence the bias stress reliability. During 4300-s positive/negative bias stresses, stable output current and on/off ratio are demonstrated by using octadecyltrichlorosilane (OTS)-passivated vertical channel. The good reliability together with the low operation voltage and the high output current make vertical organic transistors capable of driving organic light emitting diode.

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1. Introduction

Active matrix organic light emitting diodes (OLED) displays have attracted lots attentions in recent years. One critical issue for developing AM-OLED is the bias-stress effect (BSE) of the driving transistor [1,2]. The driving transistor needs high enough on-current to obtain sufficient light efficiency in OLED. When driving transistor is continuously operated in on state, the threshold voltage shifts and driving current decreases along with the operation time [1–3]. There are several kinds of thin film transistor (TFT) technologies like amorphous silicon (a-Si) TFT [4], low temperature polycrystalline silicon (LTPS) TFT [5], oxide TFT [6], and organic field effect transistor (OFET), etc. OFETs particularly have advantages of low-cost, flexible, and large-area solution process. However, BSE is still a challenge in OFETs [7]. When OFET is operated, accumulated holes in channel region generate defect states to trap charge. The charge trapping may also related to the –OH groups on dielectric interface and the absorbed oxygen/water molecules in dielectric and semiconducting layers [7–9]. Besides, due to the low carrier mobility of organic materials, the output current in OFET is usually too low to drive OLED.

To greatly improve the output current by reducing channel length, various vertical channel organic transistors were reported [10–12]. In vertical transistors, the channel length depends on the thickness of the semiconductor thin film. Hence, low operation voltage and high current output can be expected. However, there is still no report to investigate the bias stress reliability in vertical organic transistors. In this work, we study the BSE in vertical organic transistor. With poly(3-hexylthiophene) (P3HT) as the channel material and with hydrophilic dielectric material, vertical organic transistor exhibits a greatly improved bias stress reliability than its OFET counterpart. Moreover, we use different types of self-assembled monolayers (SAMs) to treat the vertical channel and study the effect of SAM on BSE reliability. Using octadecyltrichlorosilane (OTS-18) to treat the base can effectively reduce trap states between base electrode and organic semiconducting layer and hence obtain a further improved BSE reliability.

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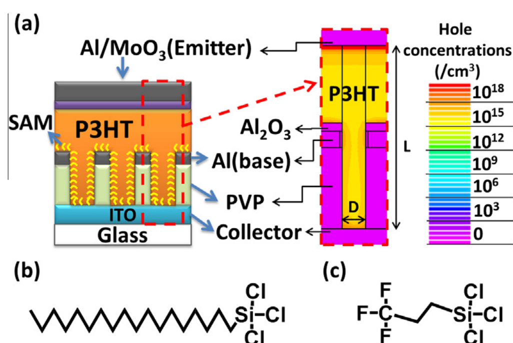

Fig. 1. (a) (left) the schematic diagrams of SCLT. (right) 2-dimensional hole concentration distribution in vertical channel when SCLT is operated in *ON* state, (b) the chemical structure of OTS-18, and (c) the chemical structure of FPTS.

The vertical organic transistor used in this work is space-charge limited transistor (SCLT), which is one of the promising devices that exhibits high output current of 3–50 mA/cm^2 at low operation voltage [11]. The operation principle of SCLT is like a solid-state triode tube. As shown in Fig. 1(a), by using p-type channel material, holes are injected from emitter electrode into vertical channel and arrive at collector electrode. The porous base electrode plays the role of controlling the potential profile inside the openings so the on-state and off-sate of the vertical channel is controlled.

2. Experimental

Fig. S1 shows the schematic fabrication process of SCLT. First, we prepared an indium tin oxide (ITO) glass substrate as the collector (C). Cross-linkable poly(4-vinyl phenol) (PVP) (Mw approx. 20000, Aldrich) and cross-linking agent poly(melamine-co-formaldehyde) (PMF) were dissolved in propylene glycol monomethyl ether acetate (PGMEA) with a PVP:PMF mass ratio of 11:4. The solution was then spin-coated onto the ITO glass substrate and annealed at 200 °C for 1 h to form a 200-nm-thick insulting layer. Then, a thin poly(3-hexylthiophene) (P3HT) (RR >98.5%, Rieke Metals Inc.) layer was spin-coated on the PVP layer to modify the surface energy. The substrate was spin-rinsed with p-xylene to increase the P3HT surface polarity. After that, negatively charged polystyrene (PS) spheres with diameter as 100 nm were adsorbed on the substrate. After evaporating a 40-nm-thick Al metal and removing the PS spheres by a Scotch tape, a grid-like Al metal is formed and served as the base (B). With grid-like Al as the mask, O_2 plasma at 100 W was applied to etch the bare PVP for 10 min to form deep nanopores. After treating the template by SAM, P3HT dissolved in chlorobenzene was spin-coated or blade-coated onto the substrate and annealed at 200 °C for 10 min to form a 450-nm-thick active layer. Finally, a top electrode containing thin molybdenum oxide (MoO_3) and Al was evaporated to serve as the emitter (E). Two kinds of SAMs, octadecyltrichlorosilane (OTS, Fig. 1(b)) and trichloro(3,3,3-trifluoropropyl)silane (FPTS, Fig. 1(c)), were added onto template by 2-h-immersion in 1 mM SAM solution in anhydrous toluene with a following 1-h annealing at 200 °C.

All the electrical measurement was carried out in a glove box with N_2 environment to simulate the condition with good packaging. We used HP E4145B semiconductor parameter analyzer to measure the electric characteristics and the bias-stress effect of SCLT. Negative base bias ($V_B = -1.0$ V) and positive base bias ($V_B = +1.0$ V) were applied for 4300 s; during this time, collector and emitter

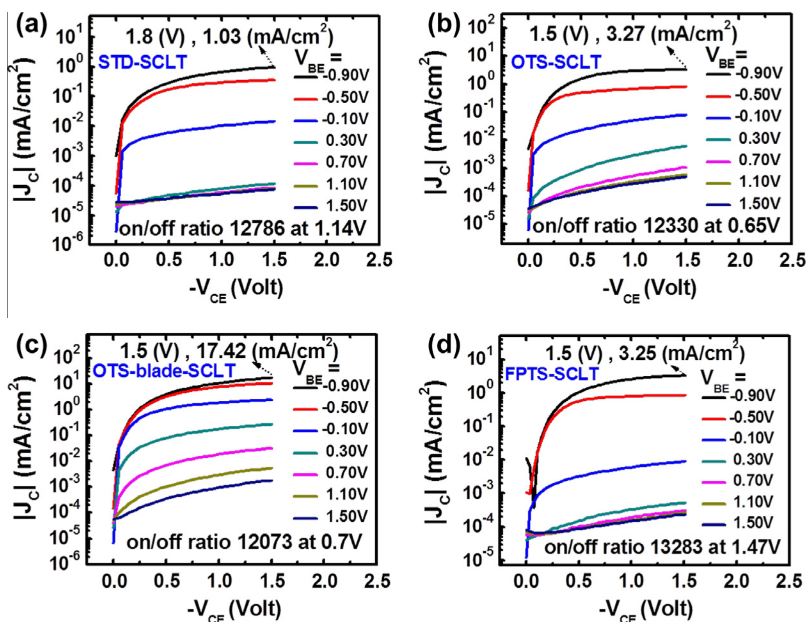

Fig. 2. The original J_{CE}–V_{CE} characteristics for (a) STD SCLT (without SAM treatment), (b) OTS-SCLT (with OTS-18 treatment and spin-coated P3HT layer), (c) OTS-blade-SCLT (with OTS-18 treatment and blade-coated P3HT layer), and (d) FPTS-SCLT (with FPTS treatment).

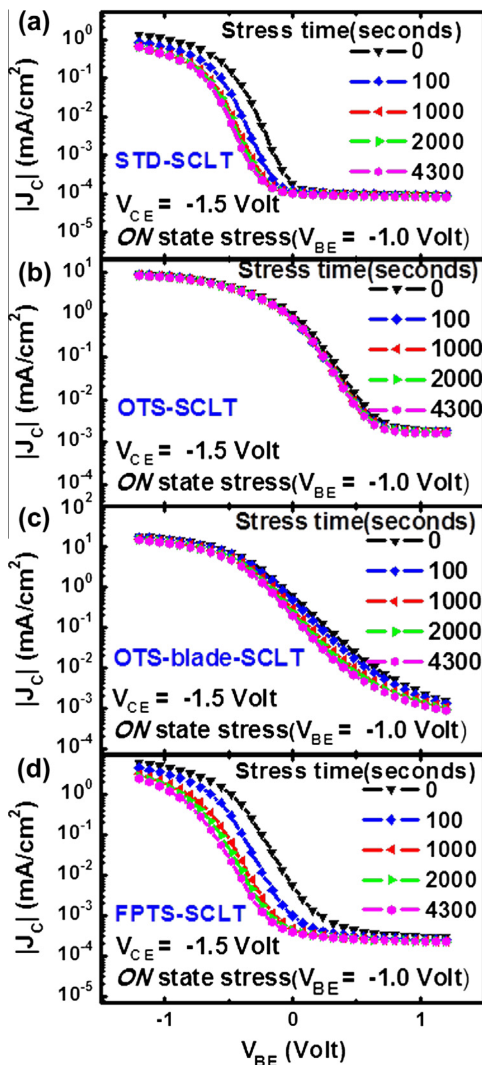

Fig. 3. The transfer characteristics under on-state bias stress for (a) STD SCLT (without SAM treatment), (b) OTS-SCLT (with OTS-18 treatment and spin-coated P3HT layer), (c) OTS-blade-SCLT (with OTS-18 treatment and blade-coated P3HT layer), and (d) FPTS-SCLT (with FPTS treatment).

were biased at $V_C = 0$ V and $V_E = -1.5$ V respectively. Threshold voltage is defined according to the method shown in Fig. S2.

3. Results and discussions

The collector current density (J_{CE}) as a function of collector voltage (V_{CE}) with various base voltage (V_{BE}) for STD-SCLT, SCLT treated by OTS (OTS-SCLT), and SCLT treated by FPTS (FPTS-SCLT) are shown in Fig. 2(a, b, and d), respectively. For OTS-SCLT, we also use blade coating to form P3HT layer. In our previous report, the output current can be increased by using the blade coating (without spinning) process to improve the pore filling and chain packing [11]. The J_{CE}–V_{CE} curve of OTS-SCLT with blade-coated P3HT (i.e. OTS-blade-SCLT) is shown in Fig. 2(c). All four transistors in Fig. 1 exhibit on/off current ratio larger than 12,000.

Then, on-state bias stress (negative bias stress) effects of STD-SCLT, OTS-SCLT (spin-coated P3HT and blade-coated P3HT), and FPTS-SCLT are investigated by plotting the collector current density (J_{CE}) as a function of base voltage (V_{BE}) with various stress time in Fig. 3(a, b, c and d), respectively. In STD-SCLT, under negative bias stress, transfer characteristics shifts about −0.2 V after 4300-s stress. The threshold voltage (Vth) shifts toward more negative voltages as shown in Fig. 3(a). For OFET with poly(3-hexylthiophene) (P3HT) as the channel material and with hydrophilic dielectric material (e.g. SiO_2 with –OH groups), a 3–10 V threshold voltage shift is usually observed after 4000-s on-state stress [13]. The significantly improved bias stress reliability in P3HT SCLT is explained by its channel carrier distribution. When SCLT is operated in ON state, the two-dimensional hole carrier distribution in the vertical channel is simulated by using TCAD Silvaco [parameters provided in Ref. [14] and is shown in Fig. 1(a). Clearly, channel current flows through the whole P3HT bulk. The good bias-stress reliability in SCLT may be attributed to the bulk conduction mechanism. For OFET, channel is formed at dielectric/semiconductor interface. High density carriers are accumulated in channel when OFET is turned on. Previous report tells that, in OFET, BSE is strongly related to the trapped charges at dielectric/semiconductor interface [7]. Moreover, the defect state creation is enhanced by high carrier concentration [15]. Here, in SCLT, current flows through the whole bulk region in the vertical channels. Without the accumulated high concentration carriers at semiconductor/dielectric or semiconductor/base interface, the defect-state generation during operation may be suppressed. Also, the bulk current may be less sensitive to the trapped charge at semiconductor/dielectric interface. Hence, an improved BSE in SCLT is achieved.

With OTS treatment, the bias stress effect in SCLT can be further suppressed as shown in Fig. 3(b and c). Almost no curve shift is observed for OTS-SCLT with spin-coated P3HT after 4300-s negative-bias stress. For OTS-SCLT with blade-coated P3HT, a slight curve shift is observed. For FPTS-SCLT (Fig. 3(d)), the curve shift is severe and is even larger than that in STD-SCLT. The influence of SAM on BSE in SCLT will be discussed as follows.

To observe the on-state BSE more clearly, threshold voltage shift is plotted as a function of stress time for all devices in Fig. 4(a). Standard deviation is calculated from three independent devices. We clearly observe that, even with a certain device-to-device variation, OTS-SCLTs indeed exhibit greatly suppressed BSE than STD-SCLTs. On current (measured at $V_{BE} = -1$ V and $V_{CE} = -1.5$ V) is also plotted as a function of stress time in Fig. 4(b). When STD-SCLT and FPTS-SCLT suffers from output current degradation during on-state stress, OTS-SCLT can deliver rather stable output current. Moreover, when P3HT is coated onto OTS-treated device by using blade coating (OTS-blade-SCLT), output current is enhanced. The BSE stability of OTS-blade-SCLT is a bit inferior to that in OTS-SCLT, but is much better than that in STD-SCLT. The off-state stress effect is also evaluated by applying $V_{BE} = 1$ V

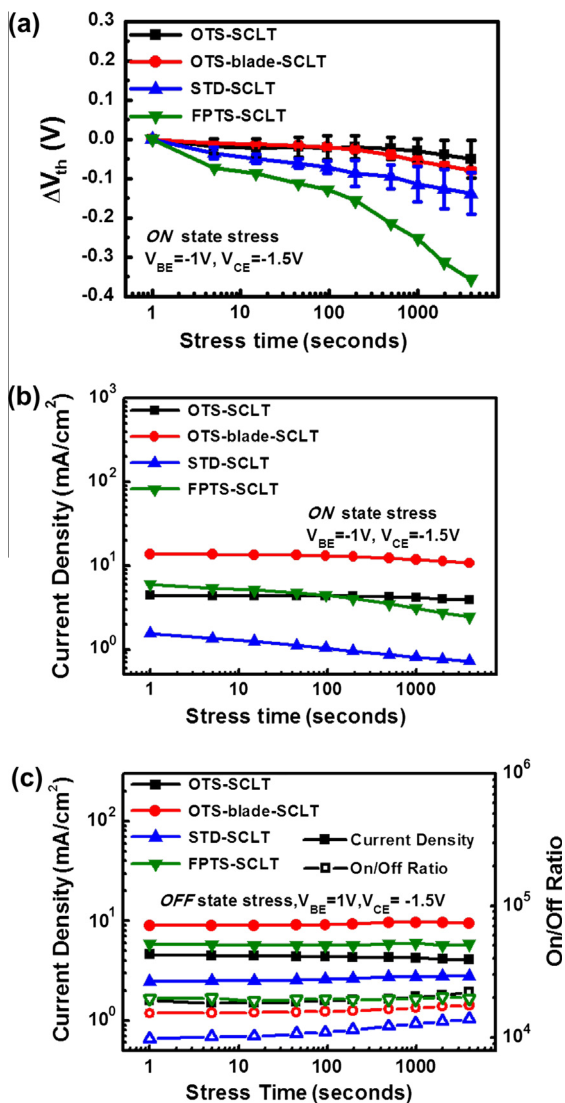

Fig. 4. (a) Threshold voltage shift and (b) on state current density as a function of on-state stress time. (c) Output current density and on/off current ratio as a function of off-state stress time.

and $V_{CE} = -1.5$ V. The on current and the on/off current ratio are plotted as a function of off-state-stress time in Fig. 4(c). All devices exhibit stable output current and stable on/off ratio under off-state stress.

In our previous work, we demonstrated that OTS-SCLT exhibits better nanopore filling and better P3HT chain packing then STD-SCLT [11]. Here, we assume that the improved BSE in OTS-SCLT is also related to the enhanced nanopore filling and chain packing. Particularly, the defect state density in conventional OFET is known to be related to molecular packing at organic/insulator interface. Using SAM treating insulator can improve the P3HT chain packing in P3HT OFET and reduce the interface defect [16]. Also, in OFET, device with OTS-modified SiO_2 dielectric exhibit better bias stress reliability than device with bare SiO_2 dielectric layer [17]. Here in the vertical channel SCLT, we propose that the BSE is due to the charge trapping at base/organic interface. During on-state bias stress, negative base bias attracts hole and hence creates hole trapping surrounding the base electrode. (It is noted that base current density is not increased after stress.)

The proposed mechanism is plotted in Fig. 5. For STD-SCLT, as shown in Fig. 5(a), defect states exist on interface between base and P3HT. Here a thin AlO_x layer is used to represent the surface oxidation of base electrode when we use oxygen plasma to etch through the PVP layer. When SCLT is turned on, hole current flows vertically through P3HT channel. Defect states surrounding base then capture holes to form positively-charged sites. To overcome the influence of the trapped positive charge, we hence need to apply a more negative base bias to turn on SCLT. The formation of defect states surrounding base electrode may be due to several reasons. The poor chain packing and poor pore filling may create defective structure sites. Also, the hydroxyl groups on AlO_x surface may serve as trapping centers to capture holes [18]. Many research groups have reported that using self-assemble monolayer can effectively eliminate the hydroxyl groups and hence reduce the interfacial trapping centers. In our work, when using OTS to treat the substrate, the hydroxyl groups are eliminated by OTS as shown in Fig. 5(b) [19,20]. Also, improved pore filling and chain packing suppress the formation of defective film. The vertical channel carriers hence will not influenced by hole-trapping phenomenon. The base electrode can also maintain its function without being influenced by the surrounding trapped charges.

Improved pore filling and suppressed hole trapping are proposed to explain the good bias stress reliability in OTS-SCLT and OTS-blade-SCLT. On the other hand, for FPTS-SCLT, poor pore filling is observed to explain the severe threshold voltage shift during on-state stress. The SEM image of the cross-sectional view of FPTS-SCLT is shown

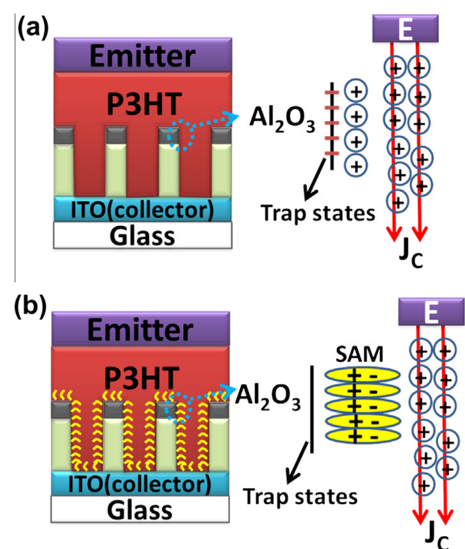

Fig. 5. The schematic diagrams of negative bias stress effect with (a) no SAM treatment device and (b) SAM treatment device.

in Fig. S3. It is found that many vertical pores are empty, P3HT only form a thin film above the textured substrate. The poor pore filling is due to the strong hydrophobic property after FPTS treatment. In some tests, the dewetting of P3HT on FPTS-treated substrate even causes difficulty to form uniform P3HT film. According to previous reports, using fluorinated self-assemble monolayer or fluorine-rich polymer to treat the substrate can effectively prevent the adsorption of water molecules and hence minimize the trap formation [21]. Here, we propose that the poor bias stress reliability of FPTS-SCLT is caused by the dewetting problem and hence the poor pore filling.

4. Conclusions

In summary, we found that P3HT vertical transistor exhibits a much better BSE than P3HT OFET. For OFET, channel carriers accumulated in semiconductor/insulator interface are sensitive to the interface trapping states. Here in our work, we demonstrated that relatively good bias-stress reliability can be obtained in SCLT. For standard P3HT SCLT, 4300-s bias stress only generates a very small threshold voltage shift (<0.2 V). The good reliability may be explained by the bulk-dominated current flow since carriers flow through vertical bulk channels, not accumulate at interfaces. The small threshold voltage shift in standard SCLT can be further suppressed by adding OTS on base electrode. We proposed that small amount of charges are trapped at base/semiconductor interface to generate the small threshold voltage shift. Treating the interface by OTS can suppress the charge trapping and eliminate the small threshold voltage shift. At the same time, OTS-treatment enhances the output current of SCLT. With the improved output current and good bias-stress reliability, OTS-treated SCLT may be used for OLED driving.

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.orgel.2014.04.007.

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