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Improved performances in low-voltage-driven InGaZnO thin film transistors using a SiO_2 buffer layer insertion

Z.W. Zheng · Y.C. Chen

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Abstract In this paper, we report the device characteristics of indium gallium zinc oxide (IGZO) thin film transistors (TFTs) with high-κ lanthanum aluminate ($LaAlO_3$) based gate insulators. The IGZO TFT with single $LaAlO_3$ gate insulator has an operation voltage as low as 1.5 V but suffers a low on-off-state drive current ratio (I_{on}/I_{off}) of 1×10^3, a large subthreshold swing (*SS*) of 0.405 V/dec and a small field effect mobility (μ_{FE}) of 0.84 cm^2/V sec. Inserting a SiO_2 buffer layer between IGZO active channel layer and $LaAlO_3$ gate insulator results in a reduced effective dielectric constant but with significant improved characteristics including a high I_{on}/I_{off} of 6.2×10^4, a small *SS* of 0.113 V/dec and a large μ_{FE} of 5.2 cm^2/V sec. Such good performances can be attributed to the lowered gate leakage and reduced interface trap issue owing to the smooth SiO_2 buffer layer insertion.

1 Introduction

At the rapid growth of flat panel display market, oxide thin film transistors (TFTs) [1–14] have attracted much attention as emerging devices that exhibit higher mobility compared to the conventional amorphous or polycrystalline silicon TFTs [15–17] and organic TFTs [18–21]. Among various oxide TFTs, ZnO-based TFTs [1–14], especially indium gallium zinc oxide (IGZO) TFTs [4–14], have been considered as potential candidates for flexible display applications, due to their advantages of low production cost, high mobility, excellent uniformity, good optical transparency, etc. However, the currently developing IGZO TFTs still suffer large operation voltage and low device mobility. In addition, low threshold voltage (V_t) and small subthreshold swing (*SS*) are also needed for high-speed operation. To solve these issues, improving the properties of active channel material in the fabrication process [7–9], such as IGZO thickness, channel composition, provides an alternative solution. Apart from the active channel layer material, the insulating material is also of great significance for high-performance TFTs. It is well known that gate dielectrics with high dielectric constant and small surface roughness allow the TFTs to have low operation voltages, because the high carrier density in the active channel layer could be induced at a relatively low voltage bias compared to traditional dielectrics and polymer insulators. Therefore, incorporating high-κ gate materials into TFTs has been widely applied to improve the device performances [17–19].

In this paper, we report the device performances of IGZO TFTs with high-κ lanthanum aluminate ($LaAlO_3$) [17–19, 22] based gate dielectrics. Due to the high dielectric constant, large energy bandgap and high thermal stability of $LaAlO_3$ dielectric, low threshold voltage (V_t) and low operation voltage can be achieved in the $LaAlO_3$-based TFTs. However, $LaAlO_3$ dielectric still suffers interfacial issue that degrades the electron mobility as reported in the literature [22]. To solve this problem, using a SiO_2 buffer layer inserted between the IGZO active channel layer and $LaAlO_3$ gate insulator, improved device performances are achieved as compared to the TFTs with single $LaAlO_3$ gate dielectric, including a higher I_{on}/I_{off} of 6.2×10^4, a smaller *SS* of 0.113 V/dec and a larger μ_{FE} of 5.2 cm^2/V sec. Such good characteristics can be attributed to lowered gate leakage cur-

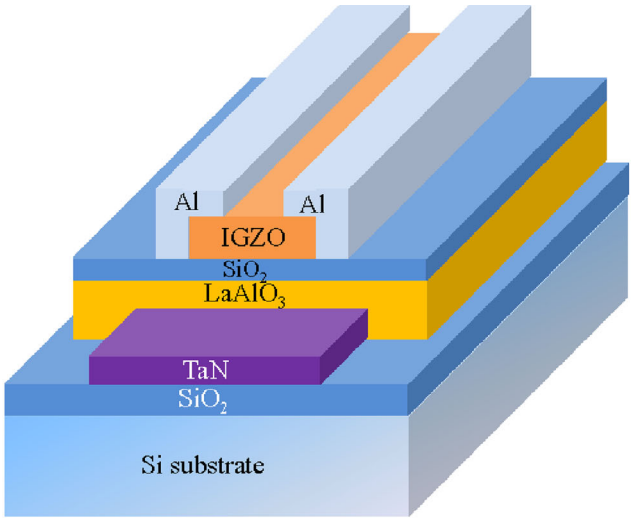
Z.W. Zheng (✉)
Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
e-mail: wei7553@hotmail.com

Y.C. Chen
Institute of Photonic System, National Chiao Tung University, Hsinchu 300, Taiwan

rent and reduced interfacial issue with a SiO_2 buffer layer insertion [10–12, 20, 21, 23]. The present results demonstrate that IGZO TFTs with stacked $LaAlO_3/SiO_2$ gate dielectrics show high potential for future high-speed and low-power applications.

2 Experimental details

Figure 1(a) and (b) shows the schematic structure and photograph of the IGZO TFT with device micrograph in the inset, respectively. The top-contact bottom-gate type IGZO TFTs were prepared on the 300-nm thick insulating SiO_2 grown on 4-inch silicon substrates with a shadow mask process. A 50-nm thick TaN bottom gate (G) electrode was formed by physical vapor deposition (PVD) and patterned. Then, a 30-nm thick $LaAlO_3$ and 10-nm thick SiO_2 were deposited by e-beam evaporation at room temperature, followed by annealing in O_2 ambient at 400 °C to improve the gate oxide properties. Subsequently, a 40-nm thick IGZO active layer was deposited using dc reactive sputtering from an IGZO target under Ar ambient mixed with O_2 gas. Finally, 300-nm thick Al was thermally coated to form source (S) and drain (D) electrodes, followed by N_2 sintering at 300 °C to reduce contact resistance. The devices have a channel width (W) of 500 µm and a channel length (L) of 50 µm. The metal–insulator–metal (MIM) capacitors of gate dielectrics were also fabricated side-by-side to characterize the gate capacitance and leakage current. For comparison, the TFT devices without SiO_2 buffer layer were also fabricated as control samples. The gate insulators were characterized by atomic force microscopy (AFM) analysis. The electrical characteristics of TFT devices were measured at room temperature using HP4156C semiconductor parameter analyzer.



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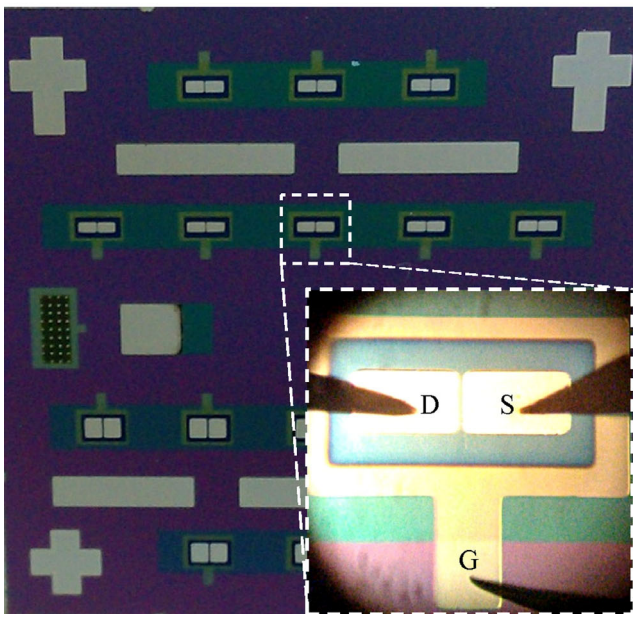

b

Fig. 1 (**a**) Schematic structure and (**b**) photograph of the IGZO TFT with device micrograph in the *inset*

3 Results and discussion

Figure 2 shows the capacitance–voltage (C–V) characteristics of the Al/[with and without SiO_2 buffer layer]/$LaAlO_3$/TaN gate capacitors on the same substrate, with the current density–voltage (J–V) characteristics in the inset. A high capacitance density for gate dielectrics is needed to induce a large carrier density at a relatively low operation voltage. The high capacitance density of 62 and 23 fF/µm^2 measured at 100 kHz is obtained for the MIM capacitors without and with SiO_2 buffer layer, respectively, as shown in Fig. 2.

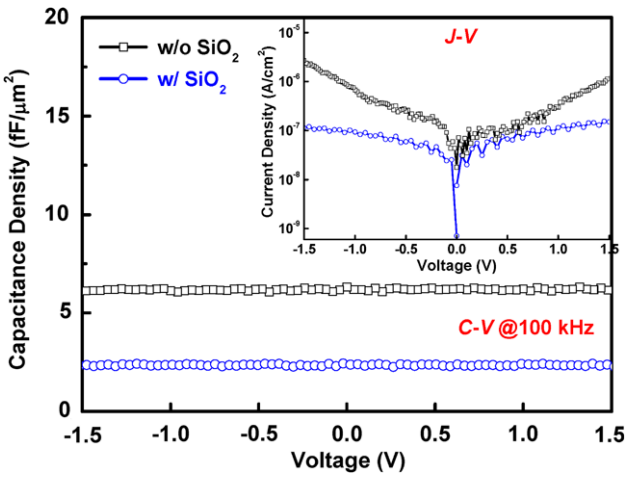

Fig. 2 C–V characteristics of Al/[with and without SiO_2 buffer layer]/$LaAlO_3$/TaN gate capacitors on the same substrate, with J–V characteristics in the *inset*

It indicates the equivalent oxide thickness (EOT) of ~5.5 and ~15 nm for single $LaAlO_3$ and stacked $SiO_2/LaAlO_3$ gate dielectrics, respectively. The high dielectric constant of ~21 can be extracted for $LaAlO_3$ dielectric, while the reduced effective dielectric constant of ~10.4 is obtained for $SiO_2/LaAlO_3$ gate stack. Although the insertion of SiO_2 buffer layer decreases effective gate capacitance and effective dielectric constant, the structure reduces the gate leakage current density (1.1×10^{-7} A/cm^2 @ −1.5 V) further by more than one order of magnitude as compared to the single $LaAlO_3$ structure (2.7×10^{-6} A/cm^2 @ −1.5 V) in the inset of Fig. 2. This smaller gate leakage by introducing a SiO_2 buffer layer could reduce the off-current level in TFT devices and improve the I_{on}/I_{off}, indicating that the insertion of SiO_2 buffer layer is a powerful solution for lowering off-state power [10–12, 20, 21, 23], in contrast to single insulator.

Since the surface morphology of the gate dielectrics is very critical to device performances [12–14, 21], the surface roughness of the $LaAlO_3$ gate insulators on bottom TaN gate without and with SiO_2 buffer layer was examined by AFM analysis, as shown in Fig. 3(a) and (b), respectively. Smooth surfaces of single $LaAlO_3$ and stacked $SiO_2/LaAlO_3$ dielectrics with root mean square (RMS) roughness of 0.572 and 0.590 nm are obtained, respectively. The difference in RMS roughness between single $LaAlO_3$ and $SiO_2/LaAlO_3$ stack is just 0.018 nm, which is much smaller than atomic scale. It indicates that there is no degraded roughness after the deposition of SiO_2 buffer layer. Moreover, the SiO_2 buffer layer prevents the carriers moving into the gate dielectric, due to the lager conduction band offset (ΔE_c) of 4.3 eV between SiO_2 and IGZO channel as compared to that of 2.1 eV between $LaAlO_3$ and IGZO channel [24–26], as shown in the energy band diagram in Fig. 4. This smooth surface with proper ΔE_c as a barrier between the gate dielectric and channel is preferred and favorable to be flat gate stack to prevent gate leakage, especially for bottom-gate TFT structures.

Figures 5(a) and (b) displays the output I_d–V_d and transfer I_d–V_g characteristics of the IGZO TFT without SiO_2 buffer layer, respectively. This TFT device behaves as in enhancement mode with good saturation characteristics and can be operated under the voltage bias as low as 1.5 V in Fig. 5(a), indicating that incorporating high-κ $LaAlO_3$ dielectric can give an advantage of lowering the operation voltage. From the measured results, the IGZO TFT with single $LaAlO_3$ insulator shows a low V_t of 0.36 V extracted from the linear $I_d^{1/2}$–V_g curve in Fig. 5(b) but suffers a low I_{on}/I_{off} of 1×10^3, a large SS of 0.405 V/dec, which can be calculated from I_d–V_g curve in Fig. 5(b). Besides, a small μ_{FE} of 0.84 cm^2/V sec is obtained according to the extraction from a gradual channel approximation in the linear region using the equation of $\mu_{FE} = (\partial I_d/\partial V_g) \cdot (L/W)/(V_d \cdot C_g)$, where I_d, V_d, V_g and C_g are the drain current, drain voltage, gate voltage and gate insulator capacitance per unit area, respectively [27].

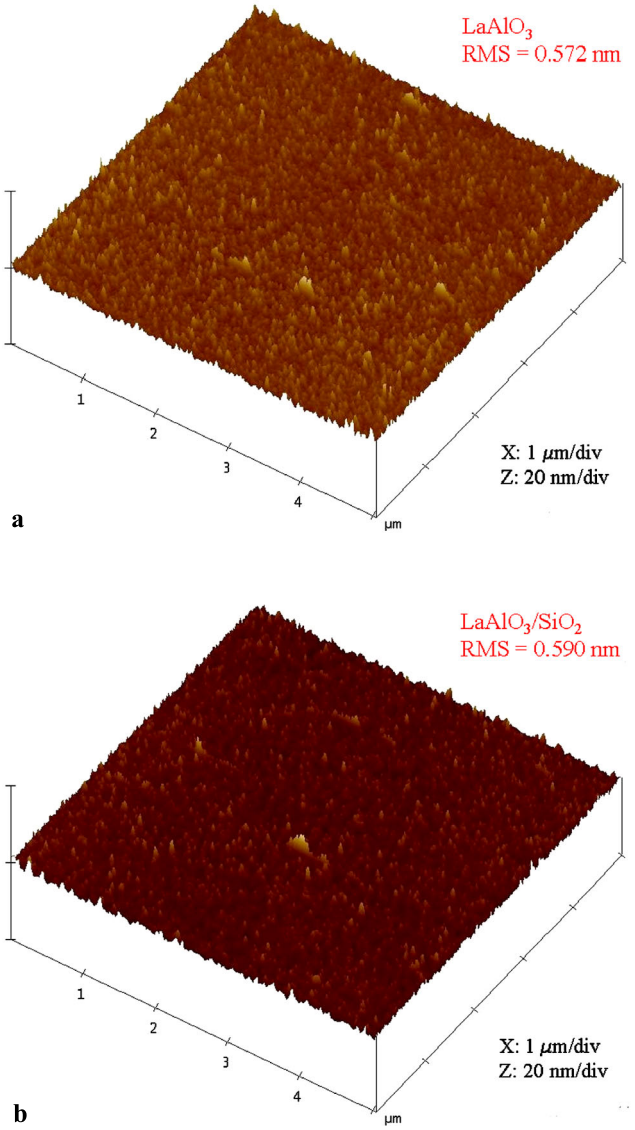

Fig. 3 AFM images of (**a**) single $LaAlO_3$ and (**b**) stacked $LaAlO_3/SiO_2$ gate insulators on bottom TaN gate

To further improve the performances of the IGZO TFTs, a SiO_2 was inserted as buffer layer at the interface of IGZO/$LaAlO_3$. The output I_d–V_d and transfer I_d–V_g characteristics of the IGZO TFT with inserted SiO_2 buffer layer are shown in Fig. 6(a) and (b), respectively. Using a SiO_2 buffer layer, the IGZO TFT device exhibits improved performances including a high I_{on}/I_{off} of 6.2×10^4, a small SS of 0.113 V/dec and a large μ_{FE} of 5.2 cm^2/V sec with a low V_t of 0.27 V. The comparison of the TFT parameters is provided in Table 1, indicating that SiO_2 buffer layer insertion is necessary for stable operation of the TFT. Although the effective dielectric constant of gate stack decreased with

Table 1 Important transistor parameters for the IGZO TFTs without and with SiO_2 buffer layer

Insulator	Operation voltage (V)	V_t (V)	I_{on}/I_{off}	SS (V/dec)	μ_{FE} (cm^2/V sec)	N_{max} (cm^{-2})
$LaAlO_3$	1.5	0.36	1×10^3	0.405	0.84	2.2×10^{13}
$LaAlO_3/SiO_2$	1.5	0.27	6.2×10^4	0.113	5.2	1.3×10^{12}

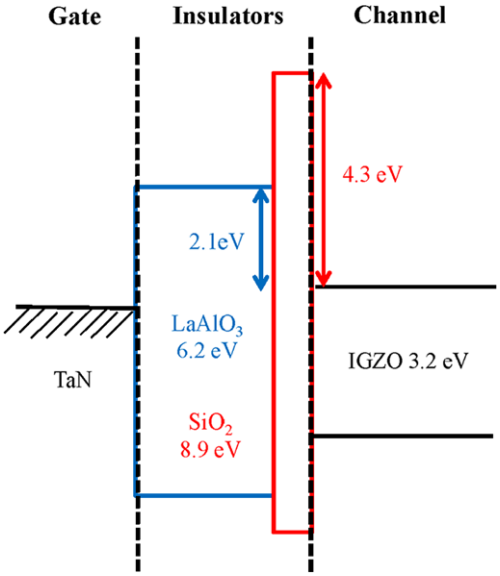

Fig. 4 Energy band diagram of gate stack for the IGZO TFT

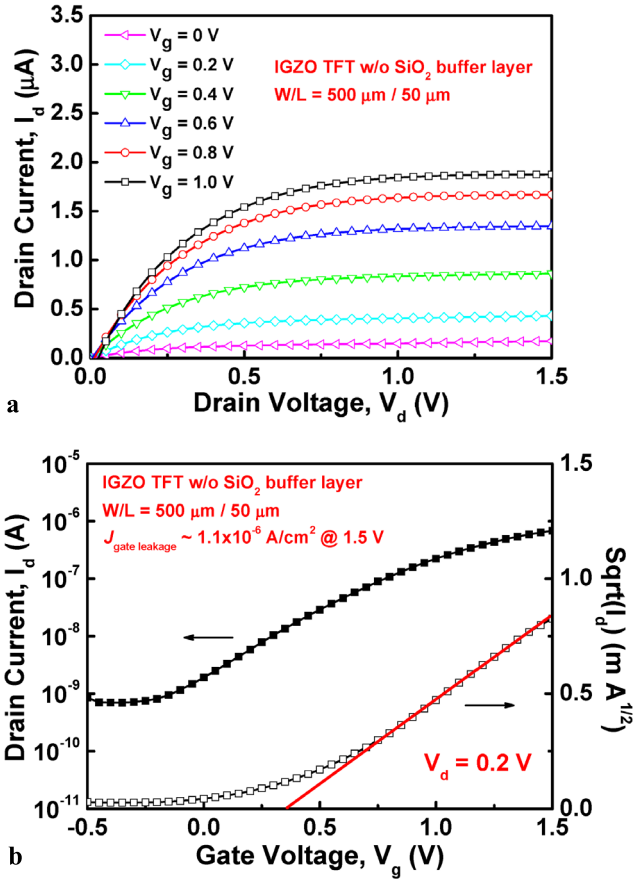

Fig. 5 (**a**) Output I_d–V_d characteristics and (**b**) transfer I_d–V_g characteristics of the IGZO TFT without SiO_2 buffer layer

addition of the SiO_2 buffer layer, the device performances have been greatly improved. It can be attributed to the lowered gate leakage and reduced interfacial issue caused by SiO_2 insertion [10–12, 20, 21, 23]. The off-current of the TFT device decreases after the SiO_2 buffer layer deposition and thus improves the I_{on}/I_{off}, which agrees with the small gate leakage for $SiO_2/LaAlO_3$ gate stack. On the other hand, the performances of TFTs are strongly influenced by the interface trap states at the interface between the active channel and gate insulator, since the field-induced carriers are confined to a very thin region close to the interface. The interface defects can produce trapping or scattering effects, leading to the degradation of μ_{FE} and SS. From SS, we can infer the maximum density of surface states at the gate dielectric/IGZO channel interface, according to the SS equation [12]: $N_{max} = [SS \cdot \log(e)/(kT/q) - 1] \cdot (C_g/q)$. Here, k is the Boltzmann constant, T is absolute temperature, q is charge quantity of an electron. The N_{max} is calculated to be $\sim 2.2 \times 10^{13}$ cm^{-2} for the TFT device without SiO_2 buffer layer insertion, while much lower N_{max} of $\sim 1.3 \times 10^{12}$ cm^{-2} for the TFT device after inserting SiO_2 buffer layer. It is well known that the TFT performances are greatly governed by the surface states at the interface. Due to the interfacial issue caused by $LaAlO_3$ [22], inserting a smooth SiO_2 buffer layer evaporated at room temperature without sputtering plasma damage can effectively passivate high-κ surface and reduce interface states near the IGZO active channel layer [10–12], resulting in the improvement of μ_{FE} and SS. A very small SS of 0.113 V/dec was achieved, close to the theoretical minimum value of 0.060 V/dec at room temperature, which indicates low interface trap density using a SiO_2 buffer layer insertion.

4 Conclusions

We demonstrate improved performances in IGZO TFTs using a SiO_2 buffer layer inserted between the IGZO active channel layer and high-κ $LaAlO_3$ gate insulator. Good TFT device characteristics are achieved simultaneously, including a low V_t of 0.27 V, a good I_{on}/I_{off} of 6.2×10^4, a small

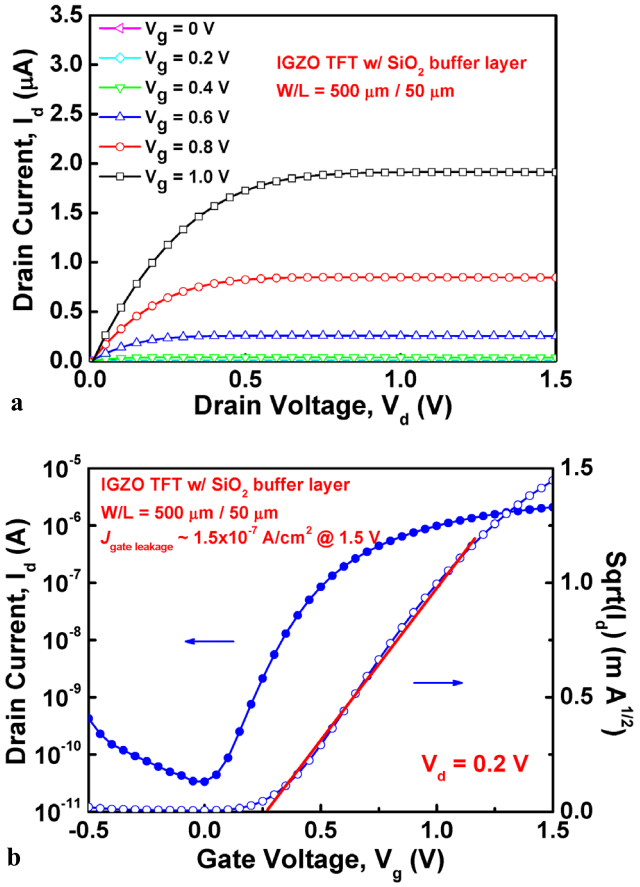

Fig. 6 (**a**) Output I_d–V_d characteristics and (**b**) transfer I_d–V_g characteristics of the IGZO TFT with SiO_2 buffer layer

SS of 0.113 V/dec and a large μ_{FE} of 5.2 cm^2/V sec at operation voltage as low as 1.5 V. Such good performances were attributed to the lowered gate leakage and reduced interfacial issue caused by SiO_2 buffer layer insertion. These present results show that low-voltage-driven IGZO TFTs with stacked $LaAlO_3/SiO_2$ as gate insulators have a great promise for future high-speed and low-power applications.

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