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Tuning of the Fermi level is investigated in graphene channels using two in-plane gates with significantly different-sized isolating gaps. While the n-type tuning was achievable in both schemes, the wide-gap device had an enhanced minimum drain current and less prominent current modulation than the narrow-gap device. In addition, further p-type tuning was not observed in the wide-gap device at negative gate biases. These phenomena indicated that both devices had distinct field-strength dependences and Fermi level tuning effects, which may be critical for the practical design of devices.
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Owing to its unique electrical, chemical, and thermal properties, graphene, a two-dimensional material formed by carbon atoms in a honeycomb lattice, has attracted a lot of attention.[1] To prepare graphene films, many methods, including mechanical exfoliation using scotch tape, sublimation of silicon carbide in a high-vacuum chamber, and chemical vapor deposition (CVD) on metal templates,[1–7] have been performed. To achieve large-area and high-quality graphene films, the CVD growth of graphene on copper (Cu) foil has been regularly adopted. However, chemical contamination or water adsorption during the sample transferring process causes most graphene films to appear heavily p-type doped.[8] Often, positive biases that result in minimum drain currents (crossing between the Fermi level and the Dirac point) are observed in graphene field-effect transistors.[8,9] To operate around the Dirac point, effort has been devoted to n-type doping graphene films. Possible approaches to achieve this goal include: applying an ammonia gas flow during the graphene growth process or immersing the graphene films in a chemical solution.[9] Although these methods are effective in obtaining n-type doped graphene films, they do not provide precise control over the carrier density. Conversely, the control over carrier densities can be achieved electrically by employing the architecture of a dual-gate device.[10,11] Through tuning either the top or the bottom gate voltage, the Fermi level of a graphene film can be manipulated. In doing this, the original positive bottom/top gate voltage at the minimum drain current can be shifted to a zero or negative bias. However, the main disadvantage of this approach is that the top dielectric layers can possibly influence the graphene channels, leading to a more complicated fabrication procedure. To solve these problems, an in-plane-gate device architecture is an alternative choice for graphene transistors.[12,13] This in-plane-gate device architecture has been widely applied for one-dimensional transistors and quantum transport devices.[14,15]

In this paper, tuning the Fermi level of graphene channels is achieved with in-plane-gates, and examined using bottom gates. Two devices with significantly different-sized isolating gaps (10 μm versus 100 nm or less) between their in-plane gates and channels are investigated. The channels of both devices were p-type doped in nature and could be electrically converted to n-type with comparable positive biases applied to the in-plane gates. Upon being tuned into n-type, the 10-μm-gap device had an enhanced minimum drain current and a less prominent current modulation as its bottom-gate voltage was swept around its bias point, corresponding to the Dirac point. In addition, with a negative in-plane gate voltage, only the 100-nm-gap device could be tuned further p-type effectively. These phenomena may originate from the field effect, owing to the distinct sizes of the insulating gaps and the non-uniform carrier density profiles in the graphene channels as a result of the in-plane-gate geometry.[16]

The graphene films were prepared with a low-pressure CVD system. Copper foils about 25 μm in size were annealed at 1030 °C for 30 min in a quartz tube furnace that was filled with 320 mTorr hydrogen gas (H_2) to remove the metal oxide. After annealing, the gas mixture was composed of methane and H_2 with flow rates 7 and 15 sccm, respectively, which was sent into the tube to grow the graphene. During the 10-min growth period, the pressure was maintained at 650 mTorr. The samples were then removed from the tube and underwent a standard graphene transfer procedure.[10] After these steps, the graphene films were attached to 600-nm silicon-dioxide/silicon (SiO_2/Si) substrates, which were pre-patterned with titanium/gold (Ti/Au) electrodes. The same film preparation and transferring procedure has been discussed elsewhere.[17]

For the fabrication of the 10-μm-gap device, a pattern was formed using standard photolithography and oxygen (O_2) plasma etching was performed to define the transistor channel on the film. A scanning electron microscope (SEM)

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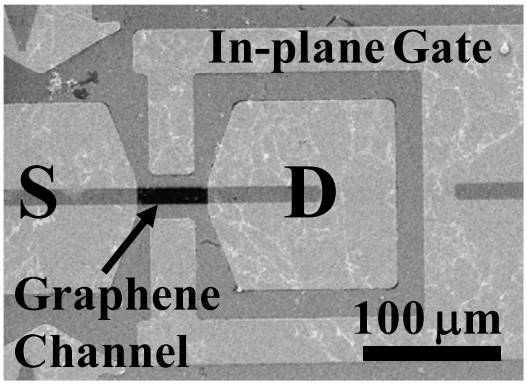
image of the device is shown in Fig. 1(a). The in-plane gate, drain, and source electrodes were made of Au. The channel itself and the separations between the channel and in-plane gates were all 10 μm. The drain currents (I_D) are plotted as a function of the bottom gate voltage ($V_{GS,b}$) at different in-plane gate biases ($V_{GS,in} = -100$, 0, and 100 V) in Fig. 1(b). As a positive $V_{GS,in}$ was applied, the bottom-gate voltage ($V_{GS,b,min}$) at the minimum drain current ($I_{D,min}$) shifted from 70 to nearly 0 V. This result suggests that the in-plane gate voltage shifted the Fermi level in the graphene channel and shows the potential for Fermi level tuning. The minimum drain current ($I_{D,min}$) nearly doubled from 20 to 40 μA.



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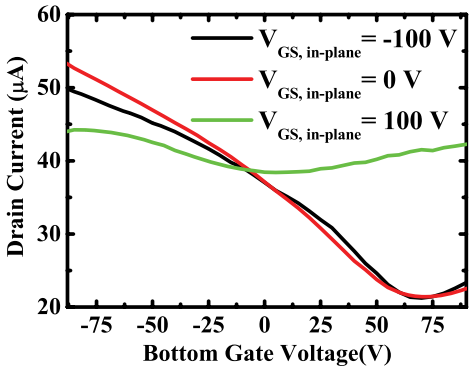

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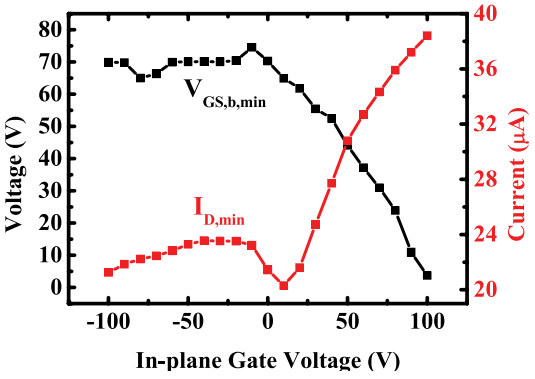
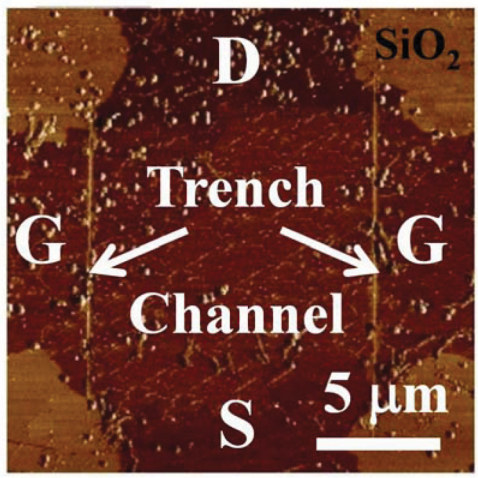


(c)

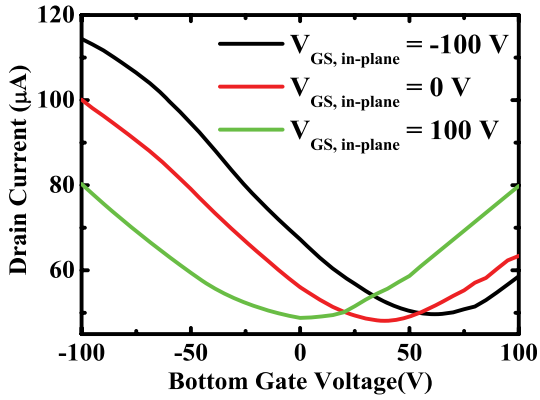
FIG. 1. (a) SEM image of an in-plane gate graphene transistor with 10-μm isolating gaps. (b) The drain current, I_D of this device as a function of the $V_{GS,b}$ at $V_{GS,in} = -100$, 0, and 100 V. (c) The minimum drain current, $I_{D,min}$ and corresponding bottom-gate bias, $V_{GS,b,min}$ versus $V_{GS,in}$.

The corresponding modulation of I_D with the bottom-gate voltage, $V_{GS,b}$ around $V_{GS,b,min}$, was not as sharp as its counterpart at $V_{GS,in} = 0$ V. Conversely, the $V_{GS,b}$-I_D curve at a negative in-plane gate voltage of $V_{GS,in} = -100$ V remained similar to that at $V_{GS,in} = 0$ V. This observation indicated that further inducing holes through electrical control of $V_{GS,in}$ was ineffective. The distinct trends in the current modulations at opposite $V_{GS,in}$ polarities could be demonstrated by plotting $V_{GS,b,min}$ and $I_{D,min}$ as a function of $V_{GS,in}$, as shown in Fig. 1(c). The effective tuning with an increasing $V_{GS,in}$ was accompanied by a negative shift in the $V_{GS,b,min}$ and an increase in $I_{D,min}$. However, variations in these two quantities were much less significant (also non-monotonic for $I_{D,min}$) as $V_{GS,in}$ became negative, implying that electrical p-type tuning did not function properly.

The device with 100-nm-wide isolating gaps between the channel and the in-plane gates exhibited different behavior. An image of the device layout is shown in Fig. 2(a). In this device, a crisscross graphene sheet was scraped with atomic force microscopy (AFM) tips at the joints between two of the graphene arms, resulting in two trenches (isolating gaps). The AFM scraping over the graphene surfaces proved to be effective at electrically isolating the graphene sheets at the two sides of the trench.[18] The trenches were about



(a)



(b)

FIG. 2. (a) An image of a crisscross graphene film after AFM scraping (100-nm trenches). (b) The $V_{GS,b}$-I_D curves of the narrow-gap device under $V_{GS,in} = -100$, 0, and 100 V.

100 nm in width. The graphene sheet between the two trenches was 10 μm wide and played the role of the channel, while the two disjointed graphene arms functioned as in-plane gates. The $V_{GS,b}$–I_D curves for this device, measured with $V_{GS,in} = -100$, 0, and 100 V, are shown in Fig. 2(b). The comparison between the two curves at $V_{GS,in} = 0$ V in Figs. 1(b) and 2(b) show that the device with AFM-scraped gaps had a smaller $V_{GS,b,min} = 40$ V, indicating that the corresponding channel was less p-type doped in nature. This characteristic may originate from the change in the graphene-SiO_2 interface, induced by the AFM scraping.[17] At $V_{GS,in} = 100$ V, the bottom-gate voltage, $V_{GS,b,min}$ at the minimum drain current was lowered to 0 V. This bias shift indicated that the n-type tuning was effective. In contrast to the doubling of the $I_{D,min}$ in the 10-μm-gap device, the minimum drain current did not alter much. Meanwhile, the current modulation around $V_{GS,b,min}$ remained as sharp as that at $V_{GS,in} = 0$ V. For a negative bias of $V_{GS,in} = -100$ V, the voltage $V_{GS,b,min}$ increased to around 70 V, indicating that further p-type tuning through electrical control of the in-plane gates was possible. In addition, the sharp current modulation remained under these circumstances.

The differences between these two devices may have been caused by the non-uniformity of the carrier profiles that were induced by distinct field effects.[16] The drain current I_D was proportional to the channel conductivity σ_{ch}, which is related to the average local surface carrier density along the channel cross section:

$$\sigma_{ch} = q\mu \int \frac{dx}{W} n(|E_F - E_{Dirac}(x)|), \quad (1)$$

where q and μ are the charge and mobility of the carriers, respectively, of which the product $q\mu$ is roughly identical and has the same sign for both electrons and holes; W is the width of the channel; and $n(|E_F–E_{Dirac}(x)|)$ is the surface carrier density (regardless of carrier types) at position x, which only depends on the difference in the magnitude between the Fermi level, E_F, and local Dirac-point energy, $E_{Dirac}(x)$. The surface density (n) nearly vanished at $E_F = E_{Dirac}$, except for some minor contributions such as charged impurities.[19] However, the density n always increased, regardless of whether E_F was above or below E_{Dirac}. From this viewpoint and Eq. (1), switching off the channel conductivity σ_{ch} with a constant E_F became difficult when $E_{Dirac}(x)$ had a large spatial fluctuation or simply deviated from a constant in the channel because $E_F–E_{Dirac}(x)$ cannot simultaneously vanish everywhere. This issue is not common in semiconductors with considerable bandgaps. As long as the Femi level is deep inside the bandgap, the local carrier density is always small and the spatial variations of band edges play a minor role in this aspect.

Figure 3 shows a schematic band diagram of the 10-μm-gap device under a positive $V_{GS,in}$. Only half of the channel is depicted owing to its symmetric layout. Because the widths of the isolating gap and channel were comparable, a considerable voltage drop was present across the channel region shown in Fig. 3. This voltage drop lifted the Fermi level E_F ($V_{GS,b} = 0$) at a zero bottom-gate voltage close to/above the Dirac-point energy, $E_{Dirac}(x)$ (tuned into n-type electrically). Although the wide gap led to a mild electric field (F_1) near

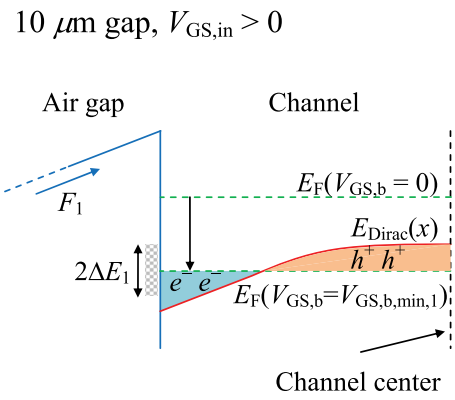


FIG. 3. The weak field (F_1) induced a wide-range variation in the $E_{Dirac}(x)$, which smoothed the current modulation of the wide-gap device.

the graphene edge, this field persisted in the channel and induced a wide-range of variations in the Dirac-point energy $E_{Dirac}(x)$. In this case, when the bottom-gate voltage, $V_{GS,b,min,1}$ that minimizes the drain current was applied, the corresponding Fermi level E_F ($V_{GS,b} = V_{GS,b,min,1}$) did not conform well with $E_{Dirac}(x)$, and the minimum drain current was enhanced. It was also expected that a change in E_F within twice the standard deviation, ΔE_1 of the energy difference $E_F(V_{GS,b} = V_{GS,b,min,1}) - E_{Dirac}(x)$ would not suddenly change the I_D, which partially explains the smooth modulation of I_D with $V_{GS,b}$. However, the mild modulation could have also been caused by the non-uniform in-plane field distributed along the channel (from the drain to the source).[16]

The band diagram for the 100-nm-gap device at a positive $V_{GS,in}$ is shown in Fig. 4. With an intense external field $F_2 \gg F_1$, $E_{Dirac}(x)$ varied sharply around the graphene edge. Because of the lack of a bandgap, the spatial charge could easily be induced, even when the graphene sheet had a low carrier density. With this, the electrons induced by F_2 accumulated around the edge of the film, screening the intense field and confining the sharp variation of $E_{Dirac}(x)$, only at the edge. The accumulated electrons experienced more disorder and extrinsic scattering than those in the graphene sheet, causing them to become less mobile. As a result, the modulation of I_D with $V_{GS,b}$ around the minimum-current voltage $V_{GS,b,min,2}$ was mainly influenced by the flat profile of $E_{Dirac}(x)$ in the channel. Because the deviation (ΔE_2) of

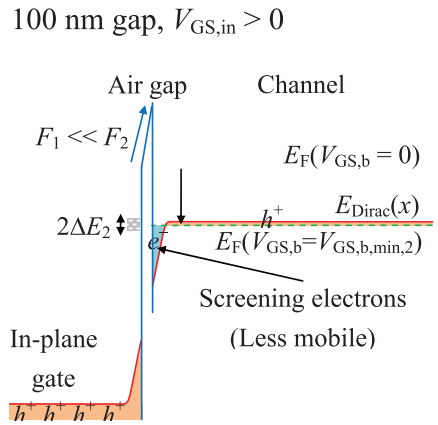


FIG. 4. The induced electrons screened the intense field F_2, maintained the flatness of the $E_{Dirac}(x)$, and kept the current modulation of the narrow-gap device sharp.

$E_F(V_{GS,b} = V_{GS,b,min,2}) - E_{Dirac}(x)$ was narrow in this case, the current modulation remained sharp. For the negative in-plane gate voltage, the incapability of further inducing holes in the 10-μm-gap device may be attributed to the already strong screening from holes, which further prevented the weak external field from penetrating the graphene channel. Conversely, the electrical p-type tuning might still be effective in the 100-nm-gap device because of the intense external field and the weaker screening (less natural p-type doping because of AFM scraping).

In conclusion, tuning of the Fermi level in graphene channels was achieved with two in-plane gates of different sizes. The device architecture simplified the fabrication procedure. Modulation of the drain current through the in-plane gate was influenced by the external field strength, carrier screening near the graphene edge, and the uniformity of the Dirac-point energy inside the channel. These factors affected the capability of Fermi level tuning and the sharpness of the current modulation, and have to be taken into account in the practical design of devices.

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