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Material growth and device characterization of AlGaN/GaN single-heterostructure and AlGaN/GaN/AlGaN double-heterostructure field effect transistors on Si substrates

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An $Al_{0.2}Ga_{0.8}N/GaN/Al_{0.1}Ga_{0.9}N$ double-heterostructure field effect transistor (DH-FET) structure was grown on a 150-mm-diameter Si substrate and the crystalline quality of the epitaxial material was found to be comparable to that of an $Al_{0.2}Ga_{0.8}N/GaN$ single-heterostructure field effect transistor (SH-FET) structure. The fabricated DH-FET shows a lower buffer leakage current of 9.2×10^{-5} mA/mm and an improved off-state breakdown voltage of higher than 200 V, whereas the SH-FET shows a much higher buffer leakage current of 6.0×10^{-3} mA/mm and a lower breakdown voltage of 130 V. These significant improvements show that the $Al_{0.2}Ga_{0.8}N/GaN/Al_{0.1}Ga_{0.9}N$ DH-FET is an effective structure for high-power electronic applications. © 2014 The Japan Society of Applied Physics

Owing to the superior material properties of GaN, including high breakdown field, wide band gap, high saturated electron velocity, and high operation temperature, GaN-based devices have attracted much attention for high-power switching applications.[1] Conventional AlGaN/GaN single-heterostructure field effect transistors (SH-FETs) fabricated on SiC, sapphire and Si substrates all exhibit high breakdown voltage and low specific on-resistance characteristics.[2–4] The difficulties of the large lattice mismatch and the large thermal mismatch between GaN and Si substrates have been overcome in recent years. The extraordinary development has made GaN-on-Si technology for high-power and high-frequency devices on Si substrates with diameters larger than 150 mm realizable.[5–7] The production of GaN devices on large-diameter Si substrates at a low fabrication cost is considered the key factor for leading GaN-based devices into the next-generation power electronic market.

In order to further improve the breakdown voltage of the GaN-on-Si devices, several methods have been proposed over the last few years, such as the use of a thicker epitaxial layer, the inclusion of a carbon-doped GaN buffer, the implementation of a field plate structure, ion-implantation isolation, and local Si substrate removal.[8–13] Additionally, AlGaN/GaN/AlGaN double-heterostructure field effect transistors (DH-FETs) for high-breakdown-voltage devices were also investigated because of the better electron confinement and higher breakdown field when using the AlGaN back barrier.[14,15] However, even with these advances, studies focusing on the comparison of the device performances of SH-FETs and DH-FETs fabricated on larger diameter Si substrates are still lacking.[16]

In this work, an $Al_{0.2}Ga_{0.8}N/GaN/Al_{0.1}Ga_{0.9}N$ DH-FET structure with an $Al_{0.1}Ga_{0.9}N$ back barrier and a conventional $Al_{0.2}Ga_{0.8}N/GaN$ SH-FET structure with a GaN buffer were grown on 150-mm-diameter Si substrates. Both wafers show good crystalline quality. The epitaxial layer growth process and the crystal quality of the DH-FET and SH-FET structures on Si substrates are discussed and the device performances are compared in this study. It is found that the breakdown voltage of the DH-FET is greatly improved with the $Al_{0.1}Ga_{0.9}N$ back barrier layer.

The epitaxial growth of the DH-FET and SH-FET structures on 150-mm-diameter Si(111) substrates were carried out using a Thomas Swan metal organic chemical vapor deposition (MOCVD) system. Trimethylgallium (TMGa), trimethylaluminum (TMAl), and ammonia were used as the precursors for Ga, Al, and N elements, respectively. H_2 was used as the carrier gas. Firstly, an AlN nucleation layer (200 nm) and multi-$Al_xGa_{1-x}N$ transition layers (600 nm) were grown on the Si substrate. Following the transition layer growth, the $Al_{0.2}Ga_{0.8}N/GaN/Al_{0.1}Ga_{0.9}N$ (27 nm/55 nm/1.4 µm) epitaxial layers were grown for the DH-FET. The cross-sectional transmission electron microscopy (TEM) images of the whole DH-FET epitaxial structure and the $Al_{0.2}Ga_{0.8}N/GaN/Al_{0.1}Ga_{0.9}N$ heterostructure layers are shown in Figs. 1(a) and 1(b), respectively. The sample of the $Al_{0.2}Ga_{0.8}N/GaN$ SH-FET (27 nm/2.6 µm) structure was grown on the same AlN and multi-$Al_xGa_{1-x}N$ buffer layers as the control sample for device performance comparison.

A Laytec EpiCurve® TT system was used for in-situ measurement of the wafer temperature, reflectance, and wafer curvature during epitaxial layer growth. The crystalline qualities of these two structures were examined using the high-resolution X-ray diffraction (HRXRD) Bede D1 system. From room-temperature Hall measurements, the mobility of 1110 $cm^2 V^{-1} s^{-1}$ and the sheet carrier concentration of $8.5 \times 10^{12}/cm^2$ were obtained on the DH-FET structure. The SH-FET structure exhibited the mobility of 1270 $cm^2 V^{-1} s^{-1}$ and the sheet carrier concentration of $8.7 \times 10^{12}/cm^2$.

The DH-FET and SH-FET devices were fabricated after the epitaxial growth. The device mesa regions were defined using an inductively coupled plasma (ICP) etcher. The Ti/Al/Ni/Au (20/120/25/100 nm) multilayer metal was deposited as the source and drain ohmic contact metal using an electron beam evaporator, and was subsequently annealed at 800 °C for 60 s in N_2 atmosphere. According to the transmission line model method, the ohmic contact resistances of 0.5 and 0.6 Ω·mm were obtained for the DH-FET and SH-FET structures, respectively. Finally, the Ni/Au (20/300 nm) metal was deposited as a Schottky gate metal using the electron beam evaporator. The gate width (W_g), gate length (L_g), gate-to-drain spacing (L_{gd}), and gate-to-source spacing (L_{gs}) were 100, 1, 4.5, and 1.5 µm, respectively. The electrical characteristics of the devices were measured using Agilent E5270B.

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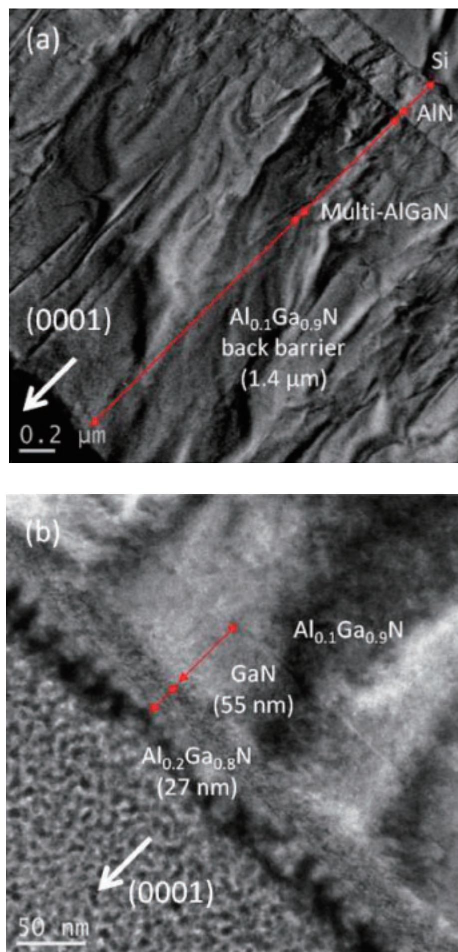

Fig. 1. Cross-sectional TEM images of (a) DH-FET structure with AlN and multi-AlGaN buffer layers on the Si substrate, and (b) $Al_{0.2}Ga_{0.8}N$/GaN/$Al_{0.1}Ga_{0.9}N$ double heterostructure.

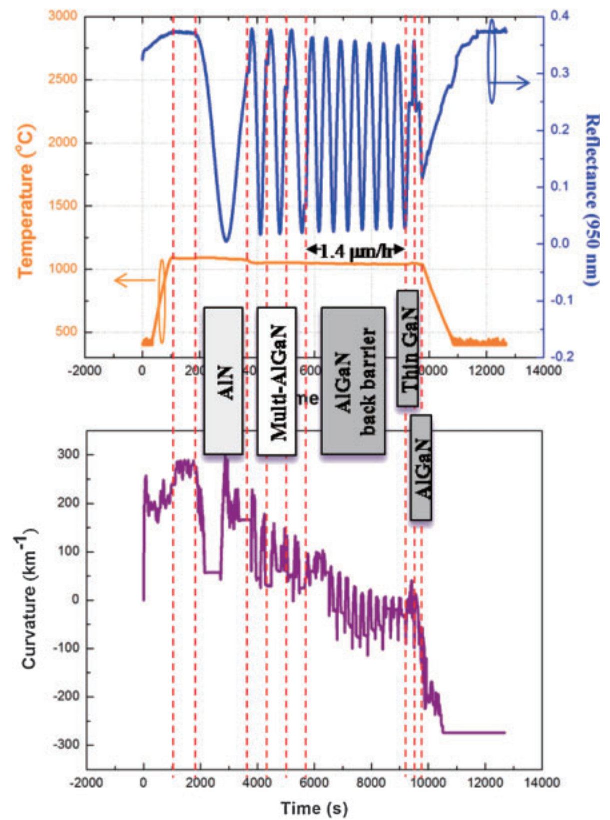

Fig. 2. Data of in situ measurements of temperature, reflectance, and wafer curvature during the growth of DH-FET.

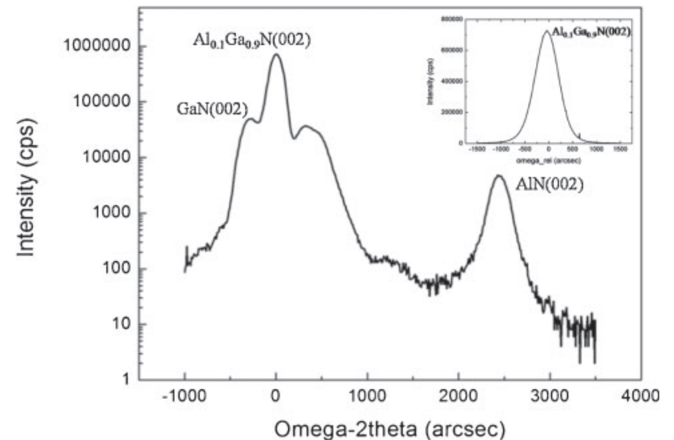

Fig. 3. XRD ω–2θ scan of DH-FET epitaxial structure. The inset shows the rocking curve of the $Al_{0.1}Ga_{0.9}N(002)$ peak.

Figure 2 shows the transients of temperature and reflectance (upper figure) and the wafer curvature (lower figure) obtained with a Laytec EpiCurve® TT system during the growth of the $Al_{0.2}Ga_{0.8}N$/GaN/$Al_{0.1}Ga_{0.9}N$ DH-FET structure. The growth rate was 1.4 µm/h and the layer thickness was 1.4 µm for the $Al_{0.1}Ga_{0.9}N$ back barrier, as determined from the Fabry–Perot oscillations using the reflectance at 950 nm. The reflectance intensity maxima and minima occurred at constant values during the growth of the $Al_{0.1}Ga_{0.9}N$ back barrier. This indicates that the epitaxial layers were quite smooth. Meanwhile, a SH-FET with a 2.6-µm-thick GaN buffer was grown on a Si substrate for comparison.

The in-situ wafer curvature measurement is essential for optimizing growth recipes and controlling the stress in order to maintain crack-free wafers. By emitting two parallel laser beams from the Laytec EpiCurve® TT curve head, the curvature can be calculated from the difference between the initial separation distance of the parallel beams and the distance between reflected laser beams. A convex wafer means a negative curvature due to compressive stress. For the DH-FET, a negative curvature trace was observed during the growth of the multi-$Al_xGa_{1-x}N$ transition layers and the $Al_{0.1}Ga_{0.9}N$ back barrier, indicating that an effective compressive stress was introduced. Owing to the significant difference between thermal expansion coefficients of GaN and the Si substrate, this compressive stress induced in the epitaxial layer is necessary to compensate for the tensile stress during the cooling process.

Figure 3 shows HRXRD ω–2θ scanning and rocking curve results for the DH-FET. The Al composition of 10.3% in the AlGaN(002) peak shows the highest intensity in the ω–2θ scan. A higher Al composition in AlGaN is required to provide a higher conduction band discontinuity. However, when the Al composition is above 10%, the thermal conductivity of AlGaN becomes quite low because of alloy scattering.[17] Therefore, the Al composition should be kept below 10% for the growth of the $Al_xGa_{1-x}N$ back barrier.

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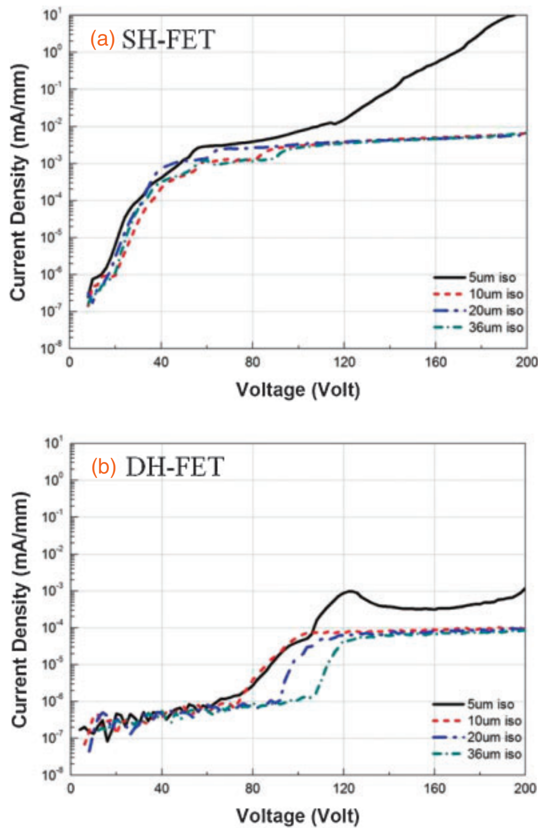

Fig. 4. Buffer leakage currents of (a) SH-FET and (b) DH-FET with various metal contact spacings.

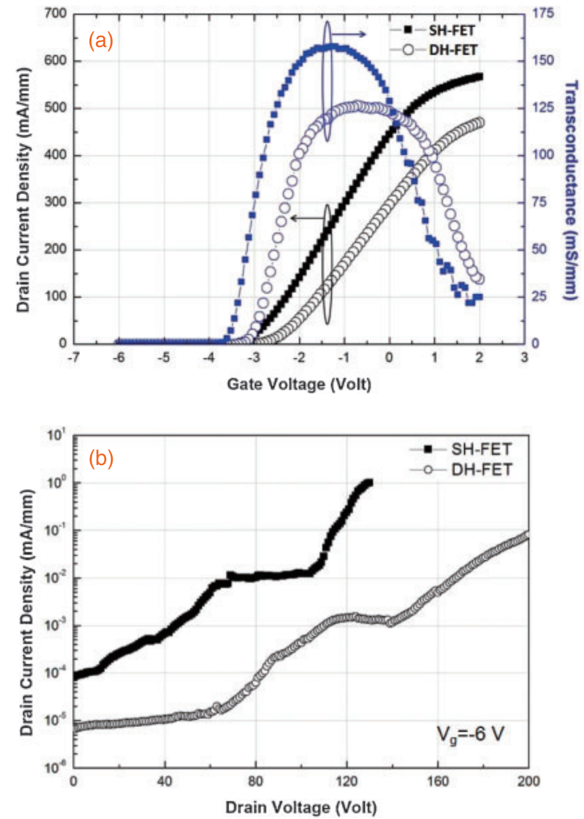

Fig. 5. Device characteristics of SH-FET and DH-FET ($W_g/L_g/L_{gd}/L_{gs}$ = 100/1/4.5/1.5 µm). (a) I_D–V_G transfer characteristics and (b) breakdown voltage characteristics.

Compared with the GaN buffer used for SH-FET, the DH-FET buffer has better electron confinement in the GaN channel owing to a higher conduction band discontinuity, which helps to prevent the leakage current at the $Al_{0.1}Ga_{0.9}N$ back barrier. The full-widths at half-maximum (FWHMs) of X-ray rocking curves for the $Al_{0.1}Ga_{0.9}N(002)$ ω-scan and $Al_{0.1}Ga_{0.9}N(102)$ ω-scan were 578.8 and 1110 arcsec, respectively. On the other hand, the SH-FET exhibited the FWHMs of 473.8 and 653.8 arcsec for the GaN(002) ω-scan and GaN(102) ω-scan, respectively. The SH-FET has narrower FWHMs owing to the presence of the 2.6-µm-thick GaN buffer. However, the crystalline quality of the $Al_{0.1}Ga_{0.9}N$ back barrier is comparable to those in other studies of AlGaN with 10% Al composition in the literature.[18,19)]

The buffer leakage current characteristics of the SH-FET and DH-FET measured using different ohmic contact spacings are plotted in Figs. 4(a) and 4(b), respectively. When measured with isolation patterns with a 5 µm gap, the breakdown voltage of the SH-FET is 170 V, as defined by the leakage current of 1 mA/mm. However, the breakdown voltage of the DH-FET is more than 200 V. The buffer leakage current of the DH-FET is 9.2×10^{-5} mA/mm when measured at 200 V with an isolation pattern having a 20 µm gap, which is much lower than that of the SH-FET measured under the same conditions (6.0×10^{-3} mA/mm). The reduced buffer leakage current of the DH-FET indicates that the higher conduction band discontinuity and higher breakdown field of the $Al_{0.1}Ga_{0.9}N$ back barrier can effectively reduce the leakage of the electrons from the channel to the buffer.

The transfer characteristics and leakage currents of the SH-FET and DH-FET are plotted in Figs. 5(a) and 5(b), respectively. The fabricated devices have a gate-to-drain spacing (L_{gd}) of 4.5 µm. The maximum drain current density of 475 mA/mm under $V_g = 2$ V for the DH-FET is lower than the current density of the SH-FET. The reduction in drain current density may result from the lower sheet carrier concentration of the DH-FET. Additionally, the lower sheet carrier concentration results in the threshold voltage shift. The threshold voltage shifted positively from −3.2 V for the SH-FET to −2.3 V for the DH-FET. Moreover, a lower leakage current for the DH-FET was observed. A higher breakdown voltage of greater than 200 V for the DH-FET was achieved compared with the 130 V observed for the SH-FET. The improvement of buffer isolation by using an $Al_{0.1}Ga_{0.9}N$ back barrier also reduces the punch-through effects and thus markedly improve the breakdown voltage of the device.[20)] Although the total thickness of the $Al_{0.2}Ga_{0.8}N/GaN/Al_{0.1}Ga_{0.9}N$ DH-FET is much smaller than that of the $Al_{0.2}Ga_{0.8}N/GaN$ SH-FET, the device still demonstrates improved breakdown voltage characteristics. Overall, the study reveals that the $Al_{0.1}Ga_{0.9}N$ back barrier can substantially improve the breakdown voltage of the device even with thinner buffer layers.

In conclusion, high-crystalline-quality $Al_{0.2}Ga_{0.8}N/GaN$ SH-FET and $Al_{0.2}Ga_{0.8}N/GaN/Al_{0.1}Ga_{0.9}N$ DH-FET structures were grown on 150-mm-diameter Si substrates, and the SH-FET and DH-FET devices were fabricated. For the DH-FET, a lower buffer leakage current of 9.2×10^{-5} mA/mm and an improved off-state breakdown voltage of higher than

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200 V were realized, compared with the SH-FET. Because of the higher conduction band discontinuity and the better electron confinement in the channel, the $Al_{0.1}Ga_{0.9}N$ back barrier of the DH-FET can effectively prevent punch-through effects, resulting in a lower leakage current than that of the GaN buffer SH-FET, and thus greatly reduces the buffer thickness needed for the GaN power devices. Overall, it was demonstrated that the $Al_{0.2}Ga_{0.8}N/GaN/Al_{0.1}Ga_{0.9}N$ DH-FET approach with improved device characteristics resulting from the use of a thinner buffer layer is a promising technology for future high-power electronic applications.

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