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Fabrication and characterization of field-effect transistors with suspended-nanowire channels

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Novel field-effect transistors (FETs) configured with suspended-nanowire (NW) channels were fabricated and characterized. Owing to the small aspect ratio of the etched structure, a simple wet etching process was adopted to release the NW channels. Our results show that the stiction issue can be eliminated as the channel length is sufficiently short or the air gap is sufficiently thick. In addition, the specific trends in pull-in and pull-out voltages as well as subthreshold swing (SS) with varying air gap thicknesses were investigated in terms of hysteresis characteristics. Finally, the devices were shown to withstand more than 500 cycles of operation in the cycling tests with repeatable hysteresis characteristics.

1. Introduction

Recently, micro-electro-mechanical field-effect transistors (MEM-FETs) have drawn much attention owing to their great potential in a number of applications. As an oscillator,[1–4] the vibrating object in the FET fabricated with a CMOS-compatible process could be employed as a resonator, enabling the miniaturization of the device and reduction of power consumption. Owing to the steep subthreshold swing (SS) it exhibits, the suspended-gate FET[5–8] is considered a good candidate for serving as a switching component. In addition, by taking advantage of the large hysteresis window, hybrid MEMS-FET devices could also be applied for building high-performance memory devices.[9–13]

Although the idea of implementing hybrid MEMS-FET devices in integrated circuits (ICs) has been proposed,[14–16] some important issues impede its realization in practical manufacturing and application. For example, usually the etched structure in MEMS-FETs is very deep, its formation involves a complex and rugged release process such as dry chemical etching[5] and supercritical CO_2 drying.[17,18] Recently, we have proposed and demonstrated a new and simple approach to fabricating FETs with suspended-nanowire (NW) channels with the structure shown in Fig. 1.[19] In this scheme a greatly simplified process is implemented to release the NW channels. Moreover, this new device offers a sub-100 nm air gap between the suspended-NW channels and the gate, which is beneficial for reducing operation voltage. In this work, we further investigate the characteristics of the suspended-NW channel FETs with specific focus placed on the hysteresis, endurance, and oscillation phenomena.

2. Device structure and fabrication

The fabrication flow of the suspended-NW-channel FET is illustrated in Fig. 2. It started with an in situ-doped n^+ poly-Si gate deposited and patterned on an oxidized Si substrate [Fig. 2(a)]. Next, a silicon nitride (SiN) layer and a tetraethylorthosilicate (TEOS) oxide layer were deposited sequentially by low-pressure chemical vapor deposition (LPCVD) to serve as the gate dielectric and the sacrificial layer, respectively. The thickness of the SiN layer was fixed at 20 nm, while that for the oxide is varied from 10 to 70 nm. Afterwards, an amorphous silicon (α-Si) layer was deposited by LPCVD. To transform the α-Si into polycrystalline phase,

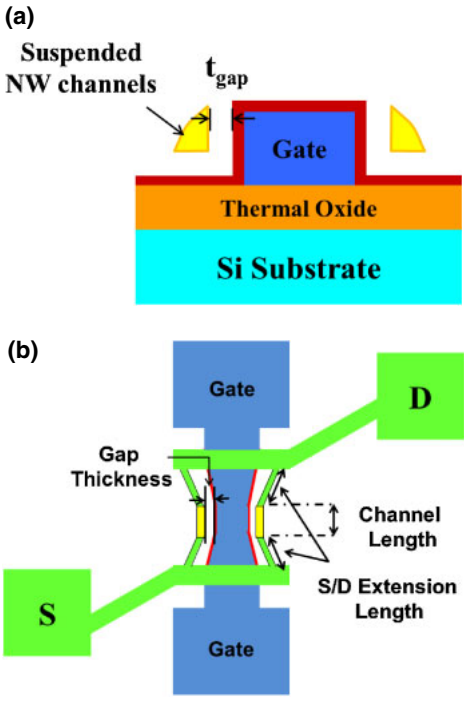

Fig. 1. (Color online) (a) Cross-sectional view and (b) top view of the suspended-NW-channel device.

the solid-phase crystallization (SPC) process was performed at 600 °C in N_2 ambient for 24 h [Fig. 2(b)]. The source/drain (S/D) pad regions were subsequently defined with a photolithographic step, followed by a standard dry etching to form the S/D. During the etching, poly-Si spacers abutting the sidewalls of the gate were simultaneously formed [Fig. 2(c)] and served as the NW channels connecting between the source and the drain. To dope the S/D, a photoresist (PR) pattern was generated to cover the central channel regions, followed by a P_{31}^+ S/D ion implantation at a dose of $5 \times 10^{15}\,cm^{-2}$ at 15 keV [Fig. 2(d)]. Then, the wafer was capped with a 300-nm-thick TEOS oxide layer deposited at 700 °C as the passivation layer [Fig. 2(e)]. Afterwards, another lithography process was carried out to define the region where the sacrificial layer would be etched off. Finally, a wet-etching process using an HF-containing solution was performed to remove the top passivation oxide

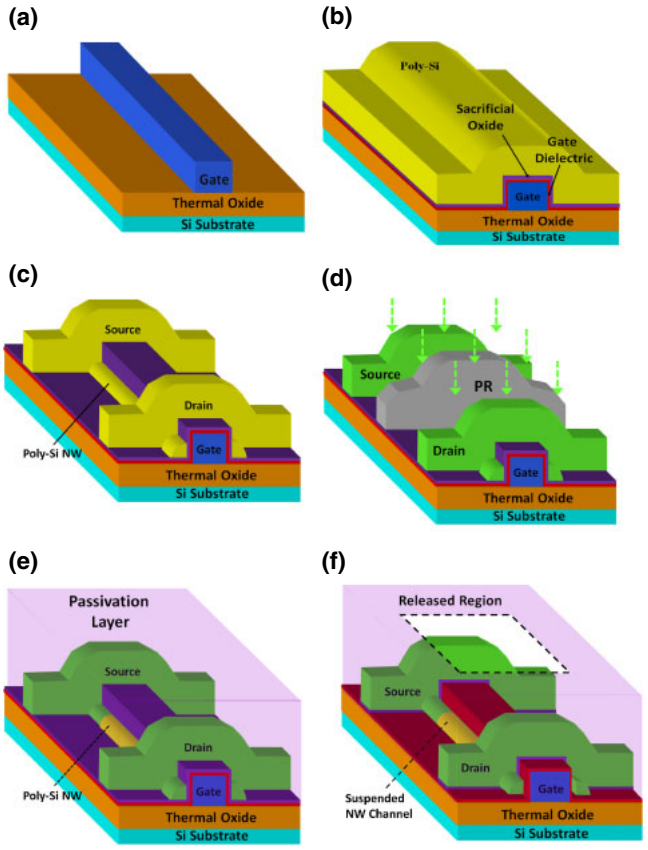

Fig. 2. (Color online) Key fabrication flow of the suspended-NW-channel device.

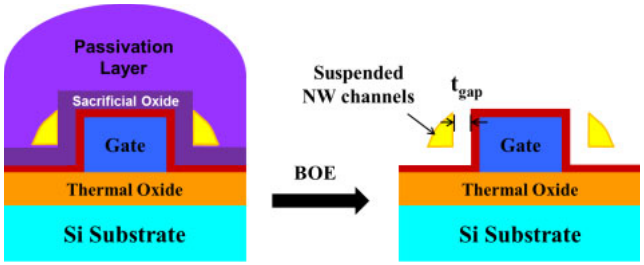

Fig. 3. (Color online) Cross-sectional schematics of the device before and after the selective oxide etching.

layer as well as the sacrificial oxide layer between the NW channels and the silicon nitride layer [Fig. 2(f)]. Cross-sectional views of the device before and after the selective oxide etching step are shown in Figs. 3(a) and 3(b), respectively.

3. Stiction

3.1 Stiction phenomenon

Figure 4 shows the cross-sectional transmission electron microscopy (TEM) views of the NW channel of a fabricated device. The pictures were taken before the sacrificial oxide layer was removed. As shown in the figures, the ratio of the NW width (54 nm) to the sacrificial oxide layer thickness (70 nm) is 0.78, which is much smaller than the ratio of gate length/sacrificial layer of SG-MOSFET.[5] Accordingly, a simple wet-etching process could be successfully

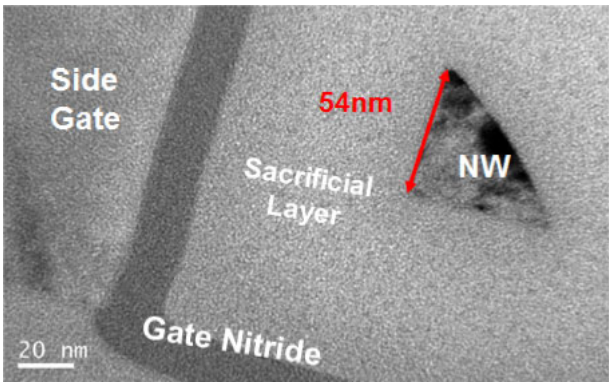

Fig. 4. (Color online) Cross-sectional TEM images of a fabricated device.

employed to remove the sacrificial oxide layer by this approach.

Although wet etching is more convenient than the dry chemical process, occurrence of the stiction phenomenon represents one of the major issues.[20,21] Indeed, such a phenomenon was observed in this work. Figure 5(a) shows two distinct transfer characteristics recorded from the fabricated devices with identical structural dimensions. The measurements were conducted by first positively and then negatively sweeping gate voltage. The results show that the fabricated devices may or may not show the hysteresis phenomenon during the measurements. Devices with suspended-NW channels are expected to show hysteresis characteristics,[19] and the operation principles are discussed in the next section. However, for a small portion of fabricated devices, the hysteresis window disappears (see the red dashed curves shown in this figure). In-line scanning electron microscopy (SEM) images of the two devices characterized in Fig. 5(a) are shown in Figs. 5(b) and 5(c). Figure 5(b) shows the device in which the NW channels were successfully released by the wet etching. In contrast, the other one, as shown in Fig. 5(c), shows the stiction issue during the wet-etching release process. The stiction failure during the wet-etching release process is caused by capillary force.[20] As shown in the SEM image, the NW channels stick to the gate nitride after the wet etching process and thus have insufficient capability to mechanically oscillate. This well explains why the device does not exhibit the hysteresis behavior in Fig. 5(a).

Fortunately, the observation of the stiction phenomenon is rare for the fabricated devices and can be completely suppressed as the channel length (L) of the device is sufficiently small. Figure 6 shows stiction probability as a function of L for devices with various air gap thicknesses. As can be seen in the figure, the yield increases with decreasing channel length. For devices of the same L, the stiction probability decreases with increasing the gap thickness. These observations are attributed to the reduction in the capillary. For gaps of 40 and 70 nm, no stiction is observed as L is smaller than 1 μm.

3.2 Theoretical analysis

To further explore the above phenomenon, we try to theoretically analyze the experimental results by considering the elastic energy and surface adhesion energy stored in the

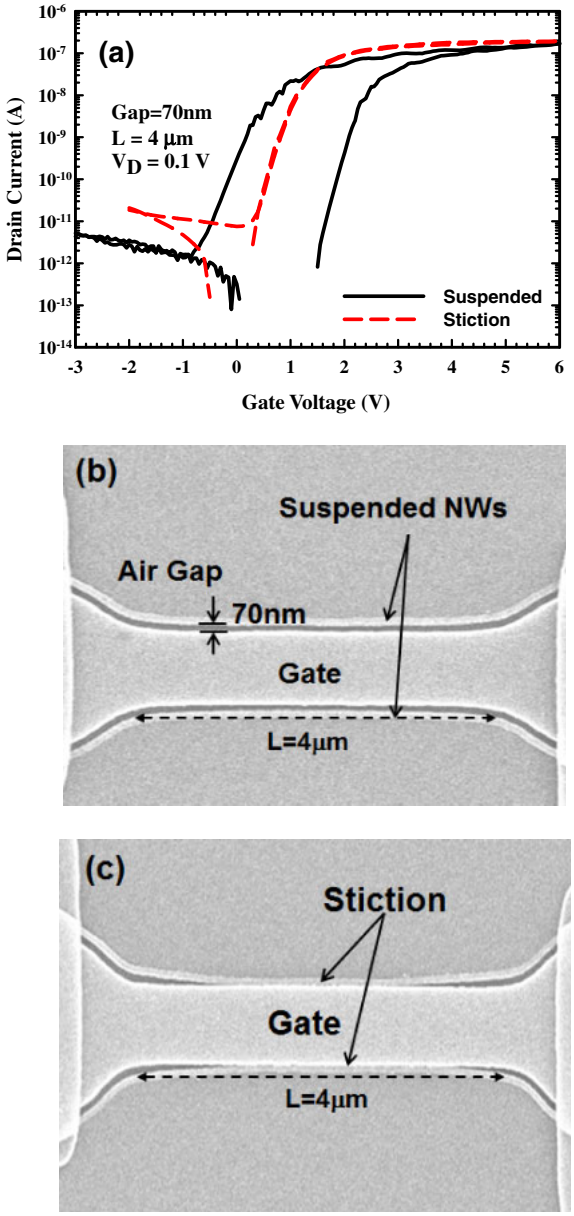

Fig. 5. (Color online) (a) Transfer characteristics of the fabricated devices with and without stiction. Corresponding SEM images of the devices (b) without and (c) with stiction.

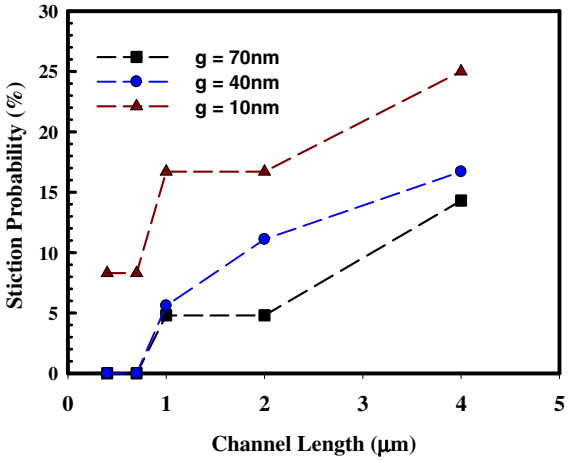

Fig. 6. (Color online) Stiction probability as a function of channel length for released suspended-NW-channel FETs.

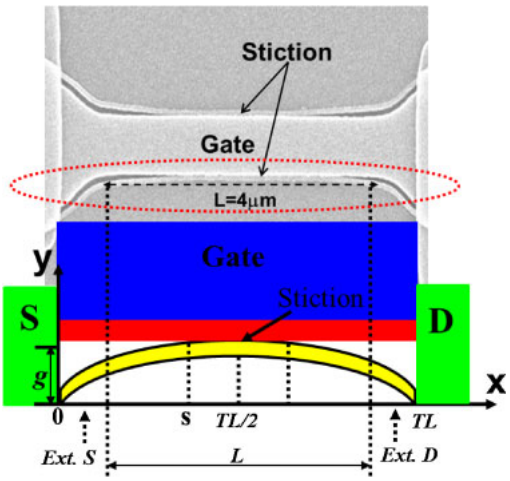

Fig. 7. (Color online) Top-view diagram of suspended-NW channel adhering to gate nitride.

system as stiction occurs, as schematically shown in Fig. 7. The elastic energy arises from the distortion of the NW channel, and the distortion results in a repulsive force on the NW channel. Such a repulsive force is balanced by the attractive force due to the adhesion energy between the two contact objects. Major dimensional parameters indicated in the figure are defined as follows: Ext S/D regions are the source/drain extension parts, and TL is the total length of the suspended nanowire including the channel and the source/drain extension parts, i.e., $TL = L + 2\text{Ext S/D}$, w and t are the width and thickness of the NW channel, respectively, and g is the initial gap thickness. The x- and y-directions are parallel and perpendicular to the source-to-drain direction, respectively. In Fig. 7, $x = 0$ corresponds to the end of the external source. It is assumed that the channel is in contact with the gate nitride from $x = s$ to $TL - s$ with a bended shape symmetrical to $x = 0.5TL$. Note that $s < 0.5TL$ for stiction to occur. The displacement of the NW channel from the equilibrium position along the y-direction is expressed as $u(x)$. To simplify the analysis, we approximate $u(x)$ with the following form:

$$u(x) = \begin{cases} g\sin\left(\dfrac{\pi}{s}x\right) & \text{for } 0 \le x \le s, \\ g & \text{for } s \le x \le \dfrac{TL}{2}. \end{cases} \quad (1)$$

The elastic energy U_E stored in the distorted suspended NW channel is then given by[22)]

$$U_E = \frac{EI}{2}\int_0^{TL/2} 2\left[\frac{d^2u(x)}{dx^2}\right]^2 dx, \quad (2)$$

where E is Young's Modulus and I is the area moment of inertia. As shown in Fig. 4, the cross-sectional shape of the NW is like a quadrant with the radius of w, so the area moment of inertia could be expressed as[23)]

$$I = \left(\frac{\pi}{16} - \frac{4}{9\pi}\right)w^4 = \alpha w^4. \quad (3)$$

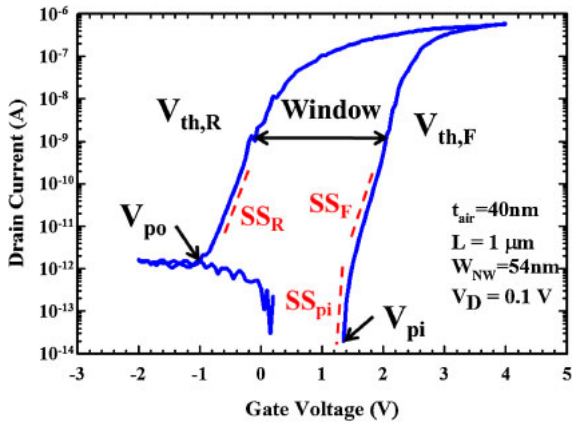

Fig. 8. (Color online) Hysteresis characteristics of the suspended-NW-channel device under forward and reverse sweeping.

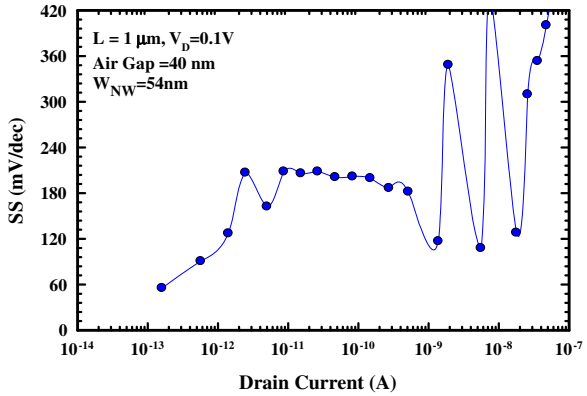

Fig. 9. (Color online) SS as a function of I_D for the device characterized in Fig. 8.

Equation (2) is solved with the boundary conditions of $u(0) = 0$ and $u(s) = g$ and has the solution

$$U_E = \frac{E\alpha\pi^4 w^4 g^2}{2s^3}. \quad (4)$$

On the other hand, surface adhesion energy[22] (only stored in the contact part, namely, $s \le x \le TL - s$) is given by

$$U_S = -\gamma_s w(TL - 2s) \text{ as } s < 0.5TL, \quad (5)$$

where γ_s is the effective adhesion energy per unit area in the contacted portion, and $w(TL - 2s)$ is the contact area. Note that the value of U_S may vary from device to device and is essential in determining the occurrence of stiction. It depends on the surface conditions,[24,25] such as the surface roughness and formation of native oxide, of the contact materials (nitride and poly-Si NW channel). For stiction to occur, γ_s must be larger than a threshold value, and the extent of the contact area (or s) depends closely on γ_s. In equilibrium, the total energy (U_T) of the system should be minimal, which can be defined as[22]

$$\frac{dU_T}{ds} = \frac{d(U_E + U_S)}{ds} = 0. \quad (6)$$

Substitution of Eqs. (4) and (5) into Eq. (6) yields

$$s = \left(\frac{3E\alpha\pi^4 w^3 g^2}{4\gamma_s}\right)^{1/4}. \quad (7)$$

To prevent stiction, the restoring force executed by the bended NW must be sufficiently large to overcome the sticking force executed by the surface adhesion energy, which is dependent on γ_s and the contact area $w(TL - 2s)$ [Eq. (5)]. As mentioned above, s is smaller than $0.5TL$ as stiction happens (Fig. 7). To address this point, Eq. (7) can be further modified to express γ_s as a function of the structural parameters, and then the threshold value γ_s^* for stiction to happen can be defined as

$$\gamma_s = \frac{12E\alpha\pi^4 w^3 g^2}{s^4} \ge \frac{12E\alpha\pi^4 w^3 g^2}{(0.5TL)^4} = \gamma_s^*. \quad (8)$$

The above expression indicates that γ_s^* increases with increasing g and decreasing TL (or L). The predicted trends are consistent with the results shown in Fig. 6, that is, the stiction probability increases as L increases or g decreases.

4. Electrical characteristics of suspended-NW-channel TFTs

4.1 Hysteresis characteristics

Figure 8 shows the typical hysteresis characteristics of a suspended-NW-channel device with a channel length of 1 μm and an air-gap thickness of 40 nm. Definitions of several major electrical parameters are shown in the figure and described as follows. During the forward sweeping, the gate voltage (V_G) corresponding to a jump in drain current (I_D) is defined as the pull-in voltage V_{pi}. The pull-out voltage V_{po} is defined as V_G when I_D drops to the level dominated by the off-state leakage during the reverse sweeping measurement. The threshold voltage V_{th} is simply defined as V_G when I_D reaches 1×10^{-9} A. The hysteresis window is defined as the difference in V_{th} between the forward ($V_{th,F}$) and reverse sweeping ($V_{th,R}$) measurements. SS values of different subthreshold regions are denoted as SS_F, SS_R, and SS_{pi}, as specified in the figures. Among the parameters, SS_{pi} is the smallest.

The operation of the suspended-NW-channel device is described as follows: In the forward sweeping measurement, an abrupt increase in I_D at V_{pi} (1.35 V in the figure) and then an ultra low SS_{pi} of 55 mV/dec are observed. This is an indication that the pull-in action of the suspended-NW channels is triggered by the increase in gate voltage. However, unlike the observation reported in a previous work on SG-MOSFET[5] that the rise in I_D is dramatic and sudden, the current remains at a modest level after pull-in and continuously increases with increasing V_G. This is ascribed to the fact that the current jump is limited by the small contact region at the channel center during the initial pull-in stage.[19] After pull-in, the contact area of the NW channel with the side gate gradually increases with increasing gate voltage, so does the drain current. The aforementioned action reflects on the subthreshold characteristics of the device. In Fig. 9, SS is shown as a function of I_D. The transition from a low-SS region corresponding to the pull-in action to the relatively stable region with a higher SS results from the aforementioned process. More interestingly, in Fig. 9, we can also see that the SS seems to oscillate in the I_D region between 10^{-9} and 10^{-7} A. This finding implies that the vibration action of the suspended subject may take place as it is in contact with the gate nitride, although the process is complicated and needs further study.

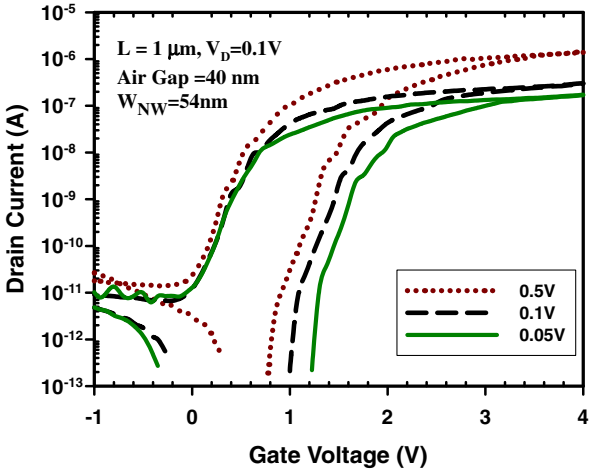

Fig. 10. (Color online) Hysteresis curves of suspended-NW-channel FETs with drain voltages of 0.05, 0.1, and 0.5 V.

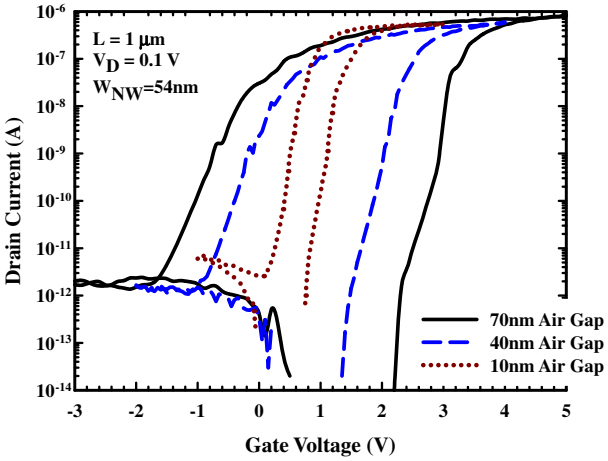

Fig. 11. (Color online) Hysteresis curves of suspended-NW-channel FETs with air gap thicknesses of 70, 40, and 10 nm.

In the reverse sweeping measurement, owing to the fact that the charges that were induced during the forward sweeping still reside in the channel,[19] $V_{th,R}$ is significantly lower than $V_{th,F}$. Moreover, no abrupt current drop is seen in the reverse sweeping. This indicates that the detachment of the NW channels occurs gradually. Another feature is the asymmetric SS of forward and reverse sweeping. As shown in Fig. 8, the SS_F (~198 mV/dec) extracted in the I_D range from 10^{-11} to 10^{-9} A is steeper than that in the reverse sweeping ($SS_R \sim 245$ mV/dec). This effect can be explained by the appearance of an additional adhesive force as the channel is in contact with the gate nitride.[26] This force tends to impede the detachment of suspended NWs from the gate nitride. As a result, a significant degradation in SS during the reverse sweeping can be observed. Finally, as the gate voltage is sufficiently low, the channel is eventually released and the device returns to the open-gap state.

The measured hysteresis characteristics with various drain voltages (V_D) are illustrated in Fig. 10, which shows that an increase in V_D tends to reduce V_{pi}. A higher V_D means that the electrons are easier to be dragged into the channel from the source and thus facilitate the pull-in of the channel. On the other hand, the pumping out of the stored electrons in the channel during the pull-out period is faster as V_D increases, resulting in a more positive V_{po}, as shown in the figure, although the effect is less profound than that for V_{pi}.

4.2 Effects of air gap thickness

Figure 11 shows the hysteresis characteristics of the fabricated devices with various air gap thickness of 10, 40, and 70 nm. The air-gap thickness dependence on pull-in voltage has been briefly discussed in our previous work,[27] in which it was found that a smaller gap thickness led to a smaller pull-in voltage owing to the smaller electrostatic force needed to be overcome. Another important indicator of the switching characteristics is the SS; the extracted results (SS_{pi}, SS_F, and SS_R) are plotted as a function of air gap thickness in Fig. 12. As can be seen, the device with a 70 nm air gap thickness shows a smaller SS_{pi} than the others with a smaller air gap thickness. This observation is reasonable as the increase in drain current after pull-in increases with increasing gap thickness.

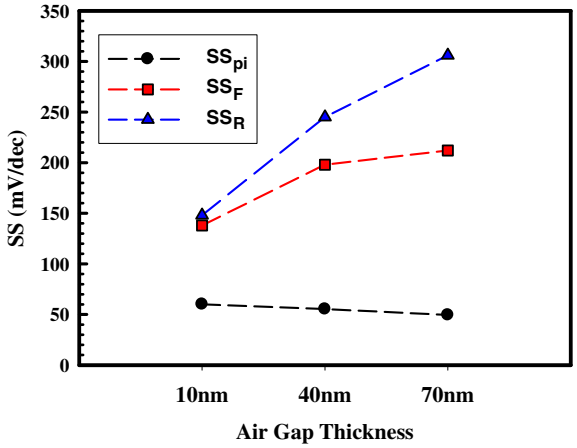

Fig. 12. (Color online) Extracted SS of suspended-NW-channel FETs with air gap thicknesses of 70, 40, and 10 nm.

Nevertheless, SS_F and SS_R exhibit trends opposite to that of SS_{pi}, as shown in Fig. 12. As has been mentioned, SS_F and SS_R are extracted in the drain current range of 10^{-11}–10^{-9} A where the portion of the NW channel in contact with the gate nitride is modulated by the gate voltage. At this stage, for the device with a larger gap thickness, a larger resilient force is exerted on the channel owing to the larger displacement. This affects the capability of the applied gate voltage to manipulate the channel; thus, SS is degraded. In addition, it can be seen that pull-out voltage (V_{po}) becomes more negative for devices with a larger gap thickness. This is attributed to the high adhesive force, which is present as the channel contacts the gate nitride. It prevents the detachment of the NW channel from gate nitrides; therefore, an additional repulsive electrostatic force by negative gate bias is needed to effect the detachment.

4.3 Reliability characteristics

In this section, we address the endurance properties of the fabricated devices. Figure 13(a) shows the typical endurance characteristics of a device in which the threshold voltages under forward and reverse modes were recorded during the cycling tests. The air gap of the device is 40 nm. In the figure,

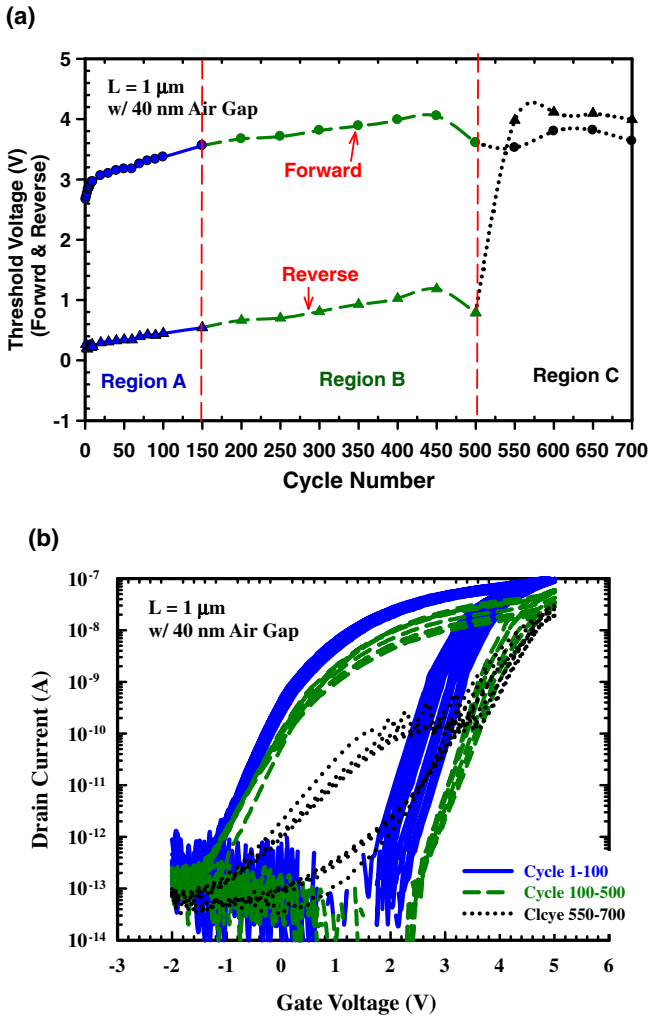

Fig. 13. (Color online) (a) Typical endurance characteristics of suspended-NW-channel FET with air gap thickness of 40 nm. (b) Hysteresis *I–V* curves of test device selected from several cycles of measurements.

three stages denoted as regions A, B, and C are identified. In regions A (cycles 1–100) and B (cycles 100–500), both $V_{th,F}$ and $V_{th,R}$ slightly increase with increasing number of cycles. To gain more insight into these results, Fig. 13(b) shows the I_D–V_G curves of the device measured at various number of cycles. It can be seen that there is no obvious change in SS in the first 100 cycles (blue solid curves); thus, the V_{th} shift induced in this stage is mainly attributed to the electron trapping in the nitride layer[28–30] while the interface degradation can be neglected. However, from cycles 100–500 (green dashed curves), both $V_{th,F}$ and $V_{th,R}$ increase and accompanied by a rise in the subthreshold swing, as shown in Fig. 13(b). This indicates that the interface degradation is no longer negligible. When the cycle reaches beyond 500, $V_{th,F}$ and $V_{th,R}$ become comparable and even show a reverse order while the occurrence of the hysteresis is limited to the current $<10^{-10}$ A. These are signs of device failure. The failure is attributed to the accumulation of degradation induced in the dielectric and at the interface. To improve the endurance, improving the quality of the gate dielectric is essential.

Figure 14 shows the endurance characteristics of a device with a larger air gap of 70 nm. It is seen that obvious window shrinkage occurs just after 60 cycles. The measured transfer curves of the device (data not shown) indicate that the

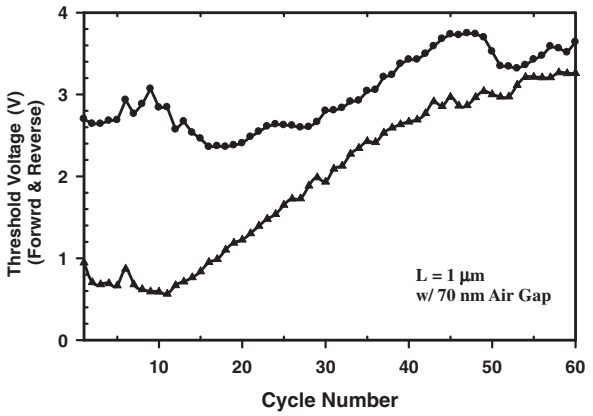

Fig. 14. Endurance characteristics of suspended-NW-channel FET with air gap thickness of 70 nm.

degradation is primarily due to the increase in the subthreshold swing of the device. The performance is much worse than the results shown in Fig. 12. A similar observation was also documented previously[31] and the cause is attributed to the larger strain resulting from the larger displacement of the channels during operation. The deformed channel is expected to suffer from the larger stress as the gap is thicker; consequently, a larger number of surface defects are generated in a limited number of operation cycles, leading to the quick shrinkage in the widow, as shown in Fig. 14. In short, although a thicker gap tends to improve the stiction issue as demonstrated in Sect. 3, it would also deteriorate the reliability of the devices. These results indicate that there exists a tradeoff between device performance and yield in selecting the gap.

5. Conclusions

Novel devices with suspended poly-Si NW channels were fabricated and characterized in this study. In this scheme, the suspended poly-Si NW channels are separate from the side gate by a nanometer-scale air gap. Owing to the low ratio of the etch depth to the thickness of the sacrificial layer, simple wet etching can be performed to release the NW channel. Stiction of the NW channels after the release process is observed and its occurrence destroys the hysteresis operation of the device. Fortunately, the problem can be eliminated as the channel is sufficiently short or the air gap is sufficiently thick.

From the hysteresis characteristics of the devices, an SS smaller than 60 mV/dec is observed at the pull-in point. The effects of gap thickness on device performance are also addressed in this work. The endurance test confirms that successful operation of the devices can be repeated retained more than 500 times. Accumulation of degradation inside and on the surface of the gate dielectric would lead to the collapse of the hysteresis characteristics.

Acknowledgments

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