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Improved high-temperature switching characteristics of Y_2O_3/TiO_x resistive memory through carrier depletion effect

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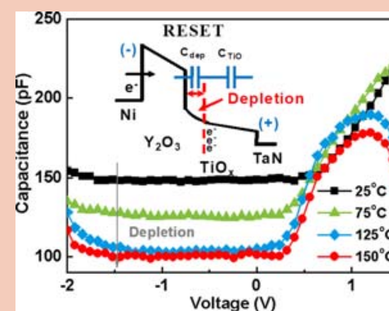
We report a stacked Y_2O_3/TiO_x resistive random access memory (RRAM) device, showing good high-temperature switching characteristics of extremely low reset current of 1 μA at 150 °C, large off/on resistance window (>200) at 150 °C, large rectification ratio of ~300 at 150 °C and good current distribution at 85 °C. The good rectifying property, lower high-temperature sneak current and tighter high-temperature current distribution can be attributed to the combined results of the oxygen vacancies in TiO_x and the related carrier depletion effect.



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1 Introduction Since the technology node scales down with the continuous trend of nonvolatile memory (NVM) toward high density, fast speed and low power consumption, the conventional flash memory [1–3] has approached technical and physical limitations. Recently, non-charge based resistive random access memory (RRAM) [4–21] has attracted much attention as one of the most promising candidates in the next-generation NVM application, due to its simple structure, low cost, high switching speed, low power consumption and high compatibility with the complementary metal–oxide–semiconductor (CMOS) processes. However, due to the barrier height lowering at high temperature, the apparent degradation on sneak current and current distribution are major challenges, especially for the scaled one-diode–one-resistor (1D1R) RRAM crossbar arrays. Therefore, the RRAM devices with excellent high-temperature switching characteristics are of great importance for production. Here, from our experimental results, we found that the conventional filament conduction mechanism might suffer from high-temperature leakage issues including large switching current, wide current distribution and high sneak current. The sneak current in resistive crossbar memory is an inherent disadvantage and urgently needs to be solved. Therefore, we proposed a Y_2O_3/TiO_x RRAM device, showing good high-temperature switching characteristics of the self-compliance function, an extremely low reset power of ~1 μW at 150 °C, good current distribution at 85 °C and large rectification ratio of ~300 at 150 °C. The improvement in high-temperature performance is mainly ascribed to the adoption of stacked Y_2O_3/TiO_x and the unique carrier depletion effect in TiO_x during switching. The present results show high potential for future high-performance memory application.

2 Experimental procedure The proposed $Ni/Y_2O_3/TiO_x/TaN$ RRAM devices with metal–insulator–metal (MIM) structure were fabricated as follows. First, 100 nm

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thick TaN was prepared by sputtering as the bottom gate on the SiO_2/Si substrate. After that, 15 nm thick TiO_x and 8 nm thick Y_2O_3 films were deposited using e-gun evaporation. Finally, 50 nm thick Ni was formed and patterned as the top electrodes, which provides high work function (5.1 eV) and works as a low-cost solution for high-κ DRAM capacitors [22]. The fabricated devices were characterized by current–voltage (I–V), capacitance–voltage (C–V), cycled endurance and X-ray photoelectron spectroscopy (XPS) measurements. To precisely analyze film bonding, the film samples were pretreated by using in-situ Ar bombardment for 10 s at a low vacuum base pressure of 8×10^{-8} torr to remove the native oxide on the sample surface.

3 Results and discussion Figure 1(a) shows the swept I–V characteristic of the RRAM devices with a single-layer TiO_x and Y_2O_3/TiO_x, respectively, which both show counterclockwise bipolar switching behaviors. The asymmetric I–V curves are attributed to the different work-functions between top Ni and bottom TaN electrodes. It is clearly to observe that the set and reset currents are large for single-layer TiO_x RRAM device. However, the switching currents can be further improved after large bandgap Y_2O_3 capping. The large bandgap Y_2O_3 dielectric owns large conduction band offset that can form a large barrier

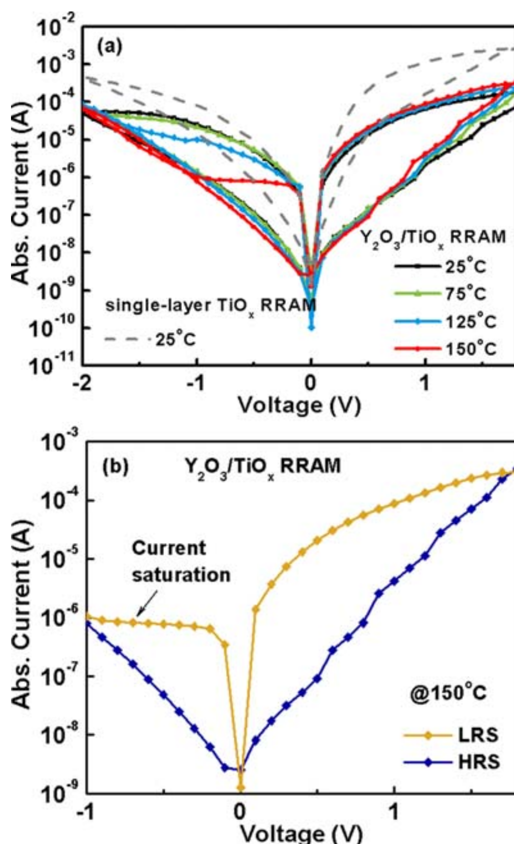

Figure 1 (a) Temperature-dependent I–V characteristics and (b) swept I–V curve at 150 °C of Y_2O_3/TiO_x RRAM device.

height with TiO_x to lower high-resistance state (HRS) and low-resistance state (LRS) currents. In addition, the forming-free and self-compliance functions for set/reset currents are also observed, which can simplify the array operations. No electroforming process is required for the Y_2O_3/TiO_x RRAM device. This forming-free property could be attributed to the abundant oxygen vacancies pre-existing in the TiO_x, which forms a low-voltage conductive path during the first switching from HRS to LRS. Thus, in comparison with single-layer TiO_x RRAM, the stacked Y_2O_3/TiO_x RRAM exhibits a larger resistance memory window of ~50 at a reading voltage of 0.5 V and lower set and reset powers. The temperature dependence of the I–V characteristics was also measured as shown in Fig. 1(a). In the reset process, a decreasing current trend (positive temperature coefficient; TC) is apparently observed from 25 °C to 150 °C in LRS. The positive TC indicates that the current transport in LRS is mainly governed by filament conduction. The filamentary switching in the TiO_x via Ti interstitial ions has been proposed in metal-oxide RRAM [16]. Furthermore, it is worthy to note that the reset current can reach a saturated current of 1 μA (current saturation), as shown in Fig. 1(b), which is unique and different to conventional filamentary RRAM. From the right I–V plot measured at 150 °C, we observe that the high-temperature I–V curve in HRS is similar to that of DRAM capacitor with MIM structure, which is dominated by asymmetric electrodes and less affected by bulk vacancies. However, the I–V curve in LRS shows the rectified properties of MIS (metal–insulator–semiconductor) or MS (metal–semiconductor) structures, suggesting that the LRS current at high temperature of 150 °C is not only determined by metal filament, but also related to interface junction leakage in this dielectric stack.

To explain the operation mechanism at high temperature, Fig. 2(a) displays the calculated active energy (E_a) for Y_2O_3/TiO_x RRAM device according to the HRS and LRS resistances at different temperatures (from 25 °C to 125 °C), which are obtained at 0.5 V read under 1.8 V set/–2 V reset operations. The extracted results reveal negative E_a values for the device (E_a(HRS) = –0.02 eV, E_a(LRS) = –0.05 eV), which implies that the conduction behaviors are metallic (positive TC) in TiO_x [23, 24]. Although the Ni/Y_2O_3/TaN device has no RRAM memory property, this metallic behaviour has been confirmed in Ni/TiO_x/TaN device. The amorphous TiO_x with incomplete bonding is expressed by the following equation: $Ti–O_x^* \rightarrow V_{Ti-O_x}^{2+} + 2e^- + Ti–O_x$, where $V_{Ti-O_x}^{2+}$ indicates the oxygen vacancies in TiO_x that dominate the resistive switching characteristics.

To further test the feasibility of the Y_2O_3/TiO_x RRAM at high temperature, we measured the HRS/LRS current distributions at 85 °C, as shown in Fig. 2(b). The current distribution measurements were performed under 60 μs pulses at 1.8 V set/–2 V reset voltages for 100 cycles. Here, the CV is an index of probability distribution, defined as the ratio of the standard deviation and mean value. Good current distribution for HRS (26%) and LRS (45%) was

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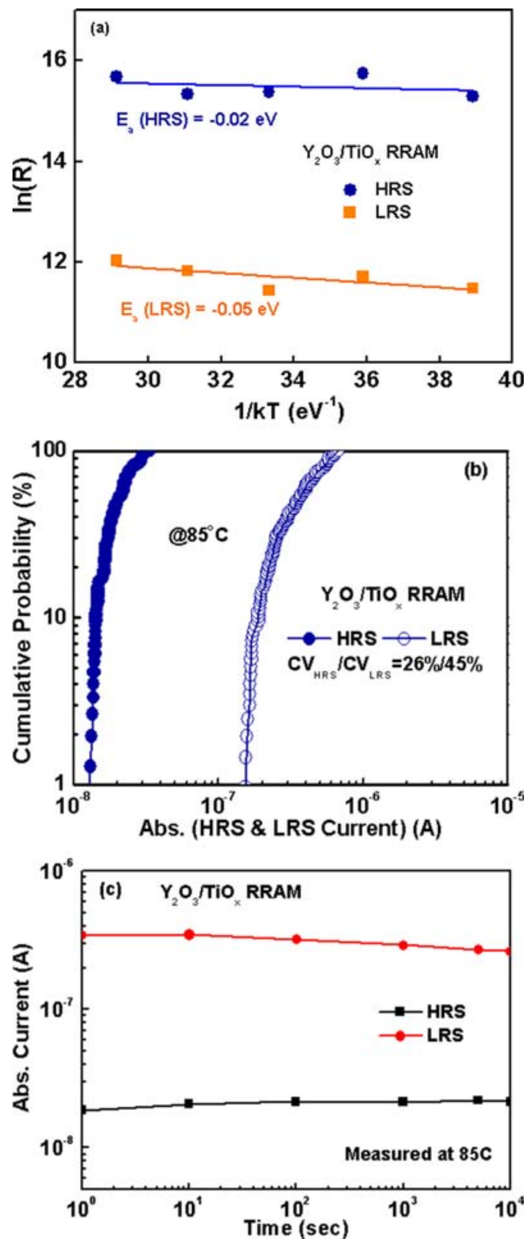

Figure 2 (a) Extracted E_a at HRS and LRS conditions under different temperatures (from 25 °C to 125 °C), (b) current distributions at 85 °C, and (c) 85 °C retention property for Y_2O_3/TiO_x RRAM device.

measured for the devices, indicating that the number of filament paths affects the switching distribution of RRAM. As shown in Fig. 2(c), the small current decays in HRS and LRS were measured for 10^4 s retention at 85 °C. Thus, the stable high-temperature performances are related to the low LRS current switching for less stress via defective films.

Figure 3(a) depicts the forward-to-reverse (FR) current ratio under 1.8 V set/–2 V reset operations, which is essential for achieving a high memory density in crossbar arrays. A FR ratio of ~300 for the devices is measured at 150 °C.

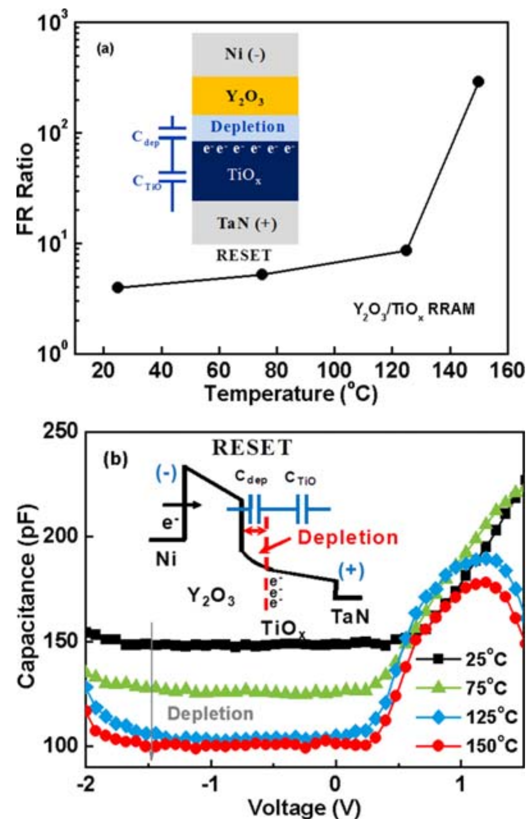

Figure 3 (a) Forward-to-reverse ratios for Y_2O_3/TiO_x RRAM device; inset: formation of the depletion layer. (b) Temperature-dependent *C–V* characteristics for Y_2O_3/TiO_x device; inset: schematic plot of the reset process.

The well rectified characteristic in LRS can effectively alleviate the sneak current in crossbar memory arrays, especially at high-temperature operation. The rectified behavior is believed to be related to depletion effect in n-type TiO_x with narrow bandgap. This is because a large number of thermally excited electrons are generated in n-type TiO_x with increasing the measured temperature from 25 °C to 150 °C. The resulting excess electrons would lower the intrinsic resistance of n-type TiO_x and localize interface electric field to form a depletion layer in TiO_x, as shown in the inset of Fig. 3(a). The carrier depletion phenomenon can be confirmed by *C–V* measurements, as reported in Refs. [25, 26]. Figure 3(b) shows the temperature-dependent *C–V* characteristics for our Y_2O_3/TiO_x device, with the schematic band diagram under reset process in the inset. It is observed that the capacitance decreases with increasing temperature under the reset process using negative bias. The reduction in capacitance with temperature up to 150 °C can be regarded as a capacitance-series effect. The temperature-dependent *C–V* characteristics indicate that the variation in capacitance with temperature directly corresponds to the change of depletion region in electron-rich n-type TiO_x, which is also supported by the temperature dependence of the reduced reset current in Fig. 1(a).

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Table 1 Comparison of device integrity data for RRAM devices with rectified characteristic.

RRAM structure	Ni/HfO$_x$/n$^+$-Si [28]	Ni/AlO$_y$/n$^+$-Si [29]	Au/ZrO$_2$:nc-Au/n$^+$-Si [30]	Ni/Y$_2$O$_3$/TiO$_x$/TaN (this work)
I_{set}@V_{set}	100 μA@2.4 V	–10 μA@–4.5 V	–0.7 A@–4 V	0.2 mA@1.8 V
I_{reset}@V_{reset}	0.6 mA@1.7 V	3 μA@0.7 V	0.8 A@1.2 V	–50 μA@–2 V
off/on ratio	>10^3@25 °C	~5@25 °C	~600@25 °C	>200@150 °C
FR ratio	~500@150 °C	~30@120 °C	~500@25 °C	~300@150 °C
I dist. (CV)	17% (I_{LRS}) 58% (I_{HRS}) @25 °C	compliance (I_{set}) 90% (I_{reset}) @25 °C	69% (I_{LRS}) 74% (I_{HRS}) @25 °C	45% (I_{LRS}) 26% (I_{HRS}) @85 °C

In Fig. 4(a), the in-situ XPS result corresponds to the oxidation state of Y^{3+} (156.8 eV and 158.9 eV), which agrees with stoichiometric Y_2O_3 [27]. The well-oxidized Y_2O_3 as capping layer is helpful to enhance the interface barrier height between Y_2O_3 and TiO_x that is critical for lowering the switching power and unwanted sneak current. Figure 4(b) shows the Ti 2p XPS spectra in the TiO_x. Different Ti ion chemical states are measured in the TiO_x dielectrics. The low-valence Ti atoms with lower binding energy such as Ti^{3+} and Ti^{2+} confirm more oxygen vacancies in the TiO_x dielectric, which provide metallic filaments and high electron carrier density under high-temperature operation.

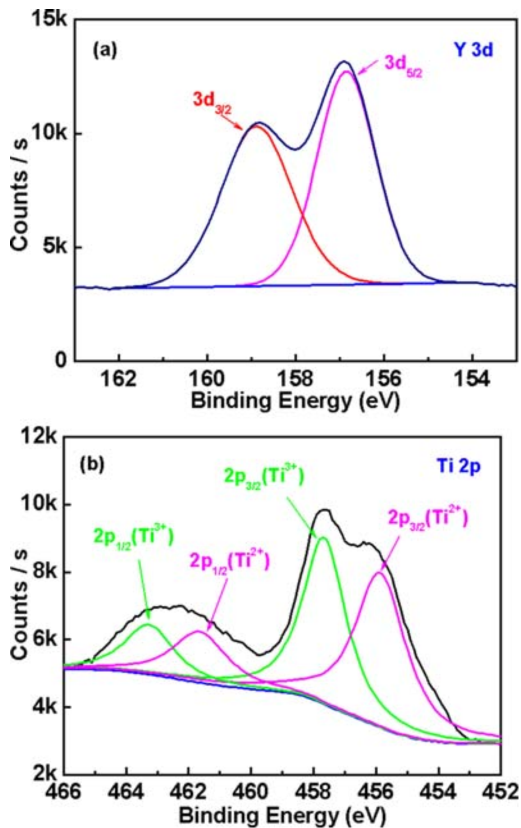

Figure 4 (a) In-situ XPS spectra of Y 3d core level for Y_2O_3 dielectric. (b) XPS spectra of Ti 2p core levels for TiO_x dielectric.

Table 1 shows the comparison of resistive switching characteristics for various RRAM devices with rectified characteristics. It is well known that the sneak current and low FR ratio at high temperature are a major problem due to temperature-induced barrier height lowering. With the combination of oxygen vacancies in TiO_x and the related carrier depletion effect, a large off/on resistance window (>200) at 150 °C, large rectification ratio of ~300 at 150 °C and good current distribution at 85 °C are all reached in our device. More importantly, the CV of high-temperature current distribution at 85 °C is even comparable to those of others measured at 25 °C.

4 Conclusion We reported a Ni/Y_2O_3/TiO_x/TaN RRAM with good high-temperature characteristics. The Y_2O_3/TiO_x device can reach a large off/on resistance window (>200), a large FR ratio of ~300 and a low reset current of 1 μA (reset power ~1 μW) at a high temperature of 150 °C. Such good high-temperature switching characteristics can be explained by the oxygen vacancies in TiO_x and related carrier depletion effect. This is beneficial to improve the high-temperature sneak current in recent 1D1R crossbar arrays and has great promise for future memory application.

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