IOPscience iopscience.iop.org

Home Search Collections Journals About Contact us My IOPscience

# The effects of channel doping concentration for n-type junction-less double-gate poly-Si nanostrip transistors

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2014 Semicond. Sci. Technol. 29 055001

(http://iopscience.iop.org/0268-1242/29/5/055001)

View the table of contents for this issue, or go to the journal homepage for more

Download details:

IP Address: 140.113.38.11
This content was downloaded on 25/12/2014 at 03:08

Please note that terms and conditions apply.

Semicond. Sci. Technol. 29 (2014) 055001 (7pp) doi:10.1088/0268-1242/29/5/055001

# The effects of channel doping concentration for n-type junction-less double-gate poly-Si nanostrip transistors

**Keng-Ming Liu[1], Fan-I Peng[2], Kang-Ping Peng[1], Horng-Chih Lin[2] and Tiao-Yuan Huang[2]**

[1] Department of Electrical Engineering, National Dong Hwa University, Hualien 974-01 Taiwan
[2] Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300 Taiwan

E-mail: kmliu@mail.ndhu.edu.tw and hclin@faculty.nctu.edu.tw

Received 31 December 2013, revised 12 February 2014
Accepted for publication 20 February 2014
Published 28 March 2014

**Abstract**

In this study, novel n-type double-gate (DG) junction-less (J-less) polycrystalline silicon (poly-Si) nanostrip transistors with different channel doping concentrations ($N_C$) have been fabricated and investigated. The effects of channel doping concentration on device characteristics were examined comprehensively in this work. The experimental data show that as the channel doping concentration of the J-less device increases, the threshold voltage ($V_{TH}$) becomes more negative. Besides, the drain-induced barrier lowering and the subthreshold swing of the J-less transistors become larger as the channel doping increases. We also found that as the channel doping increases, the off-current ($I_{OFF}$) increases and the on-current ($I_{ON}$) actually decreases due to the doping-dependent mobility degradation. The conduction mechanisms under different channel doping concentrations were also investigated by TCAD simulation. The experimental results suggest that the n-type DG nanostrip J-less transistor with lower channel doping will have superior device characteristics.

Keywords: double gate, channel doping, junction-less transistor, poly-Si, nanowire

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Over the past decades, the size of metal-oxide-semiconductor field-effect transistors (MOSFETs) has continually been shrunk. A traditional MOSFET contains two p–n junctions and between the two junctions the effective channel length is defined. To mitigate the short-channel effects (SCEs), the ultra-sharp and ultra-shallow source/drain (S/D) junctions were introduced. However, this solution poses severe constraints regarding the doping techniques and the thermal budgets [1, 2]. Another remedy for SCEs is the nonplanar device structures with the multiple-gate configuration such as the FinFET structure. The channel regions of most modern FinFETs are lightly doped or even intrinsic to minimize the device variability caused by random dopant fluctuation [3] and their S/D regions are formed by doped epi growth. Therefore, for the modern FinFETs, the precisely-controlled doping profiles for the S/D p–n junctions are intentionally avoided. Nevertheless, the adjustment of the threshold voltage ($V_{TH}$) of the modern FinFETs relies on the different work functions of the gate materials which make $V_{TH}$ adjustment difficult and costly. Recently, a lot of attention has been paid to junction-less (J-less) transistors, which feature the same type of heavy doping across the S/D and the channel [4–9]. For J-less transistors, of course, the precisely-controlled p–n junctions are avoided. Furthermore, there are some advantages for J-less devices compared with the inversion mode devices reported in the literature, such as lower electric field and higher mobility [5–8]. In fact, J-less devices have been investigated for applications in flash memory [10–12] and DRAM [13, 14].

The operation mechanism of J-less devices is quite different from that of the conventional inversion-mode (IM)

 © 2014 IOP Publishing Ltd Printed in the UK

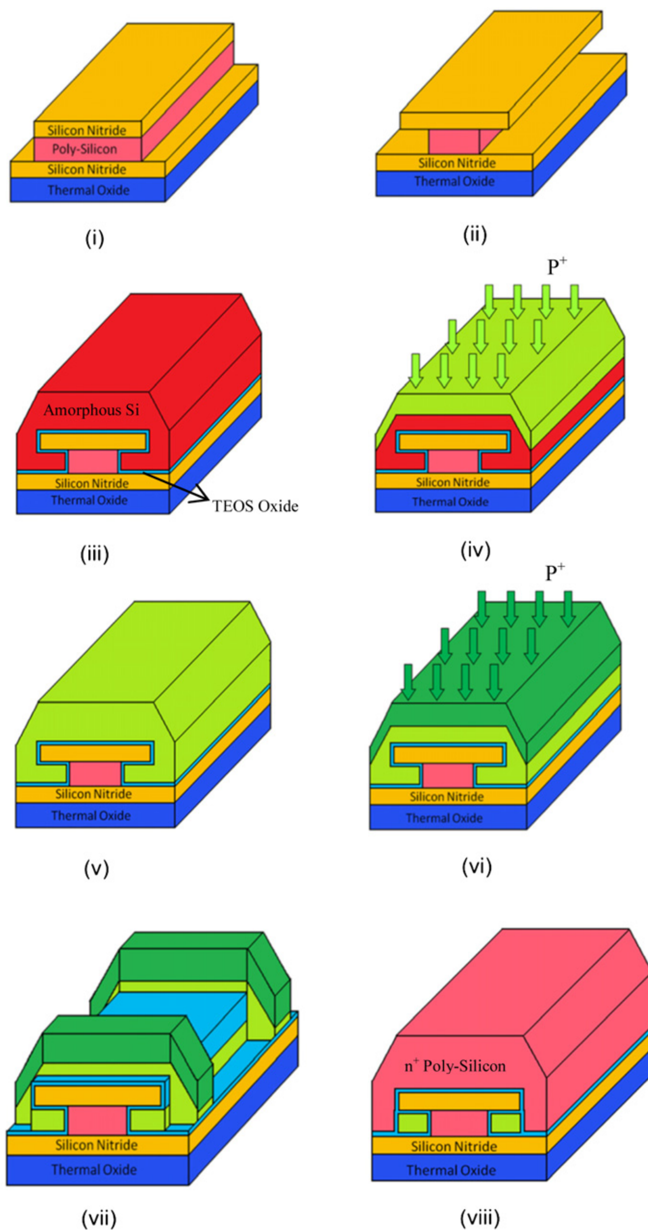


**Figure 1.** Schematic process flow of the p-type IDG J-less poly-Si nanostrip transistor.

devices [5, 7, 15–17]. Unlike IM devices, most of the conducting carriers of the J-less devices are away from the gate/channel interface and thus, lower surface scattering rate is expected. On the other hand, to effectively turn off the J-less devices, the channel layer must be thin enough to allow full depletion of carriers in the channel. The multiple-gate configuration can be further applied on the J-less devices to improve the gate controllability and suppress the SCEs. Although the theoretical and simulation works of J-less transistors are many [4, 6, 8, 16–20], comprehensive experimental studies on J-less transistors are still few. In this work, we fabricated, measured and analyzed n-type J-less double-gate (DG) nanostrip transistors with different channel doping concentrations ($N_C$). Besides comprehensive examination of the effects of channel doping concentration on J-less device characteristics, we will discuss the conduction mechanisms of J-less devices under different channel doping concentrations. This paper is organized as follows. In section 2, we briefly introduce the fabrication of n-type J-less DG poly-Si nanostrip transistors. In section 3, we will present and discuss the electrical characteristics of the fabricated devices with different channel doping concentrations. The effects of channel doping on device characteristics will be examined comprehensively. The conclusions will be drawn in the final section.

## 2. Device fabrication

Figure 1 shows the process flow of the n-type J-less DG poly-Si nanostrip transistor which basically follows the process of the previously published n-type DG poly-Si nanostrip transistor [21]. The fabrication started on Si wafers capped with a 1000 nm thick thermal oxide. First, a stack consisting of SiN (60 nm)/*in situ* doped $n^+$ poly-Si (100 nm)/SiN (50 nm) was deposited. After an anisotropic patterning of top SiN/poly-Si (figure 1(i)), a chemical plasma etching with high selectivity to SiN was used for lateral etching of the poly-Si (figure 1(ii)) to form nanometer-level cavities at the two sides of the stack. Note that the remaining $n^+$ poly-Si serves as the first gate of the completed device. Then a 15 nm thick TEOS oxide and a 100 nm thick amorphous-Si (a-Si) were deposited to fill the nanometer-level cavities. The a-Si was subsequently transformed into polycrystalline by a 600 °C annealing in $N_2$ ambient for 24 h (figure 1(iii)). Subsequently an ion implantation with phosphorus at the doses of $5 \times 10^{13}$, $4 \times 10^{14}$, and $1 \times 10^{15}$ cm$^{-2}$ was performed (figure 1(iv)), and then the samples were annealed in nitrogen ambience at 900 °C for 30 min to drive the dopants into the nanostrip channels (figure 1(v)). Since the deposition thickness of the a-Si film for the nanostrip channels is 100 nm, the nominal nanostrip channel doping concentrations would be $5 \times 10^{18}$, $4 \times 10^{19}$, and $1 \times 10^{20}$ cm$^{-3}$ for the corresponding implant doses. However, actually the doping concentration of the poly-Si film is not uniform and most of the doped phosphorus atoms would not get into the nanostrip channel region even after the annealing. Based on our process experience and TCAD simulation results [22], we estimate that the actual nanostrip channel doping concentration is only approximately one tenth of the nominal value. To reduce S/D resistances, an additional S/D doping was performed by implanting phosphorus at a dose of $5 \times 10^{15}$ cm$^{-2}$ (figure 1(vi)). To avoid the possible phosphorus diffusion into the nanostrips, the dopant activation was done by the thermal budget of the following processes. We defined the channel and S/D regions by reactive plasma etching (figure 1(vii)), and subsequently the materials for forming the second gate structure including a 15 nm thick TEOS oxide and a 100 nm thick *in situ* doped $n^+$ poly-Si were deposited (figure 1(viii)). The device was completed after standard metallization steps.

The layout of the n-type J-less DG poly-Si nanostrip transistor is shown in figure 2(*a*). Figures 2(*b*) and (*c*) are the cross-section views of the device along the dot-dashed line A–B and the dashed line C–D in figure 2(*a*), respectively.

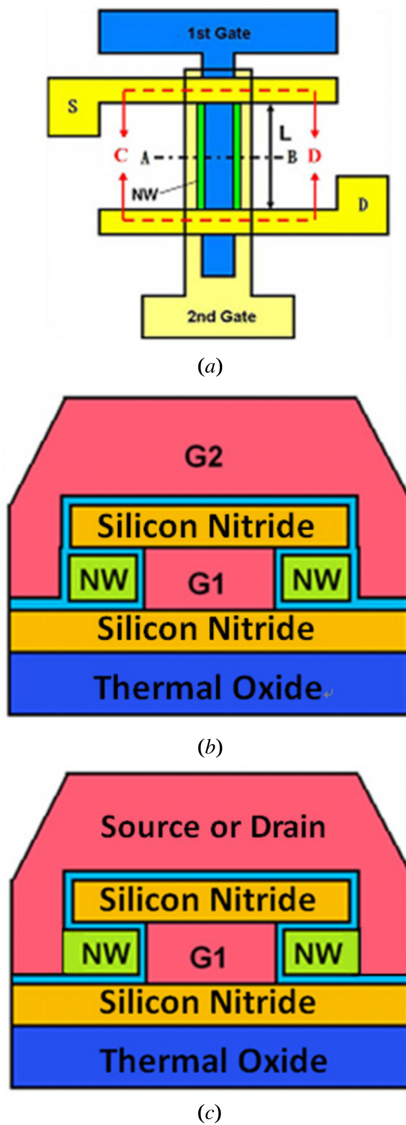


**Figure 2.** (*a*) Top view, (*b*) cross-section view along the A–B line and (*c*) cross-section view along the C–D line of the *n*-type DG J-less poly-Si nanostrip transistor.

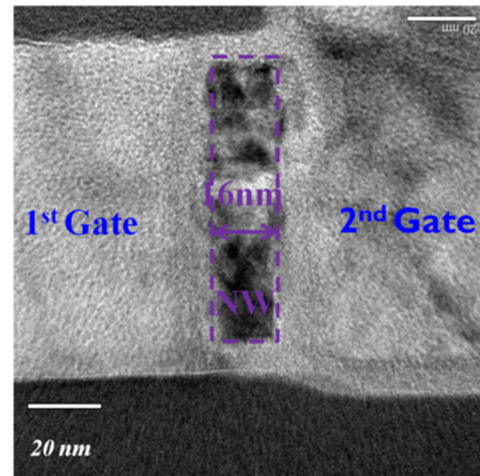


**Figure 3.** The cross-section TEM image of the n-type DG J-less poly-Si nanostrip transistor.

Two poly-Si nanostrips are surrounded by the gate oxide and embedded in the ultra-thin cavities underneath the nitride hard mask as shown in figure 2(*b*). The transmission electron microscopic (TEM) image of the cross-section view of the fabricated J-less transistor is given in figure 3. The horizontal channel thickness ($T_{Si}$) of the rectangular poly-Si nanostrip is observed to be about 16 nm from figure 3. The gate dielectrics is formed by the deposition of 15 nm thick TEOS oxide and the vertical channel width ($W_{Si}$) is about 70 nm since the gate thickness is aimed at 100 nm. The gate material for both gates is $n^+$ poly-Si. In this paper, the channel lengths ($L$) of the J-less transistors are all 400 nm.

## 3. Results and discussion

In this work, the threshold voltage ($V_{TH}$) is defined as the value of $V_G$ when $I_D$ is equal to 5 nA for the 400 nm channel length J-less transistors. The drain-induced barrier lowering (DIBL) is defined as the difference in $V_{TH}$ when $V_D$ is increased from 0.1 V to 1 V. The on-current ($I_{ON}$) is defined as the $I_D$ under the gate overdrive ($V_G - V_{TH}$) equals 1 V and $V_D$ equals 1 V. The off-current ($I_{OFF}$) is defined as the $I_D$ under $V_G - V_{TH} = -0.5$ V and $V_D = 1$ V.

Figure 4 shows the $I_D$–$V_G$ characteristics under $V_D = 0.1$ V and $V_D = 1$ V of the J-less transistors with different channel doping concentrations. Note that the chosen transistors are those whose threshold voltages are closest to the average values for each doping condition. The device characteristics under different channel doping concentrations will be discussed in the following based on the statistics. Figure 5 shows the statistics of the threshold voltages of the J-less transistors with different channel doping concentrations. The numbers of samples for the channel doping concentrations $5 \times 10^{17}$, $4 \times 10^{18}$, and $1 \times 10^{19}$ cm$^{-3}$ are 10, 11, and 24, respectively, which are subject to the device yield. The $V_{TH}$ fluctuation is mainly due to the process variation since the intrinsic variation is insignificant for the dimensions of our devices. The $V_{TH}$ of the n-type J-less transistors becomes more negative as the channel doping concentration increases. This indicates that the higher the channel doping concentration the J-less transistors have, the harder it is for the J-less transistors to be turned off at $V_G = 0$ V. Therefore, a more negative gate bias is necessary to deplete the channel and shut off the leakage current as the channel doping concentration increases.

The conduction mechanisms of the J-less transistors under different channel doping concentrations were examined by the TCAD tools, Sentaurus, from Synopsys [22]. Figure 6(*a*) shows the TCAD simulation results of the electron density distribution along the horizontal channel thickness direction at the middle channel of the J-less transistors with different channel doping concentrations under $V_G$–$V_{TH}$ = 1 V and $V_D$ = 1 V. In the TCAD simulation, the drift–diffusion (D–D) model serves as the transport model with the quantum correction made by density gradient model [22]. Note that, in the TCAD simulation, the nanostrips are assumed to be uniformly doped and the doping concentrations are one tenth

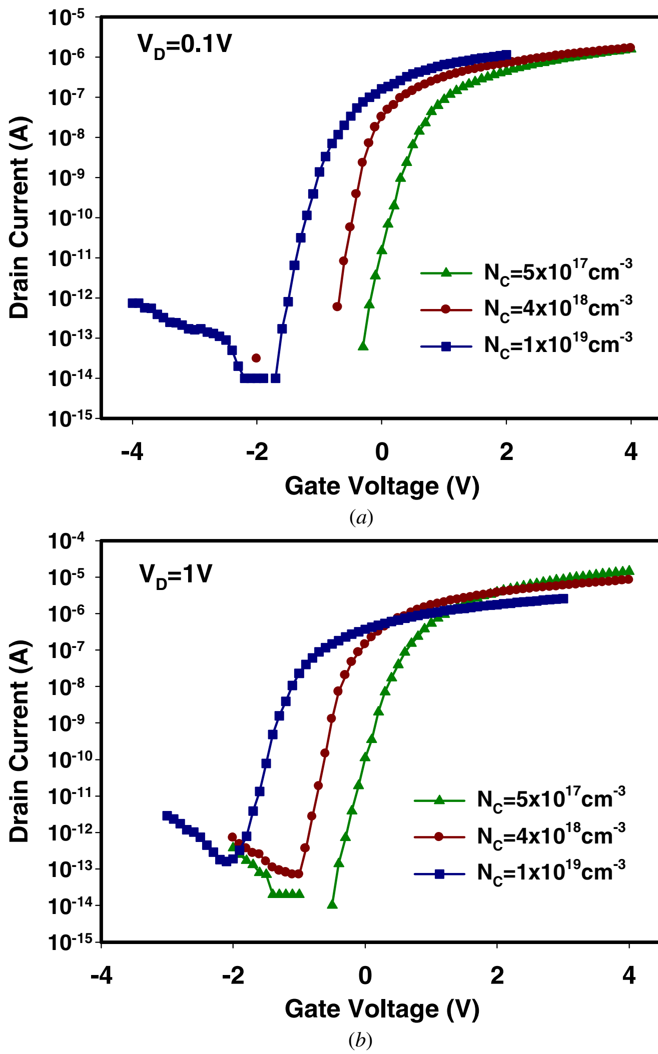


**Figure 4.** The $I_D$–$V_G$ characteristics under (*a*) $V_D = 0.1$ V and (*b*) $V_D = 1$ V of the J-less transistors with different channel doping concentrations. The chosen samples are those whose threshold voltages are closest to the average values for each doping condition.

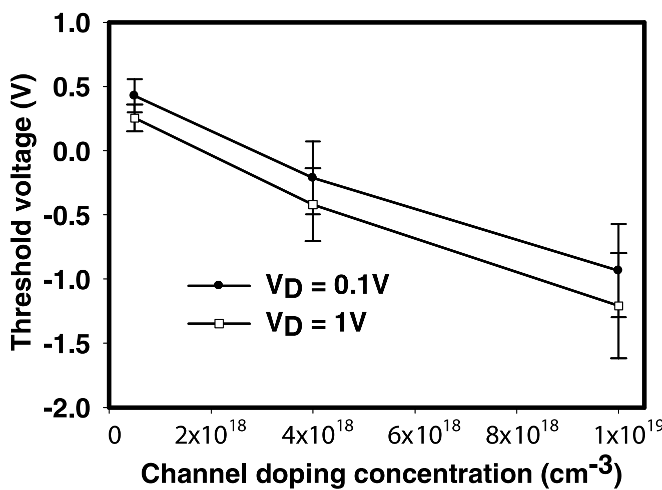


**Figure 5.** The statistics of threshold voltage under different channel doping concentrations for the *n*-type DG nanostrip J-less transistors. The error bar is determined by the standard deviation of the data. The actual channel doping concentration is estimated to be about one tenth of the nominal channel doping concentration.

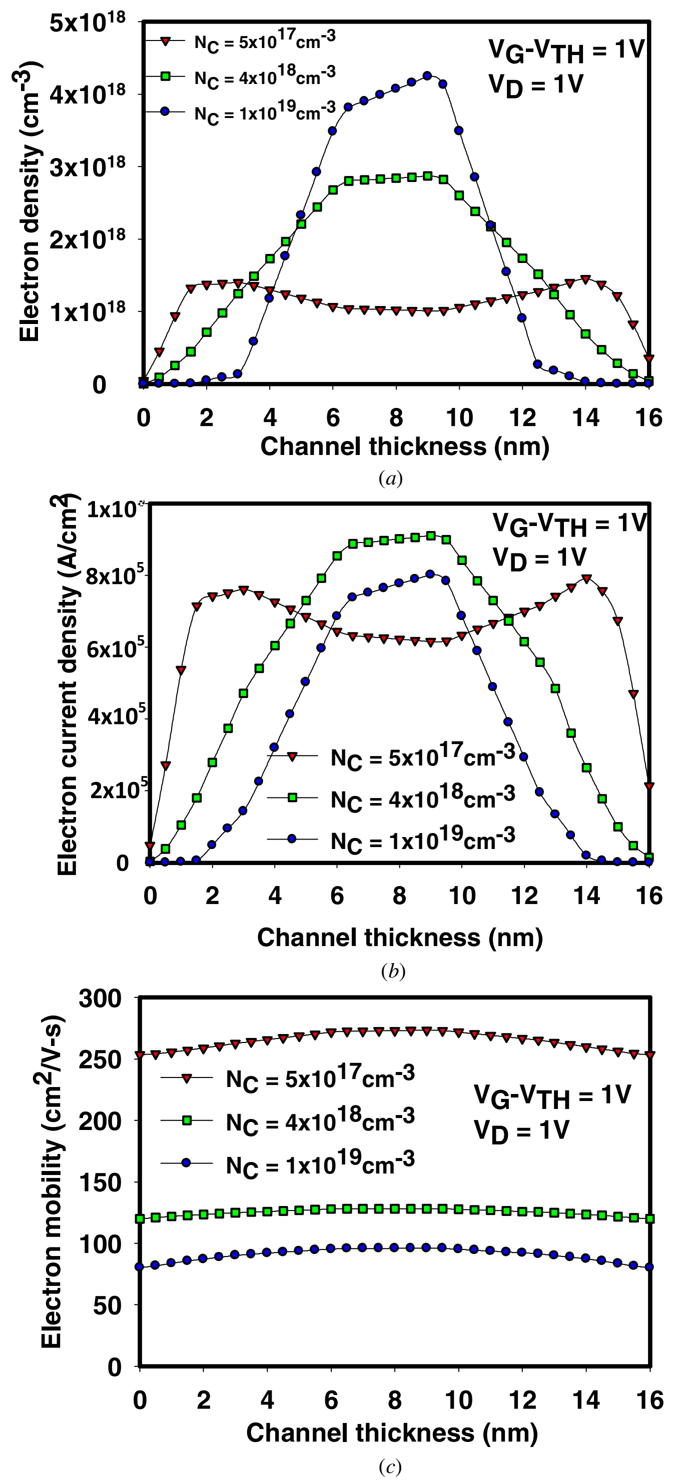


**Figure 6.** The TCAD simulation results of (*a*) the electron density distribution, (*b*) the electron current density, and (*c*) the electron mobility along the horizontal channel thickness direction at the middle channel of the J-less transistors with different channel doping concentrations under $V_G$–$V_{TH} = 1$ V and $V_D = 1$ V.

of the nominal values as mentioned in the previous section. Besides, the doping concentrations of the S/D and gates are set to be n-type $1 \times 10^{20}$ cm$^{-3}$. The geometric structure of the simulated device is identical to the fabricated one. From figure 6(*a*), we can see that for the lower channel

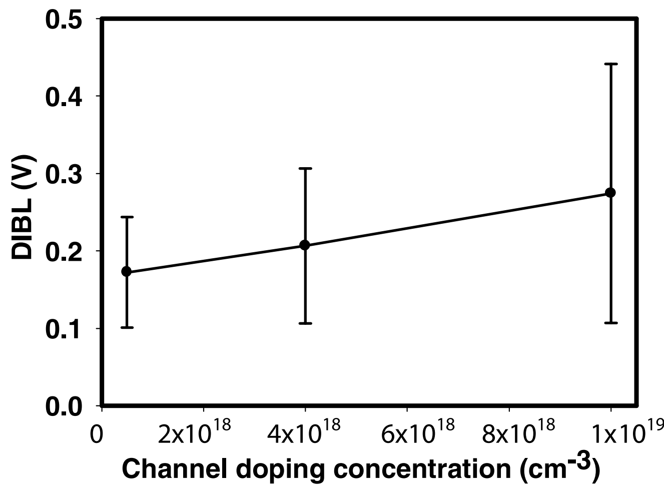


**Figure 7.** The statistics of DIBL under different channel doping concentrations for the *n*-type DG nanostrip J-less transistors. The error bar is determined by the standard deviation of the data.

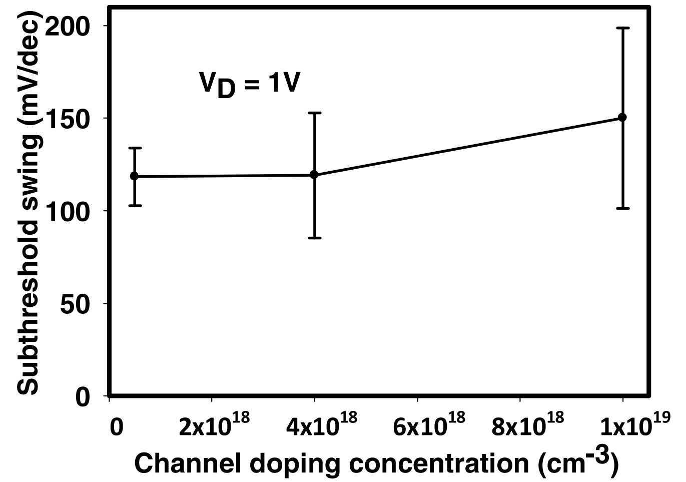


**Figure 8.** The statistics of SS under $V_D = 1$ V for the *n*-type DG nanostrip J-less transistors with different channel doping concentrations. The error bar is determined by the standard deviation of the data.

doping, the conduction current is contributed by both the accumulation layers and the carriers in the central part of the nanostrip. However, as the channel doping increases, the conduction current is only contributed by the carriers in the nanostrip central part. This can be further confirmed by figure 6(*b*), which shows the electron current density along the horizontal channel thickness direction. The transition from the partial accumulation conduction to the complete central-part conduction of our J-less devices is estimated to occur around the channel doping concentration of $10^{18}$ cm$^{-3}$.

Figure 7 shows the statistics of the DIBL of the J-less transistors with different channel doping concentrations. As the channel doping concentration increases, the DIBL value of the J-less transistor becomes larger, i.e., the SCE becomes worse. Figure 8 shows the statistics of the subthreshold swing (SS) under $V_D = 1$ V of the J-less transistors with different channel doping concentrations. The SS of the J-less transistor becomes larger as the channel doping concentration increases. Both phenomena can be explained by figure 9 which shows the two-dimensional electron density distribution at the drain-side end of the gated channel under different channel doping concentrations when $V_G = V_{TH}$ and $V_D = 1$ V. From figure 9, the electron density distribution is more uniform under lower channel doping and more centralized under higher channel doping. That means the average distance between conducting carriers and gate is longer for higher channel doping device. Consequently, the J-less transistors with lower channel doping concentration possess better gate controllability on conducting carriers and hence better DIBL and SS. This can be further confirmed by figure 10, which shows the one-dimensional electron density profiles along the horizontal channel thickness direction at the drain-side end of the gated channel under high/low channel doping concentrations and $V_G = V_{TH}$ or $V_{TH}$ −0.2 V when $V_D = 1$ V. Note that the drain-side end of the gated channel should be the current bottleneck since the carrier density is lowest therein. From figure 10, the reduction of carriers for low channel doping is significantly larger than

**Table 1.** Summary of the average values of the device characteristics of the n-type DG nanostrip J-less transistors under different channel doping concentrations.

| $N_C$ (cm$^{-3}$) characteristics | $5 \times 10^{17}$ | $4 \times 10^{18}$ | $1 \times 10^{19}$ |
|---|---|---|---|
| $V_{TH}$(V)@$V_D = 0.1$V | 0.427 | −0.213 | −0.934 |
| $V_{TH}$(V)@$V_D = 1$V | 0.254 | −0.420 | −1.208 |
| DIBL(V) | 0.17 | 0.21 | 0.27 |
| SS(mV/dec) @$V_D = 1$V | 118.3 | 119.4 | 150.1 |
| $I_{ON}$(A) | $9.92 \times 10^{-7}$ | $1.16 \times 10^{-6}$ | $7.66 \times 10^{-7}$ |
| $I_{OFF}$(A) | $1.82 \times 10^{-12}$ | $2.95 \times 10^{-12}$ | $1.36 \times 10^{-11}$ |

that for high channel doping as the gate bias is reduced by an amount of 0.2 V in the subthreshold region.

Figure 11 shows the statistics of the $I_{ON}$ of the J-less transistors with different channel doping concentrations. As the channel doping concentration increases, the $I_{ON}$ of the J-less transistor tends to decrease. This phenomenon can be explained by figure 6(*b*). For the J-less transistor with higher channel doping concentration, although the electron density is higher as shown in figure 6(*a*), the electron mobility is lower, as shown in figure 6(*c*). The mobility model used in the TCAD simulation takes account of high-field velocity saturation, doping-dependent mobility degradation, and transverse-field-dependent mobility degradation [22]. Since the mobility degrades as the doping increases, the J-less transistor with higher channel doping concentration has lower mobility and thus lower $I_{ON}$ by integrating the current density curves in figure 6(*b*). Figure 12 shows the statistics of the $I_{OFF}$ of the J-less transistors with different channel doping concentrations. The $I_{OFF}$ of the J-less transistor increases as the channel doping concentration increases. Since the SS of the J-less transistor increases as the channel doping concentration increases, consequently the $I_{OFF}$ increases as the channel doping concentration increases. Table 1 is the summary of

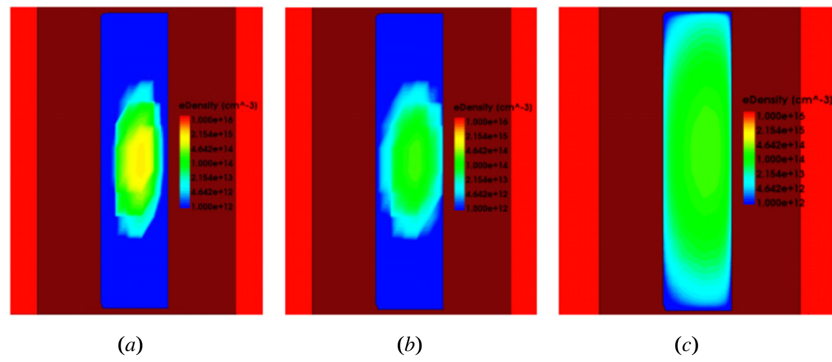


**Figure 9.** The two-dimensional electron density distribution at the drain-side end of the gated channel with the channel doping concentrations of (*a*) $1 \times 10^{19}$, (*b*) $4 \times 10^{18}$, and (*c*) $5 \times 10^{17}$ cm$^{-3}$ under $V_G = V_{TH}$ and $V_D = 1$ V.

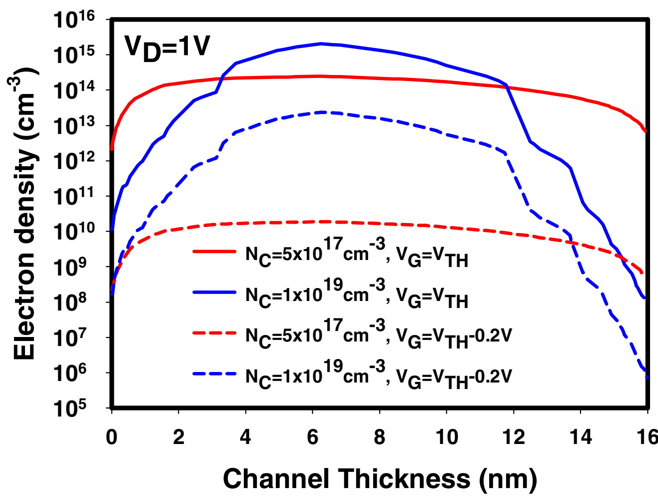


**Figure 10.** The one-dimensional electron density profiles along the horizontal channel thickness direction at the drain-side end of the gated channel under low/high channel doping concentrations ($5 \times 10^{17}$ and $1 \times 10^{19}$ cm$^{-3}$) and $V_G = V_{TH}$ or $V_{TH}$–0.2 V when $V_D = 1$ V.

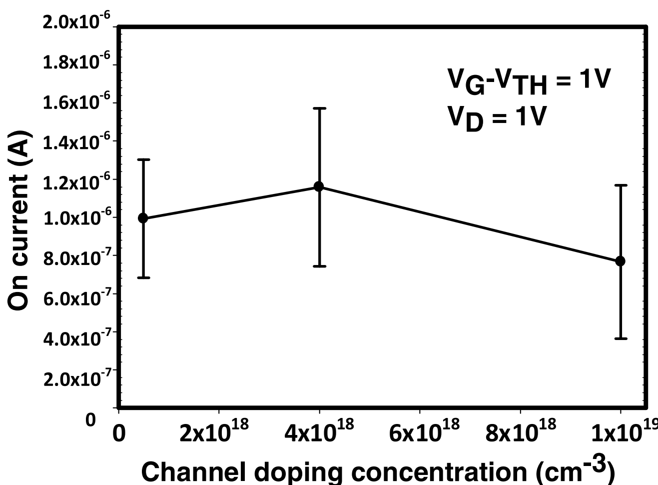


**Figure 11.** The statistics of on-current under different channel doping concentrations for the n-type DG nanostrip J-less transistors. The error bar is determined by the standard deviation of the data.

the average values of the J-less device characteristics under different channel doping concentrations. In brief, as the

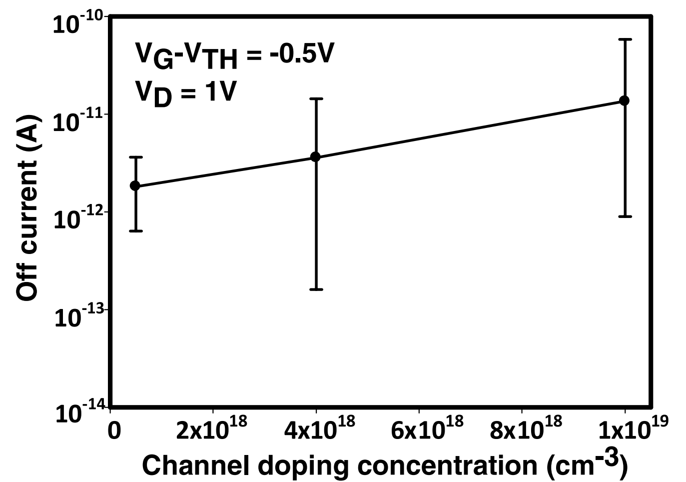


**Figure 12.** The statistics of off-current under different channel doping concentrations for the n-type DG nanostrip J-less transistors. The error bar is determined by the maximum and minimum of the data.

channel doping concentration increases, the performance of the n-type DG nanostrip J-less transistor degrades.

## 4. Conclusion

Novel n-type J-less DG poly-Si nanostrip transistors with different channel doping concentrations were fabricated and characterized. The effects of channel doping concentration on J-less device characteristics were presented and discussed. The experimental results show that as the channel doping concentration of the J-less transistor increases, the $V_{TH}$ becomes more negative and the DIBL and SS increase. Besides, the $I_{ON}$ tends to decrease and the $I_{OFF}$ increase as the channel doping concentration increases. The conduction mechanisms of the J-less transistors under different channel doping were also examined by TCAD simulation. The simulation results show that at lower channel doping concentration, the accumulation layers will form to contribute to the conduction current. Our experimental results indicate that the n-type DG nanostrip J-less transistor with lower channel doping concentration will have better device performance.

## Acknowledgments

The authors would like to thank the National Nano Device Laboratories (NDL) and the Nano Facility Center of the NCTU for assistance in device fabrication. We are also grateful to the National Center for High-performance Computing for computer time and facilities. This work was supported by the Ministry of Education in Taiwan under ATU Program, and the National Science Council under Contracts NSC 99-2221-E-009-167-MY3 and NSC 101-2221-E-259-022.

## References

[1] Hori A, Nakaoka H, Umimoto H, Yamashita K, Takase M, Shimizu N, Mizuno B and Odanaka S 1994 A 0.05 $\mu$m CMOS with ultra shallow source/drain junctions fabricated by 5 keV ion implantation and rapid thermal annealing *Proc. IEEE Int. Electron Devices Meeting* pp 485–8

[2] Asai S and Wada Y 1997 Technology challenges for integration near and below 0.1 $\mu$m *Proc. IEEE* **85** 505–20

[3] Endo K, O'uchi S, Ishikawa Y, Liu Y, Matsukawa T, Sakamoto K, Tsukada J, Yamauchi H and Masahara M 2010 Variability analysis of TiN metal-gate FinFETs *IEEE Electron Device Lett.* **31** 546–8

[4] Lee C-W, Afzalian A, Akhavan N D, Yan R, Ferain I and Colinge J P 2009 Junctionless multigate field-effect transistor *Appl. Phys. Lett.* **94** 053511

[5] Colinge J P *et al* 2010 Nanowire transistors without junctions *Nature Nanotechnol.* **5** 225–9

[6] Lee C-W, Ferain I, Afzalian A, Yan R, Akhavan N D, Razavi P and Colinge J P 2010 Performance estimation of junctionless multigate transistors *Solid State Electron.* **54** 97–103

[7] Rios R, Cappellani A, Armstrong M, Budrevich A, Gomez H, Pai R, Rahhal-orabi N and Kuhn K 2011 Comparison of junctionless and conventional trigate transistors with $L_g$ down to 26 nm *IEEE Electron Device Lett.* **32** 1170–2

[8] Colinge J P, Lee C-W, Ferain I, Akhavan N D, Yan R, Razavi P, Yu R, Nazarov A N and Doria R T 2010 Reduced electric field in junctionless transistors *Appl. Phys. Lett.* **96** 073510

[9] Su C J, Tsai T I, Liou Y L, Lin Z M, Lin H C and Chao T S 2011 Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels *IEEE Electron Device Lett.* **32** 521–3

[10] Lue H T *et al* 2008 A novel junction-free BE-SONOS NAND flash *VLSI Symp. Technical Digest* pp 140–1

[11] Choi S J, Moon D I, Kim S, Ahn J H, Lee J S, Kim J Y and Choi Y K 2011 Nonvolatile memory by all-around-gate junctionless transistor composed of silicon nanowire on bulk substrate *IEEE Electron Device Lett.* **32** 602–4

[12] Sun Y, Yu H Y, Singh N, Leong K C, Quek E, Lo G Q and Kwong D L 2011 Demonstration of memory string with stacked junction-less SONOS realized on vertical silicon nanowire *IEDM Technical Digest* pp 9.7.1–9.7.4

[13] Giusi G and Iannaccone G 2013 Junction engineering of 1T-DRAMs *IEEE Electron Device Lett.* **34** 408–10

[14] Yan R, Ferain I, Kranti A, Akhavan N D, Razavi P, Yu R and Colinge J P 2010 Nanowire zero-capacitor DRAM transistors with and without junctions *IEEE Nanotechnology Conf.* pp 242–5

[15] Lee C-W, Borne A, Ferain I, Afzalian A, Yan R, Akhavan N D, Razavi P and Colinge J P 2010 High temperature performance of silicon junctionless MOSFETs *IEEE Trans. Electron Devices* **57** 620–5

[16] Gnani E, Gnudi A, Reggiani S and Baccarani G 2011 Theory of the junctionless nanowire FET *IEEE Trans. Electron Devices* **58** 2903–2910

[17] Gnani E, Gnudi A, Reggiani S and Baccarani G 2012 Physical model of the junctionless UTB SOI-FET *IEEE Trans. Electron Devices* **59** 941–8

[18] Kranti A, Yan R, Lee C-W, Ferain I, Yu R, Akhavan N D, Razavi P and Colinge J P 2010 Junctionless nanowire transistor (JNT): properties and design guidelines *ESSDERC'10: Proc. Euro. Solid-State Device Research Conf.* pp 357–60

[19] Sallese J-M, Chevillon N, Lallement C, Iniguez B and Pregaldiny F 2011 Charge-based modeling of junctionless double-gate field-effect transistors *IEEE Trans. Electron Devices* **58** 2628–37

[20] Duarte J P, Choi S-J, Moon D-I and Choi Y-K 2011 Simple analytical bulk current model for long-channel double-gate junctionless transistors *IEEE Electron Device Lett.* **32** 704–6

[21] Lin H C, Chen W C, Lin C D and Huang T Y 2009 Performance enhancement in double-gated poly-Si nanowire transistors with reduced nanowire channel thickness *IEEE Electron Device Lett.* **30** 644–6

[22] Synopsys Inc. 2012 *Sentaurus TCAD User Manual Version* G-2012.06 (Mountain View, CA: Synopsys)