Investigation of $LaAlO_3/ZrO_2$/*a*-InGaZnO thin-film transistors using atmospheric pressure plasma jet

Chien-Hung Wu, Hau-Yuan Huang, Shui-Jinn Wang, Kow-Ming Chang and Hsin-Yu Hsu

Amorphous indium–gallium–zinc-oxide thin-film transistors (*a*-IGZO-TFTs) with the $LaAlO_3/ZrO_2$ gate dielectric stack employing a novel atmospheric pressure plasma jet process that results in small subthreshold swing and low threshold voltage are proposed and fabricated. The influence of post-deposition annealing (PDA) temperature on $LaAlO_3/ZrO_2$ gate dielectric stack and device performance was investigated. The equivalent oxide thickness of the $LaAlO_3/ZrO_2$ dielectric stack decreases from 11.5 nm without annealing to 7 nm after a 500°C annealing was applied. The $LaAlO_3/ZrO_2$/*a*-InGaZnO TFT with a 500°C annealing exhibits a small subthreshold swing of 77 mV·dec^{-1}, a high field-effect mobility of 9 cm^2·V^{-1}·s^{-1} and an excellent current ratio of 1.8×10^7, which could be attributed to the improved gate dielectric quality by the PDA. The $LaAlO_3/ZrO_2$/*a*-InGaZnO TFTs with excellent gate control ability allow the device to operate at a low operating voltage with low power consumption.

Introduction: Of the abundant AOS compound materials, amorphous indium–gallium–zinc-oxide thin-film transistors (*a*-InGaZnO TFTs) attract considerable interest for backplanes of the next-generation flat-panel displays as active matrix liquid crystal displays and active matrix organic light-emitting diode displays. Owing to their better field-effect mobility >10 cm^2/V·s and better stability against electrical stress [1, 2]. The non-vacuum techniques such as solution-processed InGaZnO films [3, 4] and atmospheric pressure plasma jet (APPJ) InGaZnO films were proposed recently [5, 6]. The APPJ technique has lower apparatus cost since it does not need a vacuum chamber and associated pumping systems; it also has better suitability for large-scale applications among the other deposition technologies. To further improve the device performance, high-κ materials of ZrO_2 and HfO_2 have been investigated for their superior properties for advanced TFT devices, such as high breakdown field intensity (10∼15 MV/cm), high dielectric constant (20∼25) and the capability of room-temperature processing [7, 8]. In this Letter, the fabrication of bottom-gate IGZO-TFTs with an $LaAlO_3/ZrO_2$ gate dielectric stack (40 nm/10 nm) is reported. The equivalent oxide thickness (EOT) of the $LaAlO_3/ZrO_2$ dielectric stack shrinks from 11.5 nm before post-deposition annealing (PDA) to 7 nm after a 500°C PDA. Excellent gate control ability with a small subthreshold swing (SS) of 77 mV·dec^{-1}, high field-effect mobility (μ_{fet}) of 9 cm^2 V^{-1}·s^{-1}, high current ratio (I_{on}/I_{min}) of 1.8×10^7 and low operation voltage of 3.0 V are attributed to the improved gate dielectric quality by the PDA.

Experiments: Fig. 1 shows the schematic of the fabricated $LaAlO_3$ (40 nm)/ZrO_2 (10 nm)/IGZO (50 nm) TFT. The staggered bottom-gate *a*-IGZO-TFTs were fabricated on heavily doped n-type silicon substrates. High-κ gate dielectrics of $LaAlO_3$ and ZrO_2 were deposited by an e-beam evaporation with thicknesses of 40 and 10 nm, respectively, on the silicon substrate which served as the gate electrode. PDA was then carried out at various temperatures (T) between 300 and 500°C in N_2 for 10 min. Subsequently, a 50 nm-thick *a*-IGZO layer was deposited by APPJ. The substrate temperature was kept at 200°C during deposition of InGaZnO. Trimethylaluminium ($Al_2(CH_3)_6$, TMA) and oxygen plasma reactants were used as precursors and oxidants, respectively. Indium nitrate ($In(NO_3)_2$), gallium nitrate ($Ga(NO_3)_2$) and zinc nitrate ($Zn(NO_3)_2$) were used as the precursor materials. The concentration of the InGaZnO solution was kept at 0.2 M and was ultrasonically atomised at 2.45 MHz into mist and then conveyed by the carrier gas (N_2) to the plasma region connected to a pulsed DC power supply at a repetition rate of 25 kHz and voltage pulse of 15 kV with a pulse width of 8 µs to generate the downstream plasma. The InGaZnO film was deposited and patterned through photolithography and wet etching. Finally, 300 nm-thick Al source/drain contacts were thermally deposited and formed by the lift-off. The channel width (W) and length (L) were 200 and 20 µm, respectively. Al/$LaAlO_3/ZrO_2$/*p*-Si (MIS structure) capacitors were fabricated simultaneously for C–V performance characterisation. The devices were characterised under an open air condition at room temperature using a semiconductor parameter analyser (2636A, Keithley, USA).

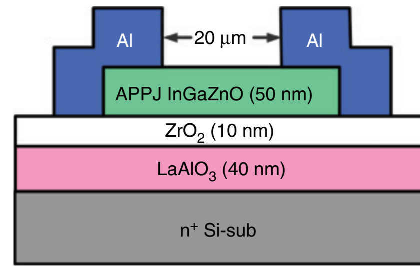

Fig. 1 *Schematic diagram of bottom-gate $ZrO_2/LaAlO_3$/IGZO-TFT*

Results and discussion: The optical transmittance spectra of the *a*-IGZO films deposited on a glass substrate are shown in Fig. 2. The average transmittance of *a*-IGZO films on a glass substrate are more than 80% in the visible range. The transmittance spectrum of the glass substrate is also indicated. In a direct-transition semiconductor, the absorption coefficient, α, and optical band gap (E_g) are related by Tang *et al.* [9] as follows: $\alpha^2 = B(h\nu - E_g)$ and $\alpha = 2.303[\log(1/T)]/d$, where B is a constant, $h\nu$ is the energy of the incident photon and T and d are the transmittance and thickness of the thin films. The band gap of *a*-IGZO films is about 3.35 eV.

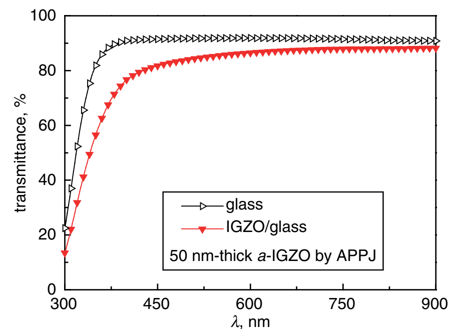

Fig. 2 *Optical transmission spectra of 50 nm-thick a-IGZO film on glass substrates by APPJ*

The C–V characteristics of the Al/$LaAlO_3/ZrO_2$/*p*-Si (MIS structure) are shown in Fig. 3. The capacitance of the Al/$LaAlO_3/ZrO_2$/*p*-Si capacitor increases with an increasing PDA temperature. The calculated EOTs of the $LaAlO_3/ZrO_2$ dielectric stacks are 11.5, 10, 9 and 7 nm for the case without PDA and at annealing temperatures of 300, 400 and 500°C, respectively. The decrease in the flat-band voltage and increase in the slope with increasing T indicates that both the interface and the bulk traps of the dielectric stack are recovered by the high annealing temperature. With a sharper slope and a considerable shift towards positive V_G-axis for the V_{fb}, an improved $LaAlO_3/ZrO_2$ gate dielectric quality could be obtained. The transfer curves of the IGZO-TFTs without and with the annealing temperatures of 300, 400 and 500°C are shown in Fig. 4. It is noted that the current maximum (I_{max}) increases with increasing T, while the current minimum (I_{min}) reduces to about 10^{-13} A. The current ratio (I_{max}/I_{min}) and the threshold voltage (V_t) are 4.7×10^5 and 1.0 V, 1.2×10^6 and 0.8 V, 5.2×10^6 and 0.5 V, and 1.8×10^7 and 0.1 V for the case without PDA and $T = 300$, 400 and 500°C. The μ_{fet} and SS were extracted through the dependences of Lg_m/C_iWV_{DS} and $\delta V_{GS}/\delta(\log I_{DS})$, which are 8.3 cm^2/V·s and 219 mV/dec, 7.8 cm^2/V·s and 335 mV/dec, 8 cm^2/V·s and 109 mV/dec, and 9 cm^2/V·s and 77 mV/dec for the case without PDA and $T = 300$, 400 and 500°C. The improved SS at high T could be attributed to the increased gate oxide capacitance (C_{ox}) and therefore the higher κ value of the $LaAlO_3/ZrO_2$ dielectric stack by the PDA; however, the deviation of SS and μ_{fet} at 300 and 400°C could be induced by the increment of interface traps since the annealing was applied before channel deposition, and a constant channel capacitance can be assumed [10]. The best device performances of I_{max}/I_{min}, SS, V_t and μ_{fet} are 1.8×10^7, 77 mV/dec, 0.1 V and 9 cm^2/V·s, respectively, which were obtained for the case with $T = 500$°C. The comparisons of the $ZrO_2/LaAlO_3$/IGZO-TFT with variant gate dielectric stacks are shown in Table 1.

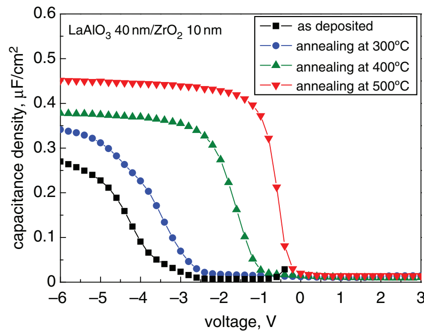

Fig. 3 *C–V characteristics of Al/LaAlO$_3$/ZrO$_2$/p-Si (MIS structure) gate capacitor annealed at different PDA temperatures*

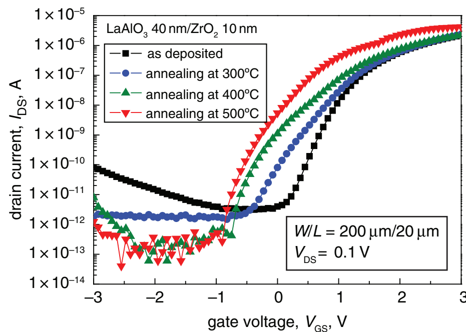

Fig. 4 *I_{DS}–V_{GS} transfer characteristics of IGZO-TFT with LaAlO$_3$ (40 nm)/ ZrO$_2$ (10 nm) dielectric stack at different PDA temperatures*

Table 1: Comparisons of LaAlO$_3$/ZrO$_2$/*a*-IGZO-TFT with variant gate dielectric stacks

Dielectric materials	Mobility (cm^2/V·s)	V_t (V)	SS (mV/dec)	I_{max}/I_{min}
PVD LaAlO$_3$/ZrO$_2$, this work	9	0.1	77	1.8×10^7
PE-ALD Al$_2$O$_3$ [5]	8.4	0.7	280	1.0×10^8
AP-CVD AlO$_x$ [6]	4.2	3.6	550	$\sim 10^8$
RF sputter ZrO$_2$ [7]	28	3.2	560	4.8×10^7
RF sputter HfON/HfO$_2$/HfON [8]	10.2	−0.92	130	2.2×10^6

Conclusion: LaAlO$_3$/ZrO$_2$/*a*-IGZO-TFTs with a silicon gate have been fabricated successfully using the APPJ process. The devices feature a small SS of 77 mV·dec^{-1}, a high μ_{FET} of 9 cm^2·V^{-1}·s^{-1} and a good I_{max}/I_{min} of 1.8×10^7 with 500°C annealing of the LaAlO$_3$/ZrO$_2$ dielectric stack. The integration of high-κ LaAlO$_3$/ZrO$_2$ dielectrics into IGZO-TFTs attains the aim of enhancing the gate control ability. It is expected that LaAlO$_3$/ZrO$_2$/*a*-IGZO-TFTs might have great potential for applications in low power-consuming and high-end displays.

Acknowledgments: This work was supported by the National Science Council of Taiwan, Republic of China, under grants NSC 100-2221-E-006-156-MY2, NSC 100-2221-E-006-045-MY2 and NSC 102-2221-E-006-217-MY2. The authors thank the Center for Micro/Nano Science and Technology, National Cheng Kung University, Taiwan, for equipment access and technical support.

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7 March 2014
doi: 10.1049/el.2014.0816
One or more of the Figures in this Letter are available in colour online.

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