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Natural substrate lift-off technique for vertical light-emitting diodes

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Hexagonal inverted pyramid (HIP) structures and the natural substrate lift-off (NSLO) technique were demonstrated on a GaN-based vertical light-emitting diode (VLED). The HIP structures were formed at the interface between GaN and the sapphire substrate by molten KOH wet etching. The threading dislocation density (TDD) estimated by transmission electron microscopy (TEM) was reduced to $1 \times 10^8\,\text{cm}^{-2}$. Raman spectroscopy indicated that the compressive strain from the bottom GaN/sapphire was effectively released through the HIP structure. With the adoption of the HIP structure and NSLO, the light output power and yield performance of leakage current could be further improved.
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Directly transitional wide-band-gap materials have the potential to cover from UV to the whole visible spectrum; in particular, gallium nitride (GaN)-based materials have attracted considerable attention all over the world owing to their important blue-green band gap and widespread applications in optoelectronic devices, such as light-emitting diodes (LEDs) and laser diodes (LDs).[1,2] However, most devices are grown on foreign substrates such as sapphire and SiC, owing to the lack of large and cheap GaN substrates. In the past, sapphire was the most widely used substrate material because of its relatively low cost and mature production technique. However, the performance of devices grown on a sapphire substrate is limited by dislocation defects from lattice mismatch and by the poor electrical and thermal conductivities of sapphire. Consequently, the techniques of laser lift-off (LLO)[3] and chemical lift-off (CLO)[4] have been adopted for fabricating the freestanding GaN membrane and the VLED structure to solve the imperfections caused by the sapphire substrate. Unfortunately, LLO may induce additional damage and high-level strain in the local area by the high-power thermal irradiation during the process. Other disadvantages of LLO are its low throughput, high cost, and complex fabrication. On the other hand, CLO can protect the GaN layer from damage during the lift-off process by using a CrN layer,[5] a ZnO layer,[6] or a Si-doping n-GaN layer[7] as the sacrificial layer. It is still difficult to maintain the etching uniformity and crystal quality simultaneously. In CLO, the sacrificial layer needs to be inserted prior to the real device epitaxial layer process, which may involve a complicated process, and the removal of a sapphire substrate in the etching solution always takes more than 24 h.[14] In this work, we demonstrate a natural substrate lift-off (NSLO) technique for fabricating high-quality GaN-based VLEDs with hexagonal inversed pyramid (HIP) structures. The HIP structure was formed using a high-temperature potassium hydroxide solution directly (KOH, 280 °C) without lithography. Furthermore, GaN-based LED structures were regrown on the HIP structure by the epitaxial lateral overgrowth (ELOG) method. Then, through the mechanical lift-off process, the sapphire substrate can be removed. The naturally formed rough surface on the GaN epilayer can improve the light extraction of the GaN-based VLEDs. The fabrication of the GaN-based VLEDs with HIP structures and optical analysis are described as follows.

An undoped GaN (u-GaN) layer was grown on a 2 in. *c*-plane sapphire substrate as a template by metal organic chemical vapor deposition (MOCVD). A 30-nm-thick GaN nucleation layer was first grown on a sapphire substrate at 490 °C after thermal cleaning with hydrogen gas purging at 1100 °C for 5 min, then annealing for 10 min, and then growing a 3-µm-thick u-GaN layer at 1030 °C, as shown in Fig. 1(a). After this first growth, the u-GaN template was dipped in molten KOH at 280 °C for 10 min to form the HIP structure, as shown in Fig. 1(b), and this etching time is chosen to obtain the right amount of GaN to be removed to facilitate the later NSLO. The molten KOH can permeate along the threading dislocation into the interface between u-GaN and the sapphire substrate, and initiate a wet-etch process. When the etching time is too short, the residual contacting area between u-GaN and sapphire is too large to lift-off the film, and when the etching time is too long, the u-GaN layer is attacked severely by KOH and the subsequent LED regrowth is not uniform. Note that the etching rate of u-GaN is related to the crystal orientation.[8,9] The bottom-up crystallographic etching is faster than the top-down etching. The V-shaped texture was formed on the interface between u-GaN and the sapphire substrate. The equivalent contact area between u-GaN and the sapphire substrate is reduced to about 23.1% of the original area owing to this V-groove formation, and the sample is called GaN-HIP hereafter. Figure 1(c) shows that the GaN-based LED structures were grown on the GaN-HIP template using the MOCVD system. The LED device structures consisted of 2-µm-thick u-GaN (for which the ELOG method was applied to obtain a fully coalesced GaN layer), a 3.5-µm-thick Si-doped n-type ($n = 3 \times 10^{18}$ cm^{-3}) GaN layer, 10 pairs of $Al_{0.02}Ga_{0.98}N/In_{0.1}Ga_{0.9}N$ multiple quantum wells (MQWs) with a 2.5-nm-thick well and a 13-nm-thick barrier as active layers, and a 100-nm-thick p-type ($p = 3 \times 10^{19}\,\text{cm}^{-3}$) GaN cap layer, the concentration of which was measured by secondary ion mass spectrometry (SIMS). The indium content and layer thicknesses in AlGaN/InGaN quantum wells were estimated by high-resolution X-ray diffraction (HRXRD).

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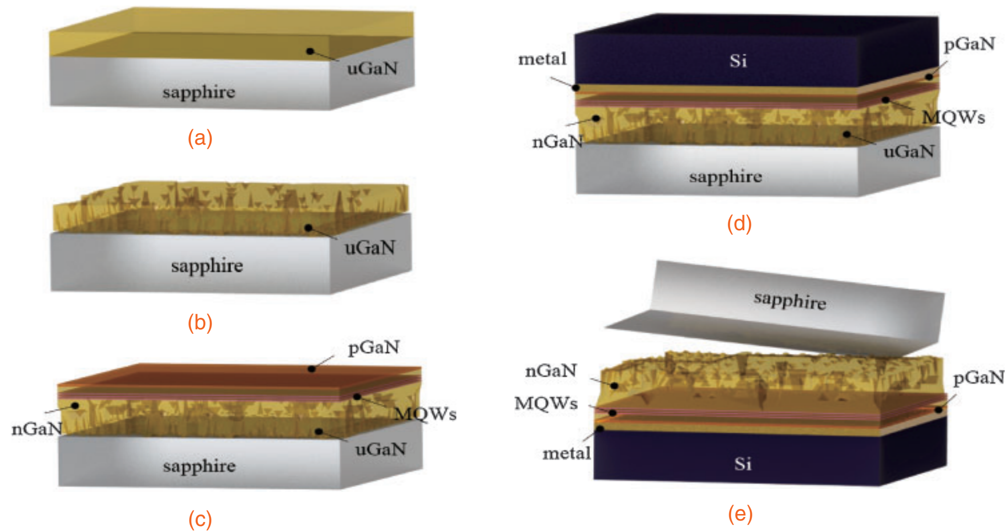

Fig. 1. Schematic diagram of fabrication of GaN-based VLED with HIP structure: (a) u-GaN on sapphire; (b) HIP structure; (c) GaN-based LED structure on HIP template; (d) wafer bonding; (e) removal of sapphire substrate by NSLO.

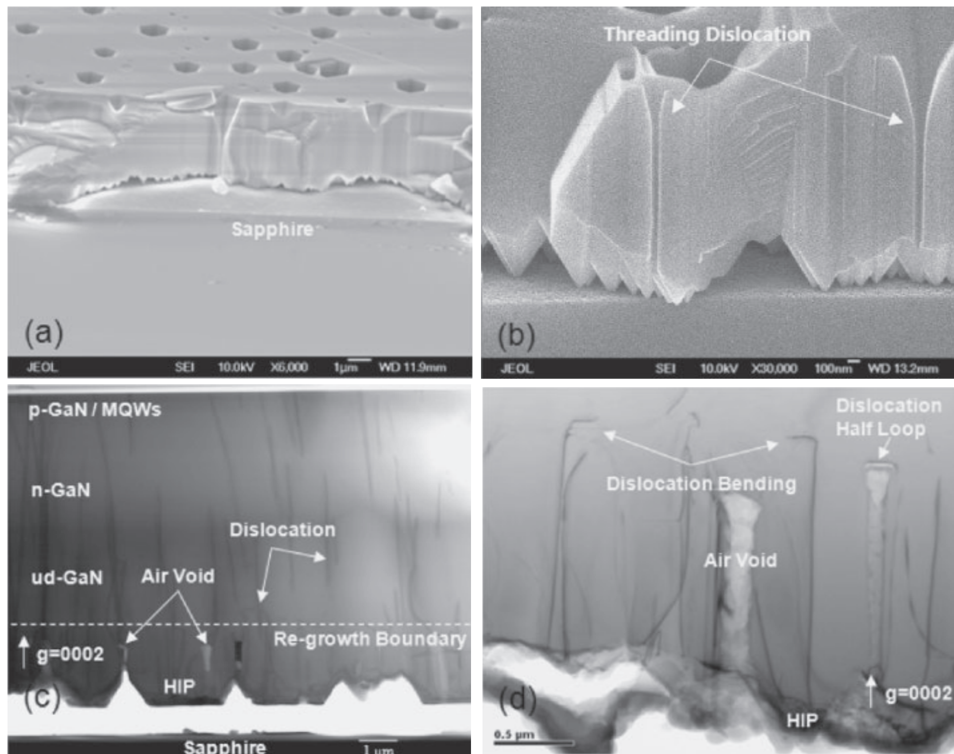

Fig. 2. Cross-sectional SEM images of (a) KOH wet-etched u-GaN and (b) GaN-HIP structure. Cross-sectional TEM images of (c) GaN-based LED structure regrown on GaN-HIP template and (d) regrown HIP GaN/air structure. The diffraction condition was $g = 0002$.

After high-temperature wet etching with KOH, V-shaped hexagonal pits of about $2 \times 10^7\,\text{cm}^{-2}$ were formed on the surface of u-GaN. A scanning electron microscopy (SEM) image of the cleaved sample is shown in Fig. 2(a), where the HIP structure at the GaN/sapphire interface is clearly observed in Fig. 2(b). The GaN-based LED was regrown on the GaN-HIP template that provided a flat top surface for the LED device growth. It was found that the HIP structures still existed after the regrowth, and some air voids were also found in the HIP structures. Figure 2(c) shows a cross-sectional transmission electron microscopy (TEM) image of the GaN LED/HIP template sample. The regrowth boundary of the GaN epilayer is indicated by a white dashed line. Air void formation was usually observed in the etching boundary during the lateral regrowth process. The dislocation density at the bottom of the GaN layer was found to be about 2×10^9 cm^{-2} and slightly reduced to $1 \times 10^8\,\text{cm}^{-2}$ at the top of the GaN layer. The dislocation density is reduced owing to the bending and half-looping of threading dislocations at the regrowth boundary. Most dislocations connect with each other by bending and loop formation, which do not extend to the top surface, as observed in Fig. 2(d). This result indicated that the vertical propagation of dislocations was effectively hindered by the lateral overgrowth.

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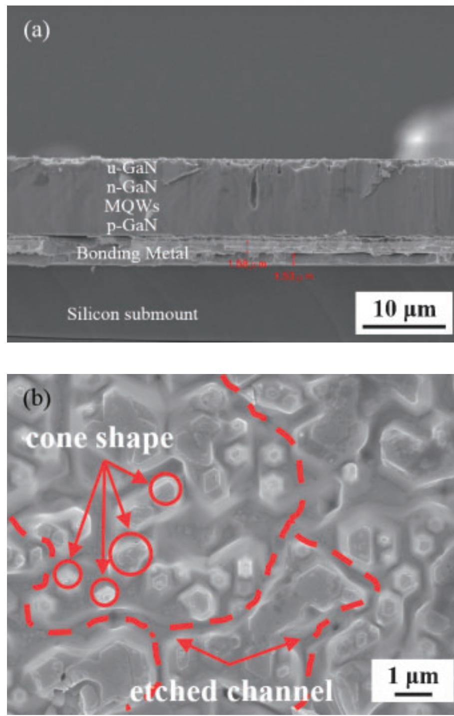

Fig. 3. (a) Cross-sectional SEM image of VLED structure fabricated using NSLO and (b) top-view SEM image of GaN-HIP morphology.

The HIP structure could serve as a separation layer in NSLO by utilizing the coefficient of thermal expansion (CTE) mismatch of materials, which can cause an unbearable shear stress to the interface between GaN-HIP and the sapphire substrate, then cause the HIP structure to break off. Therefore, the mechanical lift-off process can be achieved with the HIP structures as a sacrificial layer at a high temperature of 300 °C. A cross-sectional SEM image of the GaN-based VLED bonded to a Si wafer by bonding metals using NSLO is shown in Fig. 3(a). In Fig. 3(b), the top-view image of the untreated u-GaN-HIP (N-face, $-c$ polarity plane) surface is shown, and the cone-shaped HIP structure and etched channel could be clearly observed. The size and density of the cone shape were about 0.5–1 μm and 8×10^7 cm^{-2}, respectively. It was found that the etched channel was formed throughout the GaN/sapphire interface and resulted in the GaN epilayer partially attached to the sapphire substrate.

The Ni/Ag/Pt (30/1200/30 Å) metal layer was subsequently deposited as the reflective p-contact layer by E-beam evaporation. The sample was annealed in an atmosphere full of oxygen for 10 min at 250 °C for ohmic contact. A 100-nm-thick TiW diffusion barrier layer and a Ti/Au (150 nm/3 μm) bonding layer were deposited on the p-contact layer, and this LED wafer with the HIP structure was then flipped and bonded onto a heavily doped Si wafer, as shown in Fig. 1(d). The bonding time, pressure, and temperature were 30 min, 5 MPa, and 420 °C, respectively. The CTEs of the sapphire and GaN are 7.5×10^{-6} and 5.45×10^{-6} °C, respectively, which will induce thermal stress in the bonding and cooling processes. Owing to the reduction in the equivalent contact area, the thermal stress of the interface between the GaN-HIP structure and the sapphire substrate is enhanced by about 4-fold. Thus, the large shear stress is greater than the fracture strength of the GaN-HIP structure, and the LED with the GaN-HIP structure bonded onto the Si wafer would automatically separate from the sapphire substrate during the cooling process. Therefore, the sapphire substrate is removed and a rugged LED surface can be achieved simultaneously by this lift-off technique, as shown in Fig. 1(e). After removing the sapphire substrate, the u-GaN was etched to expose the n-GaN layer using an inductively coupled plasma (ICP) etcher; the LED mesa with a pattern of 1×1 mm^2 was defined and fabricated by photolithography and dry etching. Finally, a Ti/Pt/Au metal layer was deposited as the n-GaN ohmic contact. A high-quality VLED was obtained by NSLO. A VLED sample was also prepared by the traditional LLO method using the same process for comparison.[10]

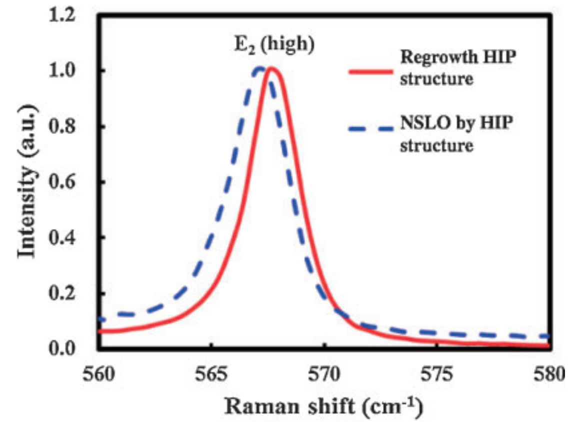

Fig. 4. Raman spectrum of GaN epilayer regrown on HIP structure and after NSLO at room temperature.

The geometric morphology of the LED structures was observed by SEM. The distribution and behaviors of threading dislocations in the epitaxial layer were analyzed by TEM. Raman spectroscopy was employed to estimate the compressive strain from the bottom GaN/sapphire. The light output power–current–voltage (L–I–V) characteristics of the VLEDs were measured using a conventional probe station and an integrating sphere instrument.

Figure 4 shows the room-temperature Raman spectrum of the GaN epilayer regrown on the HIP structure and after NSLO. The Raman shift peak of E2 (high) for the GaN epilayer regrown on the HIP structure and after NSLO was located at approximately 567.8 and 567.1 cm^{-1}, respectively. The strain of the GaN epilayer can be obtained using[11]

$$\Delta\omega = \omega_{E2} - \omega_0 = C \cdot \sigma_{xx} \tag{1}$$

$$\sigma_{xx} = M_f \cdot \varepsilon_{xx} \quad \varepsilon_{xx} = \frac{\Delta\omega}{C \cdot M_f}$$

where $\Delta\omega$ is the Raman peak difference between the strained GaN epilayer ω_{E2} and the unstrained GaN epilayer ω_0 (566.5 cm^{-1}), C is the biaxial strain coefficient, which is 2.25 cm^{-1}/GPa, M_f is the biaxial modulus of the substrate, which is 449.6 GPa, σ_{xx} is the biaxial stress, and ε_{xx} is the biaxial strain. The Raman peak of E2 (high) for GaN on sapphire without the HIP structure was 569.5 cm^{-1}, and the in-plane compressive strain ε_{xx} was about 2.97×10^{-3}. However, the in-plane compressive strain ε_{xx} was calculated as 1.30×10^{-3} and 6.03×10^{-4} for the GaN epilayer regrown on the HIP structure and after the mechanical lift-off, respectively. In other words, the residual stress of the GaN-based LED could be considerably reduced with the

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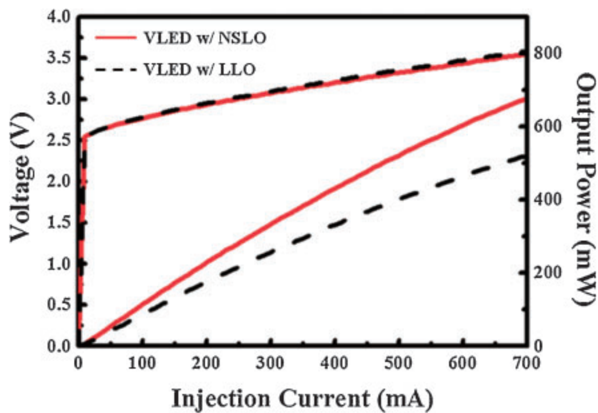

Fig. 5. Comparison of *L–I–V* properties of VLED fabricated with NSLO and that with LLO.

Table I. Electrical and optical characteristics of VLED fabricated with NSLO and that with LLO.

Process	Voltage (V)	Power (mW)	Yield (%) of $I_r < 0.2\,\mu A$ (at -5 V)
NSLO	3.21	390	91.3
LLO	3.23	300	78.3

introduction of the HIP structure to the GaN/sapphire interface.

To compare the performance of VLED fabricated with NSLO with that of VLED fabricated with traditional LLO, these VLEDs with the same LED structure and chip size were manufactured. Figure 5 shows the *L–I–V* characteristics of the VLEDs fabricated with NSLO and LLO under CW operation conditions. The turn-on voltage of VLEDs was about 2.55 V for both fabrication approaches. The *I–V* curves of these devices were almost identical, which indicated that the HIP structure and NSLO would not cause any degradation of the electrical properties of the VLED. At the driving current of 350 mA, the forward voltages of VLED fabricated with NSLO and that with LLO were 3.23 and 3.21 V, respectively. According to the corresponding *L–I* characteristics, the light output power of VLED fabricated with NSLO was 30% higher than that of VLED fabricated with LLO at 350 mA. Such an output power enhancement could be ascribed to the inherent surface roughness of the HIP structure. Besides, the comparison of the low leakage current yield ($I_r < 0.2\,\mu A$ at -5 V) between NSLO and LLO as shown in Table I also demonstrates the superiority of NSLO over LLO. The better yield performance of I_r could result from the smaller and more moderate stress release after NSLO. Conversely, the instant stress release after LLO could induce additional epilayer damage and result in the worse yield performance of I_r. The strain reduction of GaN growth on the sapphire or Si substrate owing to the air gap structure has been discussed in previous works.[12,13] The HIP structure partially relieves GaN from the sapphire substrate, which releases the compressive strain. This partially relieved layer served as a template in the subsequent regrowth process. It acted as a transitional layer that decreases the mismatched lattice constant and thermal expansion coefficient, then improve the crystal quality. Therefore, this HIP structure could efficiently reduce the stress on the regrown GaN epilayer, on which the high-efficiency VLED can be demonstrated.

In summary, we have successfully demonstrated the fabrication of the HIP structure and a high-quality vertical GaN-based LED with HIP structures by NSLO. The density of threading dislocations can be efficiently reduced by applying the regrown GaN epilayer on the HIP structure. The in-plane compressive strain ε_{xx} was calculated to be about 1.30×10^{-3} and 6.03×10^{-4} for the GaN epilayer regrowth on the HIP structure and after NSLO, respectively. It implies that the residual stress of the GaN-based LED can also be greatly reduced while introducing the HIP structure to the GaN/sapphire interface. The optical output power of VLED fabricated with NSLO is enhanced significantly (by 30%) at 350 mA operating current, and the yield of the leakage current is also improved. From the results obtained, this NSLO technique can be a good candidate for improving the performance of VLEDs, and it can be applied to large wafers such as 4 or 6 in. Si.

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