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Low interface trap density $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitor fabricated on MOCVD-grown InGaAs epitaxial layer on Si substrate

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A low interface trap density (D_{it}) $Al_2O_3/In_{0.53}Ga_{0.47}As$/Si MOS capacitor fabricated on an $In_{0.53}Ga_{0.47}As$ heterostructure layer directly grown on a 300 mm on-axis Si(100) substrate by MOCVD with a very thin buffer layer is demonstrated. Compared with the MOS capacitors fabricated on the $In_{0.53}Ga_{0.47}As$ layer grown on the lattice-matched InP substrate, the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitors fabricated on the Si substrate exhibit excellent capacitance–voltage characteristics with a small frequency dispersion of approximately 2.5%/decade and a low interface trap density D_{it} close to $5.5 \times 10^{11}\,cm^{-2}\,eV^{-1}$. The results indicate the potential of integrating high-mobility InGaAs-based materials on a 300 mm Si wafer for post-CMOS device application in the future.

$In_xGa_{1-x}As$-based devices have been considered as promising candidates to replace traditional Si devices for high-performance low-power logic application owing to the high mobility of the material.[1–5] The outstanding performance of $In_xGa_{1-x}As$-based MOS devices on an InP substrate grown by molecular beam epitaxy (MBE) has been reported.[6–8] However, the InP substrate is expensive, fragile, and available only in small sizes, and has less mature process technology than the Si substrate.[9] Therefore, the integration of the $In_xGa_{1-x}As$ material on the Si substrate is desirable for future high-performance low-power logic devices.[10–13] Overcoming the large lattice and thermal coefficient mismatches between the $In_xGa_{1-x}As$ material and the Si substrate is the key issue for the growth of a high-quality $In_xGa_{1-x}As$ epitaxial layer on the Si substrate. The growth of high-quality $In_xGa_{1-x}As$ on the Si substrate using $In_xGa_{1-x}As$ and Si_xGe_{1-x} buffer layers has been reported.[14–16] In this work, $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs fabricated on an $In_{0.53}Ga_{0.47}As$ layer grown by metal organic chemical vapor deposition (MOCVD) on 300 mm on-axis Si substrates using an InP/GaAs metamorphic buffer layer are reported. The excellent electrical characteristics of the $Al_2O_3/In_{0.53}Ga_{0.47}As$/Si MOS capacitors demonstrate the potential of integrating InGaAs-based high-mobility transistors on a 300 nm Si substrate for post-CMOS application.

The $In_{0.53}Ga_{0.47}As$-based heterostructure was grown by MOCVD on a 300 mm (12 in.) on-axis Si(100) substrate. First, the GaAs buffer layer was grown on Si. Then, an InP layer, which is lattice-matched to $In_{0.53}Ga_{0.47}As$, was grown on the GaAs buffer. Finally, a Si-doped $In_{0.53}Ga_{0.47}As$ layer was grown on top of the InP layer. The cross-sectional transmission electron microscopy (TEM) image in Fig. 1(a) shows the cross section of the grown epitaxial structure; the total GaAs/InP metamorphic buffer layer was about 840 nm thick, which is the thinnest buffer for the growth of $In_{0.53}Ga_{0.47}As$ on a Si substrate reported to date. The misfits and threading dislocations were predominantly trapped within the GaAs buffer layer, and much less threading dislocations were found inside the InP layer. The dislocation density in the $In_{0.53}Ga_{0.47}As$ channel layer was $(2–3) \times 10^9\,cm^{-2}$, as estimated from X-ray diffraction (XRD) (004) ω-FWHM using the Ayers model.[17] The high-resolution TEM image in

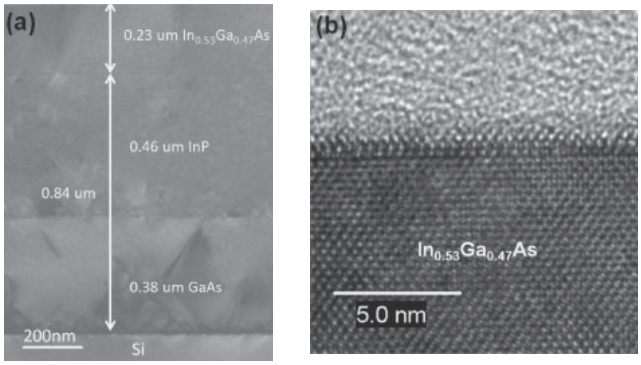

Fig. 1. (a) Cross-sectional TEM image of $In_{0.53}Ga_{0.47}As$ heterostructure on Si. The metamorphic GaAs/InP buffer in this work has a total thickness of 0.84 μm. (b) High-resolution TEM image of top InGaAs channel.

Fig. 1(b) also reveals the good crystal quality of the top $In_{0.53}Ga_{0.47}As$ layer. The surface morphology of the $In_{0.53}Ga_{0.47}As$ heterostructure was measured by atomic force microscopy (AFM), and the rms was 1.94 nm across a 5×5 μm^2 area, which is in the same range as previously reported for the InGaAs/InP/GaAs heterostructure grown on Si.[18] Figure 2 shows Hall mobility as a function of carrier concentration for the Si-doped $In_{0.53}Ga_{0.47}As$ heterostructure grown on Si. The $In_{0.53}Ga_{0.47}As$ layer on 300 mm Si exhibits high mobility ($>5000\,cm^2\,V^{-1}\,s^{-1}$) at 300 K, which is comparable to that of the $In_{0.53}Ga_{0.47}As$ layer grown on an InP substrate by MBE or MOCVD.[19,20]

Al_2O_3 was deposited epitaxially by atomic layer deposition (ALD) on the $In_{0.53}Ga_{0.47}As$ on a Si substrate for MOSCAP fabrication. The MOSCAP device process includes surface treatment, oxide deposition, gate metal deposition, and Ohmic contact formation. First, the wafers were cleaned in 1% HF solution for 3 min, then loaded into the ALD system for the oxide deposition, and the Al_2O_3 (8 nm) layer was deposited at 300 °C. After that, the films were annealed at different temperatures in nitrogen gas for 10 min to optimize the postdeposition annealing (PDA) temperature. Then, Ni/Au was deposited using an electron beam evaporator as the gate contact metal. Finally, the oxide in the Ohmic area was removed using 1% HF. Then, Au/Ge/Ni/Au was

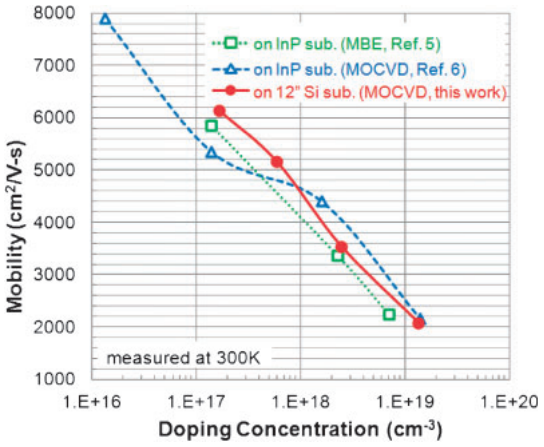

Fig. 2. Hall mobility of $In_{0.53}Ga_{0.47}As$ as a function of doping concentration. The $In_{0.53}Ga_{0.47}As$ layers were grown on InP by MBE and MOCVD.

deposited using the electron beam evaporator on an $In_{0.53}Ga_{0.47}As$ layer and annealed at 250 °C for 30 s for Ohmic contact formation.

X-ray photoelectron spectroscopy (XPS) was used to determine the Al_2O_3/InGaAs interface chemistry. The As 3d, Ga $2p_{3/2}$, and In $3d_{5/2}$ XPS spectra of the samples with different PDA temperatures and doping concentrations were investigated. No clear increase in the number of As–O and In–O bonds was observed when the PDA temperature was increased from 400 to 500 °C for n-$In_{0.53}Ga_{0.47}As$ grown on a wafer with a Si doping concentration of $1.7 \times 10^{17}\,cm^{-3}$, as shown in Fig. 3. However, the number of Ga–As bonds was reduced when the annealing temperature was increased. Ga–As bonds changed into Ga_2O_3 and GaO bonds when the annealing temperature was increased from 400 to 500 °C, as shown in Fig. 3. The same results were obtained for the n-$In_{0.53}Ga_{0.47}As$ epitaxial layers grown on Si substrate wafers with 8.0×10^{16} and $6.2 \times 10^{17}\,cm^{-3}$ Si doping concentrations. This indicates that atomic interdiffusion between the oxide layer and the underlying semiconductor occurred during the 500 °C annealing.

Figure 4 shows the C/C_{max}–V curves at 1 kHz and 1 MHz for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs on the Si substrate with various Si doping concentrations for the $In_{0.53}Ga_{0.47}As$ layer (8.0×10^{16}, 1.7×10^{17}, and $6.2 \times 10^{17}\,cm^{-3}$), and the PDA temperatures were 400 and 500 °C. C_{min} depends on the maximum width of the depletion region W_{Dm} under steady-state condition. C_{min} can be obtained as

$$C_{min} = \frac{\varepsilon_s \varepsilon_i}{\varepsilon_s d + \varepsilon_i W_{Dm}}, \quad (1)$$

where ε_i and ε_s are the permittivities of the insulator and semiconductor, respectively, and W_{Dm} can be calculated as

$$W_{Dm} \approx \sqrt{\frac{4\varepsilon_s kT \ln(N_D/n_i)}{q^2 N_D}}. \quad (2)$$

Here, N_D is the donor concentration. According to these equations, C_{min} increases if W_{Dm} decreases, which occurs when the doping concentration is increased, and C_{min} also increases when the doping concentration increases for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs on the Si substrate, as shown in Fig. 4. Furthermore, Eq. (3) shows the interface trap density (D_{it}), which was obtained by the high-low-frequency capacitance method.

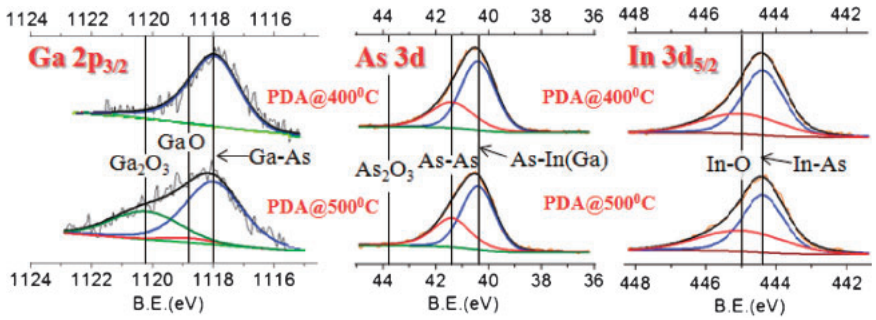

Fig. 3. XPS spectra of Ga $2p_{3/2}$, As 3d, and In $3d_{5/2}$ after $Al_2O_3/In_{0.53}Ga_{0.47}As$ was annealed at 400 and 500 °C; the Si doping concentration of the n-$In_{0.53}Ga_{0.47}As$ layer is $1.7 \times 10^{17}\,cm^{-3}$.

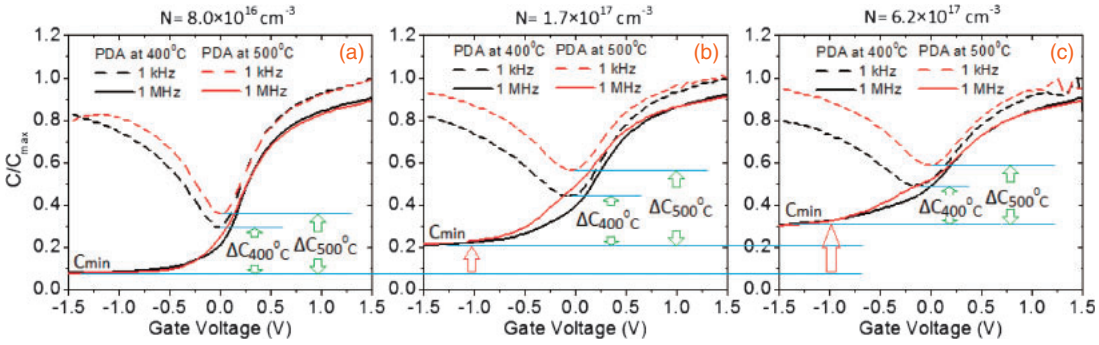

Fig. 4. C/C_{max}–V curves at 1 kHz and 1 MHz for (a) 8.0×10^{16}, (b) 1.7×10^{17}, and (c) $6.2 \times 10^{17}\,cm^{-3}$ Si-doped n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA temperatures of 400 and 500 °C.

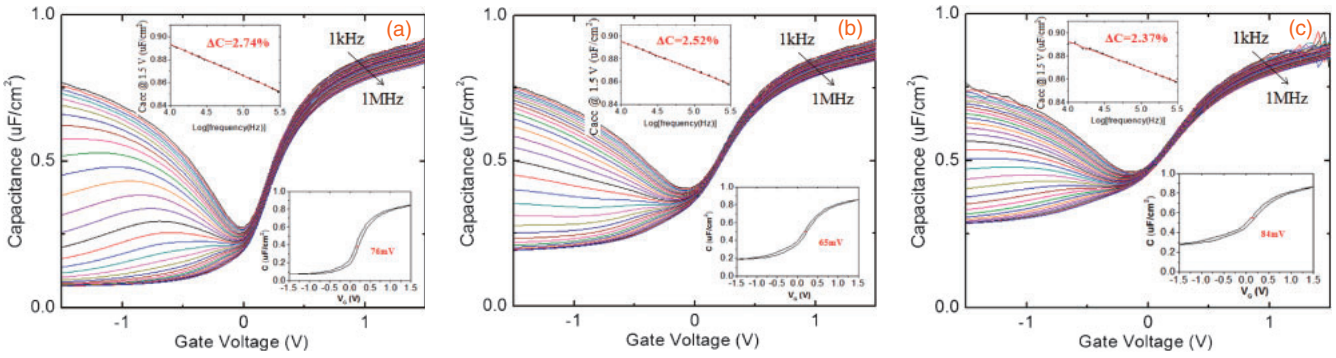

Fig. 5. *C–V* curves for (a) 8.0×10^{16}, (b) 1.7×10^{17}, and (c) $6.2 \times 10^{17}\,\mathrm{cm^{-3}}$ Si-doped n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA temperature of 400 °C (diode area A: $1.96 \times 10^{-5}\,\mathrm{cm^2}$).

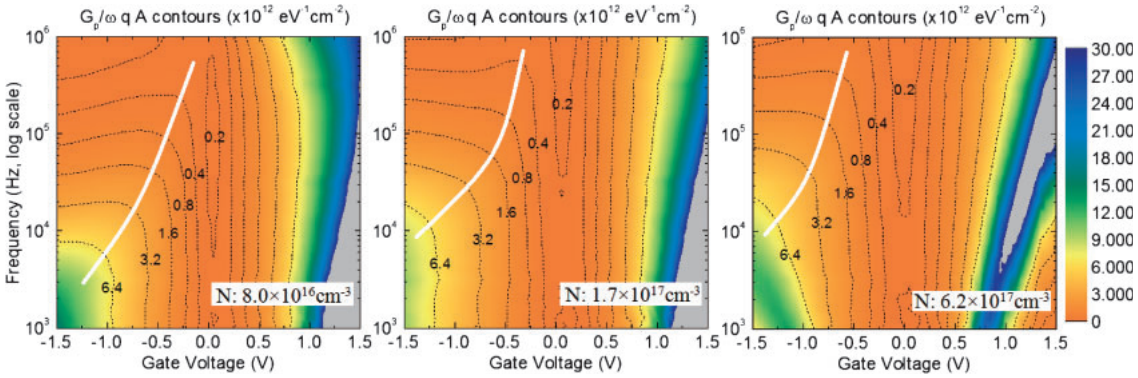

Fig. 6. Normalized parallel conductance contour map for 8.0×10^{16}, 1.7×10^{17}, and $6.2 \times 10^{17}\,\mathrm{cm^{-3}}$ Si-doped n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA temperature of 400 °C. The lines indicate the local G_p/ω maxima and trace of surface Fermi level.

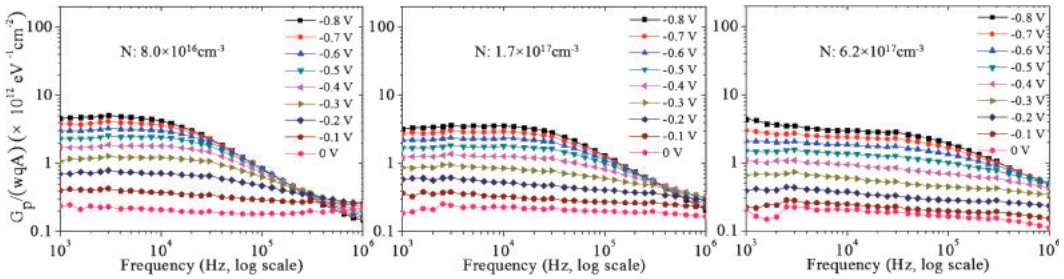

Fig. 7. G_p/wqA (A: $1.96 \times 10^{-5}\,\mathrm{cm^2}$) vs frequency curves at different gate biases after 400 °C PDA for 8.0×10^{16}, 1.7×10^{17}, and $6.2 \times 10^{17}\,\mathrm{cm^{-3}}$ Si-doped n-$In_{0.53}Ga_{0.47}As$ MOS capacitors.

$$D_{it} = \frac{\Delta C}{q^2}\left(1 - \frac{C_{HF} + \Delta C}{C_i}\right)^{-1}\left(1 - \frac{C_{HF}}{C_i}\right)^{-1} \qquad (3)$$

Here, C_i is the insulator capacitance and $\Delta C = C_{LF} - C_{HF}$; C_{LF} is the low-frequency capacitance and C_{HF} is the high-frequency capacitance. However, the D_{it} dependence on ΔC is as shown by Eq. (3). ΔC increases with higher PDA temperature in this case, indicating that the number of Ga-related oxides increased at the surface between the semiconductor and the oxide when the PDA temperature was increased from 400 to 500 °C, as shown in Fig. 3, and the annealing also results in higher D_{it}.

Figure 5 shows the multifrequency *C–V* curves for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs on the Si substrate with a PDA temperature of 400 °C. Small frequency dispersions of 2.74, 2.52, and 2.37%/decade were achieved owing to fewer border traps caused by the decrease in the amount of Ga oxides, and excellent hystereses of 76, 65, and 84 mV were observed for the 8.0×10^{16}, 1.7×10^{17}, and $6.2 \times 10^{17}\,\mathrm{cm^{-3}}$ Si-doped n-$In_{0.53}Ga_{0.47}As$ layers, respectively, owing to the reduction in oxide-related traps when the PDA temperature was 400 °C. Figure 6 shows the map of normalized parallel conductance $[(G_p/\omega)/Aq]$, with contour lines at 300 K as a function of frequency and gate bias for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP on the Si substrate. G_p, ω, A, and q are the parallel conductance, angular frequency, gate area, and elemental charge, respectively. From the figure, the conductance peak maximum shifts to a frequency of 1 kHz, which indicates that the movement of the Fermi level into the lower part (the energy position is less than 0.375 eV for $E - E_v$) of the InGaAs band gap is possible.[21)]

Figure 7 shows G_p/wqA vs frequency plots for $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs on the Si substrate with PDA at 400 °C. For interface trap analysis, Eq. (4) can be achieved

Table I. D_{it} values ($cm^{-2}\,eV^{-1}$) for Al_2O_3 (8 nm) on 8.0×10^{16}, 1.7×10^{17}, and $6.2 \times 10^{17}\,cm^{-3}$ Si-doped n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA temperatures of 400 and 500 °C.

	Doping concentration N (cm^{-3})		
	8.0×10^{16}	1.7×10^{17}	6.2×10^{17}
PDA 400 °C	5.80×10^{11}	5.87×10^{11}	5.44×10^{11}
PDA 500 °C	1.45×10^{12}	1.56×10^{12}	1.62×10^{12}

using the equivalent circuit of a MOS capacitor for interface traps with a single energy level in the band gap:

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \quad (4)$$

Here, G_p is the parallel conductance, $\omega = 2\pi f$ (f is the measurement frequency), and τ_{it} is the interface trap time constant. Interface traps at the oxide and semiconductor interface, however, are continuously distributed in energy throughout the semiconductor band gap, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln[1+(\omega\tau_{it})^2]. \quad (5)$$

G_p/ω is maximum at $\omega \approx 2/\tau_{it}$ and D_{it} is estimated by multiplying the normalized conductance peak value with a factor of 2.5 as[22)]

$$D_{it} = 2.5\left(\frac{G_p}{\omega qA}\right)_{max}. \quad (6)$$

Table I shows the comparison of D_{it} values for the three samples with different doping concentrations and with PDA at 400 and 500 °C. The similar D_{it} distribution with comparable mid-gap (above E_v 0.3 to 0.42 eV) D_{it} values of $5.5 \times 10^{11}\,cm^{-2}\,eV^{-1}$ for the MOSCAPs on the Si substrate and the $In_{0.53}Ga_{0.47}As$ MOSCAPs on the InP substrate indicates that the qualities of the $In_{0.53}Ga_{0.47}As$ layer on the Si substrate in this study and the $In_{0.53}Ga_{0.47}As$ layer grown on the InP substrate in previous reports are the same.[23)] D_{it} increased when the PDA temperature was increased to 500 °C; this phenomenon is consistent with the results of the XPS spectra. Thus, the increase in the number of Ga-related oxides at the surface results in D_{it} increase.

In summary, an $In_{0.53}Ga_{0.47}As$ heterostructure has been successfully grown on a 300 mm on-axis Si(100) substrate by MOCVD. The $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs fabricated on the Si substrate show excellent capacitance–voltage characteristics with a small frequency dispersion of approximately 2.5%/decade and a low D_{it} in the range of 5×10^{11} $cm^{-2}\,eV^{-1}$. The data are comparable to that of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP grown on the lattice-matched InP substrate. The results demonstrate the potential of integrating an InGaAs-based material on a 12 in. Si substrate by MOCVD for future high-performance low-power logic device applications and mainstream manufacturing.

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