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Effects of layer sequence and postdeposition annealing temperature on performance of La_2O_3 and HfO_2 multilayer composite oxides on $In_{0.53}Ga_{0.47}As$ for MOS capacitor application

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In this paper, we report on high-*k* composite oxides that are formed by depositing multiple layers of HfO_2 and La_2O_3 on $In_{0.53}Ga_{0.47}As$ for MOS device application. Both multilayer HfO_2 (0.8 nm)/La_2O_3 (0.8 nm)/$In_{0.53}Ga_{0.47}As$ and La_2O_3 (0.8 nm)/HfO_2 (0.8 nm)/$In_{0.53}Ga_{0.47}As$ MOS structures were investigated. The effects of oxide thickness and postdeposition annealing (PDA) temperature on the interface properties of the composite oxide MOS capacitors were studied. It was found that a low CET of 1.41 nm at 1 kHz was achieved using three-layer composite oxides. On the other hand, a small frequency dispersion of 2.8% and an excellent D_{it} of $7.0 \times 10^{11}\,cm^{-2}\cdot eV^{-1}$ can be achieved using multiple layers of La_2O_3 (0.8 nm) and HfO_2 (0.8 nm) on the $In_{0.53}Ga_{0.47}As$ MOS capacitor with optimum thermal treatment and layer thickness.
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Recently, $In_xGa_{1-x}As$ metal–oxide–semiconductor field-effect transistors (MOSFETs) have been widely investigated owing to the high electron mobility of the $In_xGa_{1-x}As$ material and the much lower turn-on voltage of $In_xGa_{1-x}As$ devices than of conventional Si devices.[1–4] Rare-earth oxides (REOs) exhibit high dielectric constant and high conduction band offset with respect to silicon and are currently being investigated as high-*k* gate dielectrics for future ultrascaled devices.[5–9] Among the binary REOs, La_2O_3 is considered as one of the most promising gate dielectric materials owing to its high κ and high band-gap energy. However, strong interdiffusion between InGaAs and La_2O_3 occurs after postdeposition annealing (PDA) when La_2O_3 is in direct contact with the $In_xGa_{1-x}As$ material.[10] In recent years, several groups have studied composite oxides such as HfO_2/Al_2O_3,[11] CeO_2/Al_2O_3,[12] and CeO_2/HfO_2[13] on InGaAs for next-generation device applications.

In this work, high-*k* composite oxides of La_2O_3 and HfO_2 are investigated for n-$In_{0.53}Ga_{0.47}As$ MOS capacitor application. HfO_2 is chosen because it has a *k* of 25 and an energy band gap of 5.5 eV, and is known to demonstrate inversion behavior with $In_xGa_{1-x}As$.[14–18] An in situ molecular beam deposition (MBD) system was used to deposit the multiple layers of HfO_2 (0.8 nm) and La_2O_3 (0.8 nm) on n-$In_{0.53}Ga_{0.47}As$. The effects of PDA temperature and annealing gas atmosphere on the interface properties and device performances of HfO_2/La_2O_3/n-$In_{0.53}Ga_{0.47}As$ and La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors are studied.

The device structure includes a 100 nm $In_{0.53}Ga_{0.47}As$ layer with $5 \times 10^{17}\,cm^{-3}$ Si doping grown on the n-InP substrate by molecular beam epitaxy (MBE). The device process can be divided into four parts: surface treatment, oxide deposition, gate metal deposition, and ohmic contact formation. The wafers were first cleaned in 4% HCl solution for 3 min, followed by an $(NH_4)_2S$ solution dip for 30 min at room temperature. Then, the wafers were loaded into the MBD system to deposit the HfO_2 (0.8 nm)/La_2O_3 (0.8 nm) multilayers on n-$In_{0.53}Ga_{0.47}As$ at 300 °C. The 10 layers of HfO_2 (0.8 nm) and La_2O_3 (0.8 nm) MOS capacitors were fabricated and annealed at temperatures ranging from 400 to 550 °C in N_2 for 5 min. Then, Ni/Au was deposited on the front side of the wafer as the gate contact metal and Au/Ge/Ni/Au was deposited on the back side of the n+ InP substrate as ohmic metal; both were deposited using an e-beam evaporator and the ohmic metal was annealed at 250 °C for 30 s for optimum contact resistance.

Figure 1 shows the X-ray photoelectron spectroscopy (XPS) spectra of the HfO_2 (0.8 nm)/La_2O_3 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ and La_2O_3 (0.8 nm)/HfO_2 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ composite oxide structures annealed at 400, 500, and 550 °C in N_2 for 5 min. The As 3d, Ga $2p_{3/2}$, In $3d_{5/2}$, and O 1s XPS spectra of the samples with different PDA temperatures were analyzed to determine the film compositions and interface properties. In general, with increasing PDA temperature, more interactions between oxides and semiconductors occur, and the number of As–As bonds is reduced owing to the high-temperature annealing, as indicated by As 3d in Fig. 1. When the PDA temperature was increased to 500 °C, the amounts of As-, Ga-, and In-related oxides decreased for both composite oxide structures. The amount of La_2O_3 increased for the La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ structure, as indicated by the XPS O 1s peak in Fig. 1. The slight reduction of the native oxides could be explained by the conversion of As–O, Ga–O, and In–O bonds to InAs, GaAs, and La_2O_3 during thermal annealing for the La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ structure. However, the amount of La_2O_3 that diffused into InGaAs increased with temperature for the HfO_2/La_2O_3/n-$In_{0.53}Ga_{0.47}As$ structure. The 500 °C annealing not only converted the As–O, Ga–O, and In–O bonds to InAs and GaAs bonds but also resulted in the increase in the amount of La_2O_3 diffusing into InGaAs for the HfO_2/La_2O_3/n-$In_{0.53}Ga_{0.47}As$ structure. Furthermore, the amounts of As-, Ga-, and In-related oxides increased significantly for both composite oxide structures when the PDA temperature was increased to 550 °C, as indicated by the As 3d, Ga $2p_{3/2}$, and In $3d_{5/2}$ spectra in Fig. 1. This indicates that at the PDA temperature of 550 °C, the diffusions of As, Ga, and In into the oxide layers were quite significant for both composite oxide structures.

Figure 2 shows the comparison of capacitance–voltage (C–V) curves at 1 MHz for the five layers of HfO_2 (0.8 nm)/La_2O_3 (0.8 nm) and the five layers of La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) composite oxides on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors, and the HfO_2 (8 nm)/n-$In_{0.53}Ga_{0.47}As$ MOS

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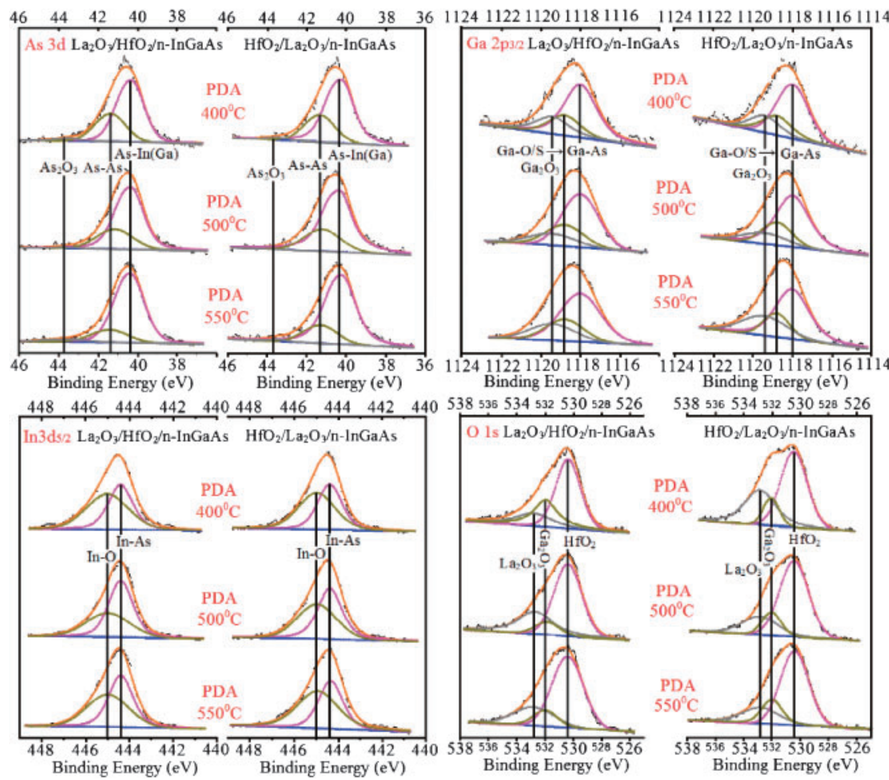

Fig. 1. As 3d, Ga $2p_{3/2}$, In $3d_{5/2}$, and O 1s XPS spectra of La_2O_3 (0.8 nm)/HfO_2 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ and HfO_2 (0.8 nm)/La_2O_3 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ with postdeposition annealing temperatures of 400, 500, and 550 °C in nitrogen gas for 5 min.

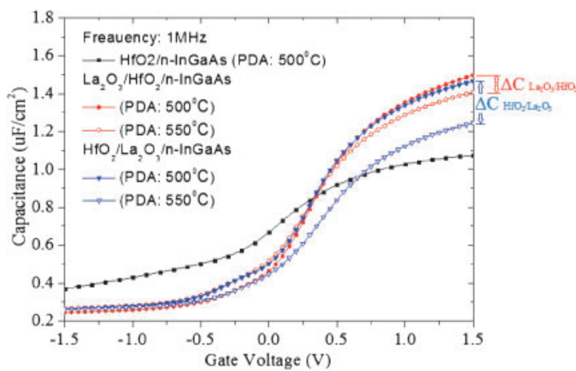

Fig. 2. Comparison of C–V characteristics of HfO_2 (8 nm)/n-$In_{0.53}Ga_{0.47}As$, La_2O_3 (0.8 nm)/HfO_2 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ and HfO_2 (0.8 nm)/La_2O_3 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors.

capacitor. The electrical characteristics of the composite oxide MOS capacitor were markedly improved when the devices were annealed at the PDA temperature of 500 °C in N_2 for 5 min. The dielectric constants of 15.2 and 14.8 were estimated for the five layers of the La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) and HfO_2 (0.8 nm)/La_2O_3 (0.8 nm) composite oxides on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors, respectively.

Some reports show that the semiconductor elements will diffuse into the oxide after annealing, resulting in the decrease in the oxide dielectric constant and the increase in the device capacitance equivalent thickness (CET).[19] In this case,

$$\mathrm{CET} = \frac{\varepsilon_0 \varepsilon_{\mathrm{SiO2}}}{C(\mathrm{accum.@}\ f = 1\,\mathrm{k})},$$

where $C(\mathrm{accum.@}\ f = 1\,\mathrm{kHz})$ is the capacitance of the accumulation region at frequency = 1 kHz, ε_0 is the vacuum permittivity, and $\varepsilon_{\mathrm{SiO2}}$ is relative permittivity of SiO_2. A CET of 2.2 nm at 1 kHz with a low interface trap density (D_{it}) of $7.0 \times 10^{11}\,\mathrm{cm^{-2}{\cdot}eV^{-1}}$ was achieved, as estimated by the conductance method[20] for the La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ capacitor, as shown in Fig. 3(a). A higher D_{it} and a lower CET were obtained for the HfO_2 (0.8 nm)/La_2O_3 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ device owing to the strong interaction between La_2O_3 and n-$In_{0.53}Ga_{0.47}As$. When the PDA temperature was increased, the interaction between the oxide and the semiconductor increased. The Gp/wqA vs frequency plot and D_{it} vs energy plot for the 5 layers of La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) and HfO_2 (0.8 nm)/La_2O_3 (0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at 500 °C are shown in Figs. 4(a) and 4(b), respectively. From Fig. 4(b), the low D_{it} of 7.0×10^{11}–$1.0 \times 10^{12}\,\mathrm{cm^{-2}{\cdot}eV^{-1}}$ in the energy range of 0.47–0.44 eV above the $In_{0.53}Ga_{0.47}As$ valence band maximum was obtained for the La_2O_3 (0.8 nm)/HfO_2 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ device. When the PDA temperature was increased to 550 °C, the capacitance decreased from 1.46 (500 °C) to 1.39 μF/cm^2 (550 °C) and 1.44 (500 °C) to 1.20 μF/cm^2 (550 °C) for the La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ structure and HfO_2/La_2O_3/n-$In_{0.53}Ga_{0.47}As$ structure, respectively. The larger capacitance decrease, particularly for the HfO_2 (0.8 nm)/La_2O_3 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ capacitor, was due to the strong interdiffusion between La_2O_3 and InGaAs after high-temperature annealing. The C–V characteristics of the composite oxide capacitors with PDA temperatures of 400, 500, and 550 °C and different oxide thicknesses are compared in Table I.

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Table I. Comparison of *C–V* characteristics of HfO_2 (8 nm)/n-$In_{0.53}Ga_{0.47}As$, La_2O_3 (0.8 nm)/HfO_2 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ and HfO_2 (0.8 nm)/La_2O_3 (0.8 nm)/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors.

Device oxide structure			CET at 1 kHz (nm)	Accumulation capacitance ($\mu F/cm^2$)		Frequency dispersion (%)	D_{it} ($10^{12}\,cm^{-2}\cdot eV^{-1}$)
				at 1 kHz	at 1 MHz		
8 nm HfO_2 PDA at 500 °C in N_2			2.71	1.30	1.07	5.1	2.58
(La_2O_3/HfO_2) × 5 PDA at (°C)	400	N_2	—	—	—	—	25.10
	500	N_2	2.21	1.60	1.46	3.5	0.70
		Forming gas	2.34	1.51	1.42	2.9	1.05
	550	N_2	2.23	1.58	1.39	3.5	0.90
(La_2O_3/HfO_2) × 4 PDA at (°C)	500	N_2	1.77	2.0	1.71	4.6	1.52
(La_2O_3/HfO_2) × 3 PDA at (°C)	500	N_2	1.41	2.52	2.04	5.0	2.21
(HfO_2/La_2O_3) × 5 PDA at (°C)	400	N_2	2.26	1.56	1.35	4.2	2.91
	500	N_2	2.25	1.57	1.44	2.8	0.97
		Forming gas	2.50	1.41	1.32	2.6	1.12
	550	N_2	2.52	1.40	1.20	4.2	1.80

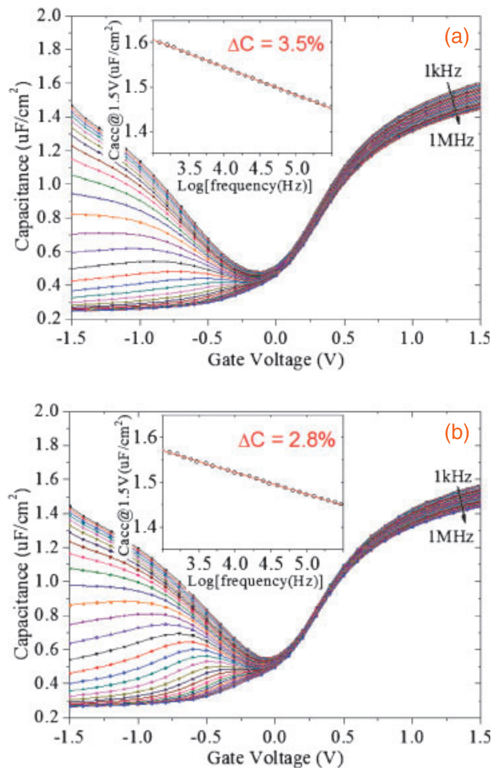

Fig. 3. *C–V* characteristics of 5 layers of (a) La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) and (b) HfO_2 (0.8 nm)/La_2O_3 (0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at 500 °C in N_2 gas for 5 min.

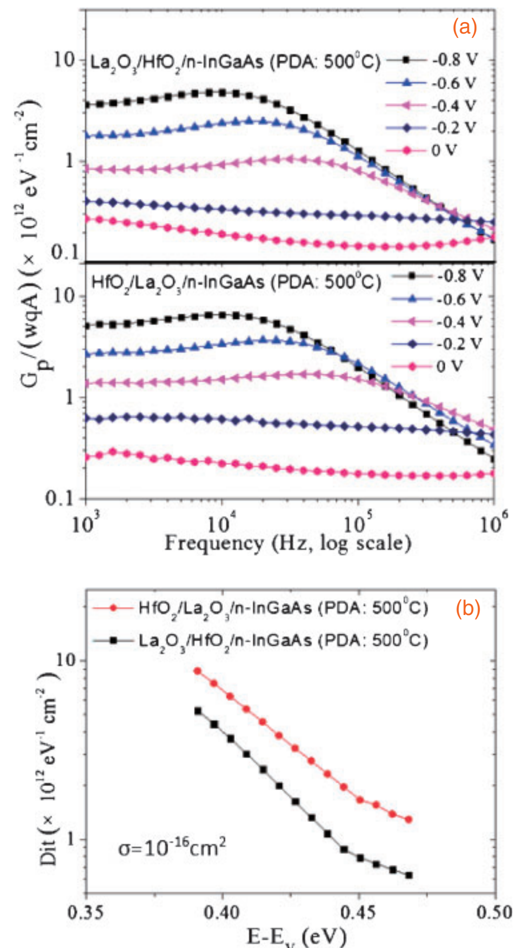

Fig. 4. (a) Gp/wqA (A: $1.33 \times 10^{-4}\,cm^2$) vs frequency curves at different gate biases and (b) D_{it} vs energy curves after 500 °C PDA for 5 layers of La_2O_3 (0.8 nm)/HfO (0.8 nm) and HfO_2 (0.8 nm)/La_2O_3 (0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS devices.

Furthermore, the device performance was further improved by forming gas (5% H_2 + 95% N_2) annealing. Figure 5 shows the *C–V* characteristics of the 5 layers of La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) and the 5 layers of La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at 500 °C in forming gas for 5 min. Frequency dispersion was improved owing to H_2 treatment,[21] especially for the La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ structure. The frequency dispersions were reduced from 3.5 to 2.9% and 2.8 to 2.6% for the La_2O_3/HfO_2/n-$In_{0.53}Ga_{0.47}As$ structure and HfO_2/La_2O_3/n-$In_{0.53}Ga_{0.47}As$ structure, respectively. However, the capacitances of both devices decreased after forming

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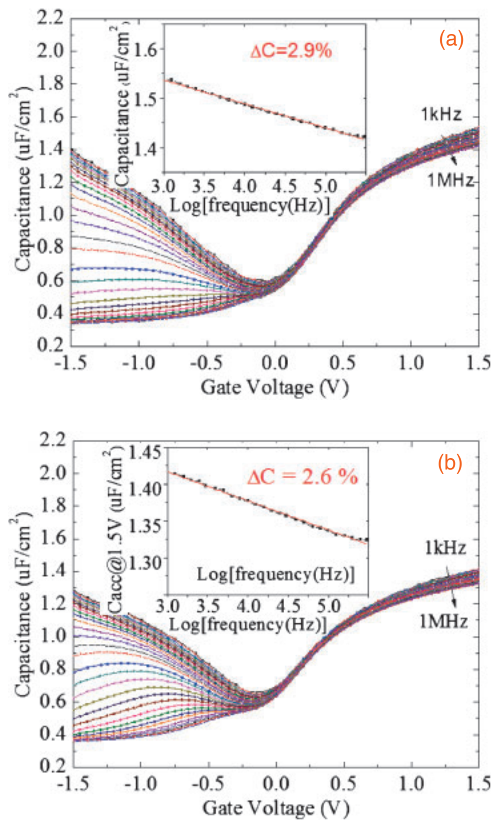

Fig. 5. *C–V* characteristics of the five layers of (a) La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) and (b) HfO_2 (0.8 nm)/La_2O_3 (0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at 500 °C in forming gas for 5 min.

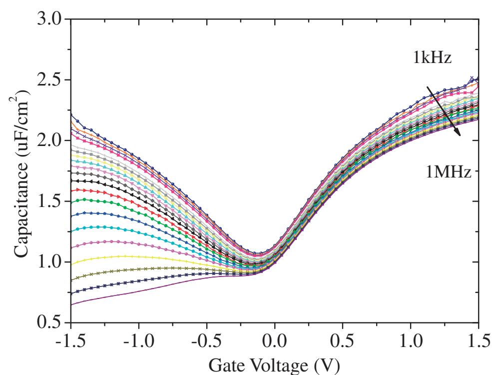

Fig. 6. *C–V* characteristics of three layers of La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) on n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at 500 °C in nitrogen gas for 5 min.

gas annealing. The device CET was improved for the 3 and 4 layers of the La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) structure on the n-$In_{0.53}Ga_{0.47}As$ device after PDA at 500 °C for 5 min in N_2 atmosphere. The *C–V* curves for the 3-layer device are shown in Fig. 6; for the composite oxide with 3 and 4 layers of the La_2O_3 (0.8 nm)/HfO_2 (0.8 nm) structure, the CETs were reduced to 1.77 and 1.41 nm, respectively, after 500 °C annealing, as measured at 1 kHz.

In summary, high-*k* composite dielectrics composed of La_2O_3 and HfO_2 layers on n-$In_{0.53}Ga_{0.47}As$ for MOS capacitor application are investigated. Overall, the La_2O_3/HfO_2 structure on the n-$In_{0.53}Ga_{0.47}As$ MOS capacitor demonstrates better performance than the HfO_2/La_2O_3 structure on the n-$In_{0.53}Ga_{0.47}As$ MOS capacitor after thermal treatment owing to the interaction between the composite oxides and InGaAs materials. A low CET of 1.41 nm at 1 kHz for 3 layers, a small frequency dispersion of 2.6%, and an excellent D_{it} of 7.0×10^{11} $cm^{-2}\cdot eV^{-1}$ can be achieved using multiple layers of La_2O_3 (0.8 nm) and HfO_2 (0.8 nm) on $In_{0.53}Ga_{0.47}As$ MOS capacitors with PDA at 500 °C.

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