The Determination of S-Parameters From the Poles of Voltage-Gain Transfer Function for RF IC Design

Shey-Shi Lu, *Senior Member, IEEE*, Yo-Sheng Lin, *Member, IEEE*, Hung-Wei Chiu, Yu-Chang Chen, and Chin-Chun Meng, *Member, IEEE*

***Abstract*—A method for estimating the S-parameters of active circuits using hand analysis is introduced. This method involves the determination of S-parameters from the poles of voltage-gain transfer function. It is found that the information on the frequency responses of input/output return loss, input/output impedance, and reverse isolation is all hidden in the poles or equivalently in the denominator of the voltage-gain transfer function of a circuit system. The method has been applied to three commonly used RF circuit configurations and one fabricated CMOS wide-band amplifier to illustrate the usefulness of the proposed theory.**

***Index Terms*—Broad-band amplifier, poles, S-parameters, transfer function.**

I. Introduction

IT IS well known that the frequency response of voltage gain of a circuit can be determined from the poles and zeros of the voltage-gain transfer function [1]. While knowing the voltage gain (or S_{21}) is enough in traditional analog circuit design, additional information on the input and output return losses (or S_{11} and S_{22}) is indispensable in microwave radio frequency (RF) circuit design because input/output impedance matching is important. In addition, the reverse isolation (or reverse voltage gain S_{12}) of a circuit has to be found to ensure circuit stability. Usually, the conventional analog circuit design starts from the calculation of the voltage-gain transfer function. One of the systematic approaches to derive the denominator of a transfer function efficiently is to write down the simultaneous equations by node or mesh analysis [2] and then find the determinant of the simultaneous equations. Some examples of how to derive the voltage-gain transfer function of a circuit efficiently can also be found in [3]. From the denominator and the numerator of the transfer function, poles and zeros are found, respectively. With the information of poles and zeros plus dc or mid-band gain, the frequency response of voltage gain of a circuit can be described. In a 50-Ω lossless transmission line system, S_{21} is consequently obtained because it is twice the voltage gain if the source impedance associated with voltage source is 50 Ω and the output port is matched [4]. As to the input and output return losses (or S_{11} and S_{22}), cumbersome calculations have to be done to find the input and output impedances, not to mention the tedious work in obtaining reverse voltage gain, which is one half of S_{12} in a 50-Ω circuit system. That is, all of the necessary quantities (or S-parameters) are calculated independently according to the traditional approach of analog circuit design.

For the circuits whose expressions of Y-parameters, Z-parameters, or other small-signal parameters can be easily obtained, the expressions of S-parameters can be obtained by plugging these small-signal parameters into the S-parameter transformations [5], and then simplifying these equations. However, such an approach is too complex and tedious to gain useful insights. There are methods of plugging in to determine S-parameter macros on SPICE for the analog circuit [6], but they do not give the analytical forms. Therefore, in this paper, a technique to perform useful S-parameter estimation using hand analysis is introduced. Specifically, a method for the determination of S-parameters and input/output impedance from the poles of the denominator of the voltage-gain transfer function is presented. It is found that input/output return loss, input/output impedance, and reverse isolation/gain can be derived from the expressions of poles or, equivalently, the denominator of the voltage-gain transfer function. That is, input/output return loss, input/output impedance, and reverse isolation/gain can be found in a unified way. In Section II, the theory of determining S-parameters from the poles of the voltage-gain transfer function is presented. In Section III, three commonly used RF circuits are taken as examples to illustrate the proposed theory.

In addition, broad-band amplifiers are used in a large variety of applications, such as wireless systems, instrumentation, and optical communications [7]–[11]. Among the variety of broad-band amplifiers, the Kukeilka configuration is one of the most popular circuits [11], [12]. However, no detailed analysis of this kind of circuit implemented in CMOS technology has ever been presented. To verify the proposed theory, in Section IV, we present the derived analytic expressions of the closed-loop poles, voltage/current gain, input/output impedance, input/output return loss, reverse isolation/gain, and transimpedance gain for the CMOS broad-band amplifier with the Kukeilka configuration. The predicted results (12.8-dB gain and 2.0-GHz bandwidth) from our theory are consistent with the simulated (12.3-dB gain and 2.1-GHz bandwidth) and measured results (10.5-dB gain and 1.7-GHz bandwidth), suggesting that our theory can be successfully applied to CMOS RF IC design.

Manuscript received January 8, 2004; revised May 22, 2004 and July 30, 2004. This work was supported by the National Science Council under Grant NSC93-2215E002-028, Grant 91EC17A05-S10017, and Grant NSC93-2752-E002-002-PAE. This paper was recommended by Associate Editor P. K. Rajan.

S.-S. Lu, H.-W. Chiu, and Y.-C. Chen are with the Department of Electrical Engineering and Graduate Institute of Electronics, National Taiwan University, Taipei, Taiwan, R.O.C. (e-mail: sslu@ntu.edu.tw).

Y.-S. Lin is with the Department of Electrical Engineering, National Chi-Nan University, Puli, Taiwan, R.O.C. (e-mail: stephenlin@ncnu.edu.tw).

C.-C. Meng is with the Department of Communication Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C. (e-mail: ccmeng@mail.nctu.edu.tw).

Digital Object Identifier 10.1109/TCSI.2004.840084

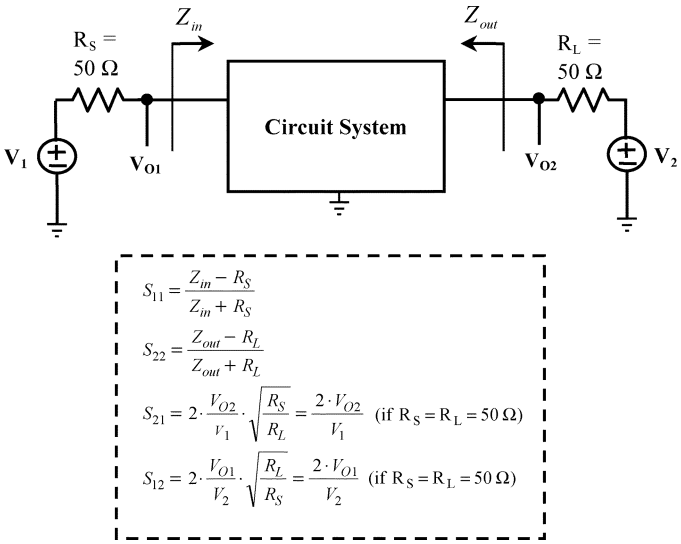


Fig. 1. Setup for the measurement/simulation of the S-parameters of a circuit system in the context of a 50-Ω measurement/simulation system.

II. Theory

Assume that the voltage-gain transfer function of a circuit system is known and is given by

$$H(s, R_S, R_L) = A_M \cdot \frac{N(s, R_S, R_L)}{D(s, R_S, R_L)} \tag{1}$$

where A_M is dc or mid-band gain, $R_S = 50\ \Omega$ is source resistance of the voltage source, $R_L = 50\ \Omega$ is load resistance, and $N(s, R_S, R_L)$ and $D(s, R_S, R_L)$ stand for the numerator and denominator of the transfer function for solving, respectively, zeros and poles. Note that the numerator and denominator, in general, are functions of R_S and R_L. In a 50-Ω system, $R_S = R_L = 50\ \Omega$. To facilitate the following discussion, we will call the denominator of the transfer function the characteristic equation $D(s, R_S, R_L) = 0$.

The setup for the measurement/simulation of the S-parameters of a circuit system is shown in Fig. 1. R_S (the source impedance associated with the voltage source) and R_L (load impedance) are connected to the input and output ports of the circuit system, respectively, and are equal to the characteristic impedance (50 Ω) of the input and output transmission lines, which are assumed to be lossless. S_{11} and S_{21} can be obtained by setting $V_2 = 0$ and $V_1 \neq 0$, while S_{22} and S_{12} can be obtained by setting $V_1 = 0$ and $V_2 \neq 0$. What are also shown in Fig. 1 are the expressions of the S-parameters in terms of the parameters shown in Fig. 1. Since S_{21} is twice the voltage gain under the previous assumed condition, S_{21} can be obtained easily and is equal to $2 \cdot H(s, R_s, R_L)$. In order to find input return loss $= 20 \log |S_{11}|$, S_{11} has to be determined. By definition, S_{11} is given by

$$S_{11} = \frac{Z_{\text{in}} - R_S}{Z_{\text{in}} + R_S} \tag{2}$$

where Z_{in} is the input impedance of the circuit. The poles of S_{11} are the roots of $Z_{\text{in}} + R_S = 0$. From the expressions of S–parameters in terms of Z- or Y-parameters [6], it is found that the denominators, or the poles, of all S-parameters are the same. Hence, $Z_{\text{in}} + R_S = 0$ is equivalent to the characteristic equation $D(s, R_S, R_L) = 0$ for the poles of voltage gain. That is

$$Z_{\text{in}} + R_S = 0 \sim D(s, R_S, R_L) = 0 \tag{3}$$

where the symbol "$\sim$" stands for "equivalent to." The zeros of S_{11} are the roots of the zero equation $Z_{\text{in}} - R_S = 0$. This zero equation can be viewed as the transformation of the pole equation $Z_{\text{in}} + R_S = 0$ with R_S replaced by $-R_S$. This implies that

$$Z_{\text{in}} - R_S = 0 \sim D(s, -R_S, R_L) = 0. \tag{4}$$

In other words, the zeros of S_{11} can be obtained by replacing R_S in the expressions of the poles with $-R_S$. At dc or mid-band frequencies, $S_{11} = (R_{\text{in}} - R_S)/(R_{\text{in}} + R_S)$, where R_{in} is the input resistance and is assumed to be known. Therefore, S_{11} can be written as follows for all frequencies:

$$S_{11} = \frac{Z_{\text{in}} - R_S}{Z_{\text{in}} + R_S} = \frac{R_{\text{in}} - R_S}{R_{\text{in}} + R_S} \cdot \frac{D(s, -R_S, R_L)}{D(s, R_S, R_L)}. \tag{5}$$

Once S_{11} is known, Z_{in} can be readily obtained. According to (3), the other way of finding Z_{in} is to isolate R_S from the other terms in the expression of $D(s, R_S, R_L) = 0$, and the sum of all of the other terms as a whole is Z_{in}. Once Z_{in} is known, S_{11} can be readily obtained. Based on similar arguments, S_{22} can be given by

$$S_{22} = \frac{Z_{\text{out}} - R_L}{Z_{\text{out}} + R_L} = \frac{R_{\text{out}} - R_L}{R_{\text{out}} + R_L} \cdot \frac{D(s, R_S, -R_L)}{D(s, R_S, R_L)} \tag{6}$$

where R_{out} is the output resistance and is assumed to be known. Once S_{22} is known, Z_{out} can be readily obtained. The other way of finding Z_{out} is to isolate R_L from the other terms in the expression of $D(s, R_S, R_L) = 0$ and the sum of all of the other terms as a whole is Z_{out}. Once Z_{out} is known, S_{22} can be readily obtained.

S_{12} is twice the reverse voltage gain. Since the poles of S_{12} are the same as those of $H(s)$, S_{12} can be completely described if the dc or mid-band gain and the zeros of the "reverse circuit" are known.

III. Applications

To illustrate the method presented in Section II, three circuits are used as examples: 1) the shunt–shunt feedback amplifier; 2) the source inductor feedback low noise amplifier; and 3) the simple common source amplifier.

A. Shunt–Shunt Feedback Amplifier

The schematic and the small-signal equivalent circuit of a two-stage local shunt–shunt feedback amplifier are shown in Fig. 2(a) and (b), respectively. For clarity and simplicity, gate-to-drain capacitance and the output resistance of transistors are neglected. The transfer function of voltage gain $H(s)$ is given by

$$H(s) = \frac{g_{m1}\left(g_{m2} - R_F^{-1}\right) R_F R_L}{1 + g_{m2} R_L} \frac{1}{D(s, R_S, R_L)} \tag{7}$$

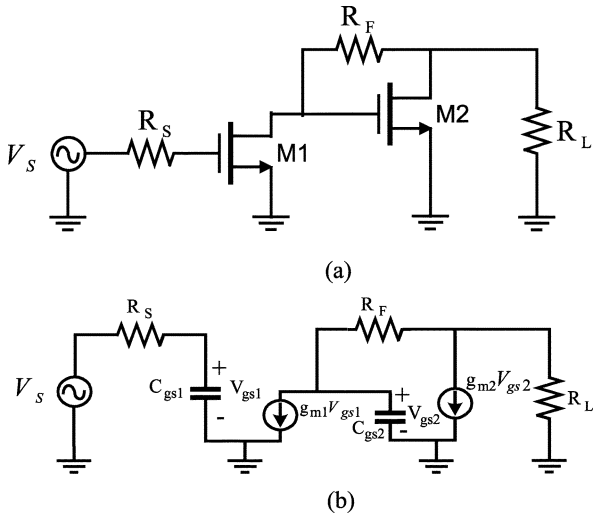


Fig. 2. (a) Schematic and (b) small-signal equivalent circuit of the shunt–shunt feedback amplifier.

where

$$D(s,R_S,R_L)=\left(1+\frac{s}{\frac{1}{R_SC_{gs1}}}\right)\left(1+\frac{s}{\frac{1}{\frac{R_F+R_L}{1+g_{m2}R_L}C_{gs2}}}\right)$$
$$=(1+sC_{gs1}R_S)\left(1+sC_{gs2}\frac{R_F+R_L}{1+g_{m2}R_L}\right). \quad (8)$$

Once $H(s)$ is known, S_{21} is two times of (7). According to conventional circuit analysis, Z_{in} and Z_{out} have to be calculated in order to find S_{11} and S_{22}. Based on direct circuit analysis, they can be shown as follows:

$$Z_{\text{in}}=\frac{1}{sC_{gs1}} \quad (9a)$$
$$Z_{\text{out}}=\frac{R_F+\frac{1}{sC_{gs2}}}{1+g_{m2}\frac{1}{sC_{gs2}}}. \quad (9b)$$

Based on our theory, if we rewrite the expression of $D(s,R_S,R_L)$, Z_{in} and Z_{out} can be found, and they agree with (9a) and (9b) as follows:

$$D(s,R_S,R_L)=sC_{gs1}\left(\frac{g_{m2}+sC_{gs2}}{1+g_{m2}R_L}\right)\left(\frac{1}{sC_{gs1}}+R_S\right)\times\left(\frac{R_F+\frac{1}{sC_{gs2}}}{1+g_{m2}\frac{1}{sC_{gs2}}}+R_L\right)$$
$$=sC_{gs1}\left(\frac{g_{m2}+sC_{gs2}}{1+g_{m2}R_L}\right)\times(Z_{\text{in}}+R_S)(Z_{\text{out}}+R_L). \quad (10)$$

The second way to find S_{11} and S_{22} with our theory is the application of (5) and (6) to yield

$$S_{11}=1\cdot\frac{D(s,-R_S,R_L)}{D(s,R_S,R_L)}=\frac{1+\frac{s}{\frac{1}{-R_SC_{gs1}}}}{1+\frac{s}{\frac{1}{R_SC_{gs1}}}} \quad (11a)$$

$$S_{22}=\frac{\frac{1}{g_{m2}}-R_L}{\frac{1}{g_{m2}}+R_L}\cdot\frac{D(s,R_S,-R_L)}{D(s,R_S,R_L)}$$
$$=\frac{\frac{1}{g_{m2}}-R_L}{\frac{1}{g_{m2}}+R_L}\cdot\frac{1+\frac{s}{\frac{1}{\frac{R_F-R_L}{1-g_{m2}R_L}C_{gs2}}}}{1+\frac{s}{\frac{1}{\frac{R_F+R_L}{1+g_{m2}R_L}C_{gs2}}}}. \quad (11b)$$

It can be shown that the results of (11a) and (11b) are equal to those obtained by inserting (9a) and (9b) into (5) and (6), respectively.

B. Source Inductor Feedback Low-Noise Amplifier

Another commonly used RF circuit is the source inductor feedback low-noise amplifier as shown in Fig. 3(a). If we neglect the gate-to-drain capacitance and the output resistance in the small-signal equivalent circuit as shown in Fig. 3(b), the transfer function can be shown to be

$$H(s)=-g_{m1}\cdot R_L\frac{sC_1(r+sL)}{D(s,R_S,R_L)} \quad (12)$$

where

$$D(s,R_S,R_L)=(1+sC_{gs1}(R_S+\omega_{T1}L_S)+s^2C_{gs1}(L_S+L_g))\cdot\left(1+\frac{s}{\omega_{M2}}\right)\cdot(1+s(R_LC_1+R_LC_2+rC_1)+s^2(rR_LC_1C_2+LC_1)+s^3R_LC_1C_2L) \quad (13)$$

where $\omega_{M2}=g_{m2}/C_{gs2}$. By isolating R_S and R_L from the other terms, Z_{in} and Z_{out} were found to be

$$Z_{\text{in}}=\frac{1}{sC_{gs1}}+s(L_S+L_g)+\omega_{M1}L_S \quad (14a)$$
$$Z_{\text{out}}=\frac{1+s\cdot rC_1+s^2LC_1}{s(C_1+C_2)+s^2rC_1C_2+s^3LC_1C_2} \quad (14b)$$

where $\omega_{M1}=g_{m1}/C_{gs1}$. The results of (14a) and (14b) are in agreement with those derived from direct circuit analysis. Once Z_{in} and Z_{out} are known, S_{11} and S_{22} can be obtained.

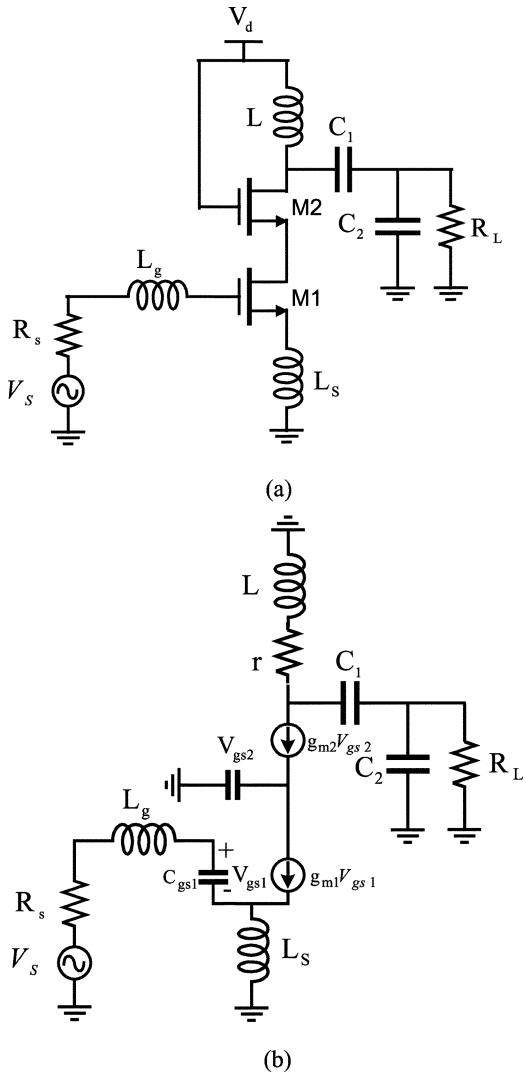


Fig. 3. (a) Schematic and (b) small-signal equivalent circuit of the source inductor feedback low-noise amplifier.

The second way to find S_{11} and S_{22} with our theory is the application of (5) and (6) to yield

$$S_{11} = 1 \cdot \frac{D(s,-R_S,R_L)}{D(s,R_S,R_L)} = \frac{\dfrac{1}{sC_{gs1}} + s(L_S+L_g) + \omega_{M1}L_S - R_S}{\dfrac{1}{sC_{gs1}} + s(L_S+L_g) + \omega_{M1}L_S + R_S} \tag{15a}$$

$$S_{22} = 1 \cdot \frac{D(s,R_S,-R_L)}{D(s,R_S,R_L)} = \frac{\dfrac{1+s\cdot rC_1+s^2LC_1}{s(C_1+C_2)+s^2rC_1C_2+s^3LC_1C_2} - R_L}{\dfrac{1+s\cdot rC_1+s^2LC_1}{s(C_1+C_2)+s^2rC_1C_2+s^3LC_1C_2} + R_L}. \tag{15b}$$

It is clear that the results of (15a) and (15b) are equal to those obtained by inserting (14a) and (14b) into (5) and (6), respectively.

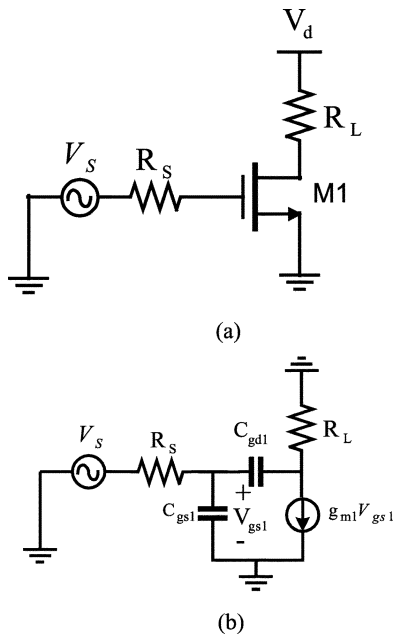


Fig. 4. (a) Schematic and (b) small-signal equivalent circuit of the simple common source amplifier.

C. Simple Common-Source Amplifier

In the previous two examples, the focus is on S_{11} and S_{22}, and the transistor feedback element C_{gd} was neglected for the sake of clarity. However, this assumption inevitably results in zero S_{12} or infinite reverse isolation. A simple common-source amplifier is shown in Fig. 4(a). Now let us consider its small-signal equivalent circuit with C_{gd} taken into account, as shown in Fig. 4(b), and turn our attention to the calculation of S_{12}. S_{12} is twice the reverse-voltage gain. Since the reverse-voltage gain has the same poles as the forward-voltage gain, the remaining thing to do is to find the zeros and dc (or mid-band) reverse-voltage gain. By inspecting Fig. 4(b), the zero is at zero frequency with a near dc gain of $R_S sC_{gd}$ and hence S_{12} is given by

$$S_{12} = 2\frac{R_S sC_{gd}}{D(s,R_S,R_L)} \tag{16a}$$

where

$$D(s,R_S,R_L) = \big(1 + s(R_SC_{gs} + R_LC_{gd} + R_S(g_mR_L+1)C_{gd}) + s^2R_SR_LC_{gs}C_{gd}\big). \tag{16b}$$

The results of (16a) and (16b) agree with those derived from direct circuit analysis.

IV. Analysis of CMOS Broad-Band Amplifier With the Kukielka Configuration

To verify the proposed theory, a Kukeilka configuration broad-band amplifier with dual feedback loops fabricated with a 0.25-μm CMOS process was designed and analyzed.

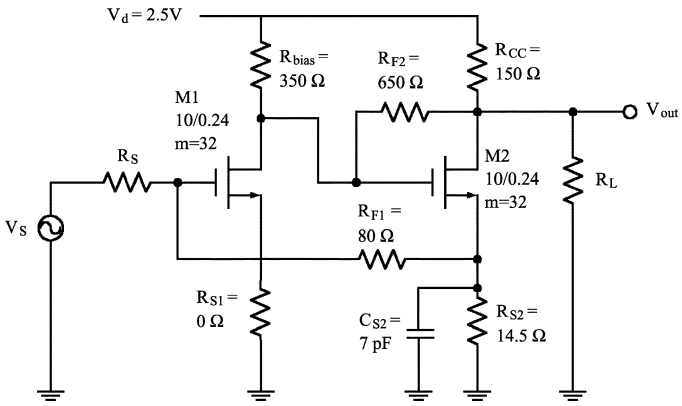


Fig. 5. Schematic of the designed dual-feedback broad-band amplifier with the Kukielka configuration with a 0.25-μm CMOS technology.

A. Circuit Architecture and the Expressions of Its S-Parameters

The schematic of the CMOS broad-band amplifier with the Kukeilka configuration is shown in Fig. 5. The input stage consists of a single nMOS M1, which drives the output stage composed of an nMOS M2 with local shunt (R_{F2}) and series (R_{S2}) feedback. There is also an overall shunt-series feedback loop composed of resistors R_{S2} and R_{F1}. Capacitance C_{S2} is added in parallel to R_{S2} to introduce peaking, which compensates for the overdamped characteristics of this configuration and hence enhances the bandwidth [14]. Clearly, this amplifier can be approximated by a two-pole system with open loop poles of ω_{p1} and ω_{p2} given by [11] and [13], as shown in (17a) and (17b) at bottom of the page, where C_{g1} and C_{g2} are the total gate capacitances of M1 and M2, $R_{\rm sub1}$ and $R_{\rm sub2}$ are the equivalent substrate resistances of M1 and M2, g_{m1} and g_{m2} are the intrinsic transconductances of M1 and M2, g_{mb1} and g_{mb2} are the transconductances of M1 and M2 due to the body effect, $G'_{m1} \equiv g_{m1}/[1+(g_{m1}+g_{mb1})R_{S1}]$ and $G'_{m2} \equiv g_{m2}/[1+(g_{m2}+g_{mb2})R_{S2}]$ are the effective transconductances of M1 and M2, and ω_{T1} and ω_{T2} are the cutoff frequencies of M1 and M2. The closed-loop poles of the voltage-gain transfer function and all four S-parameters of the amplifier are given by [1], [13]

$$\omega_{pn1},\omega_{pn2} = -\frac{1}{2}(\omega_{P1}+\omega_{P2}) \pm \frac{1}{2}\sqrt{(\omega_{P1}+\omega_{P2})^2 - 4(1+T)\omega_{P1}\omega_{P2}} \quad (18)$$

where T is the loop gain, which will be derived later. In the following, first, the expressions of voltage and current gains and input and output impedances at dc frequency will be derived. Then, the expressions of the frequency responses of the amplifier's S-parameters will be described.

1) Voltage and Current Gains and Input and Output Impedances: Fig. 6(a) is the A circuit for the broad-band amplifier without the global shunt-series feedback to calculate the voltage gain. The voltage gain of $V_{\rm out}/V_{\rm in}$ without the global feedback is

$$A_V = \frac{V_{\rm out}}{V_{\rm in}} \approx G'_{m1}R_{K1}G'_{m2}\cdot(R_{F2}\|R_{\rm sub2}\|R_{CC}\|R_L) \approx G'_{m1}R_{F2}\left(1-\frac{R_{K1}}{R_{F2}}\right) \quad (19a)$$

where $R_{K1} = [(R_{F2}+(R_{\rm sub2}\|R_{CC}\|R_L))/(1+G'_{m2}\cdot(R_{\rm sub2}\|R_{CC}\|R_L))]\|[R_{\rm sub1}\|R_{\rm bias}]$ is the impedance at point K1 looking into the gate of M2. The voltage gain with the global feedback with inspection is then

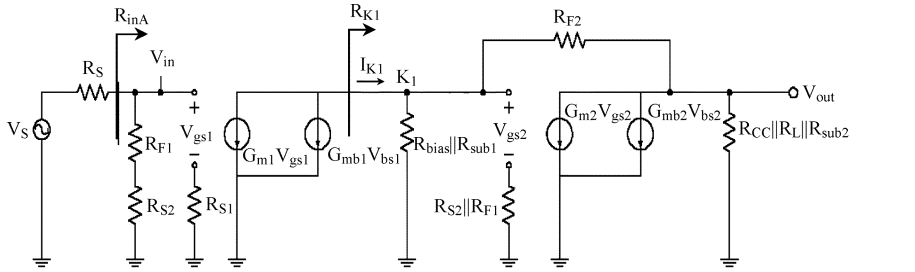
$$A_{VSF} = \frac{V_{\rm in}}{V_s}\cdot\frac{V_{\rm out}}{V_{\rm in}} = \frac{R_{\rm in}}{R_{\rm in}+R_S}\cdot A_V \quad (19b)$$

where $R_{\rm in}$ is the input resistance of the broad-band amplifier with the global feedback, which will be derived later. Fig. 6(b) is the A circuit for the broad-band amplifier without the global

$$\omega_{p1} \approx \frac{g_{m1}}{\dfrac{C_{g1}\cdot g_{m1}}{1+\dfrac{g_{m1}\cdot R_{S1}}{1+g_{mb1}\cdot R_{S1}}}\cdot[(R_S+R_{S1})\|(R_{F1}+R_{S2})]} \approx \frac{\omega_{T1}}{G'_{m1}\cdot R_S} \quad (17a)$$

$$\omega_{p2} \approx \frac{g_{m2}}{\dfrac{C_{g2}\cdot g_{m2}}{1+\dfrac{g_{m2}\cdot R_{S2}}{1+g_{mb2}\cdot R_{S2}}}\cdot\left[\left(\dfrac{R_{F2}+(R_{\rm sub2}\|R_{CC}\|R_L)}{1+G'_{m2}\cdot(R_{\rm sub2}\|R_{CC}\|R_L)}+(R_{S2}\|R_{F1})\right)\|(R_{\rm sub1}\|R_{\rm bias})\right]} \approx \frac{\omega_{T2}}{R_{F2}}\cdot(R_{\rm sub2}\|R_{CC}\|R_L) \quad (17b)$$

$$R_{\rm in} = \frac{R_{F1}+R_{S2}}{1+A_I\cdot\beta_I} = \frac{R_{F1}+R_{S2}}{1+G'_{m1}\cdot G'_{m2}\cdot R_{S2}\cdot\left[\left(\dfrac{R_{F2}+(R_{\rm sub2}\|R_{CC}\|R_L)}{1+G'_{m2}\cdot(R_{\rm sub2}\|R_{CC}\|R_L)}\right)\|(R_{\rm sub1}\|R_{\rm bias})\right]} \quad (21)$$



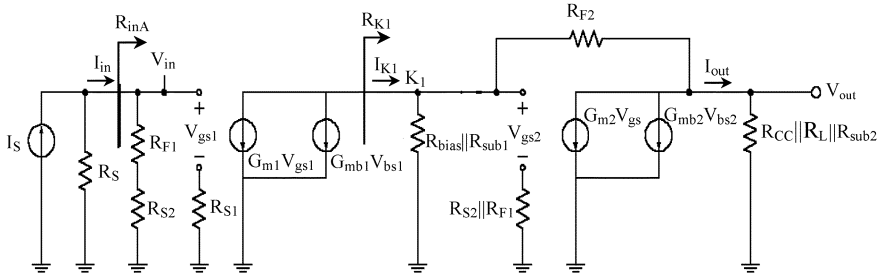
$$G_{m1} \equiv \frac{g_{m1}}{1+g_{m1}R_{S1}} \quad (g_{m1}: \text{intrinsic transconductance of M1})$$

$$G_{mb1} \equiv \frac{g_{mb1}}{1+g_{m1}R_{S1}} \quad (g_{mb1}: \text{transconductance of M1 due to the body effect})$$

$$G_{m2} \equiv \frac{g_{m2}}{1+g_{m2}(R_{S2}\|R_{F1})} \quad (g_{m2}: \text{intrinsic transconductance of M2})$$

$$G_{mb2} \equiv \frac{g_{mb2}}{1+g_{m2}(R_{S2}\|R_{F1})} \quad (g_{mb2}: \text{transconductance of M2 due to the body effect})$$

(a)



(b)

Fig. 6. The A circuit of Fig. 4 for calculating (a) voltage gain and (b) current gain.

shunt-series feedback to calculate the current gain. The feedback factor β_1 is equal to $R_{S2}/(R_{F1}+R_{S2})$. In addition, the current gain $I_{\text{out}}/I_{\text{in}}$ can be easily determined to be

$$\begin{aligned} A_I &= \frac{I_{\text{out}}}{I_{\text{in}}} \\ &= (R_{F1}+R_{S2})\cdot G'_{m1}\cdot G'_{m2} \\ &\quad \cdot \left[\left(\frac{R_{F2}+(R_{\text{sub2}}\|R_{CC}\|R_L)}{1+G'_{m2}\cdot(R_{\text{sub2}}\|R_{CC}\|R_L)}\right)\|(R_{\text{sub1}}\|R_{\text{bias}})\right]. \end{aligned} \tag{20}$$

By inspecting Fig. 6(b), the input resistance of the A circuit is $R_{F1}+R_{S2}$. According to the traditional shunt-series feedback theory, the input resistance with feedback is given by (21), shown at the bottom of the previous page. Then, the loop gain T can be represented as

$$\begin{aligned} T &= A_{IS}\cdot\beta_I = A_I\cdot\frac{R_S}{R_S+R_{F1}+R_{S2}}\cdot\beta_I \\ &= \frac{A_I\cdot\beta_I}{1+(1+A_I\cdot\beta_I)\cdot\frac{R_{\text{in}}}{R_S}}. \end{aligned} \tag{22}$$

Fig. 7 shows the circuit diagram for the calculation of output resistance. A test voltage V_x is applied to the drain node of M2. Assuming that the current flowing through the feedback resistance R_{F1} is negligible, the voltage at point P1 is $V_{P1} = G'_{m2}V_{O1}R_{S2}$. Hence, the voltage at point P2 and the current induced at the source of M1 is $V_{P2} = G'_{m2}V_{O1}R_{S2}R_S/(R_S+R_{F1})$ and $I_{K2} = G'_{m1}G'_{m2}V_{O1}R_{S2}R_S/(R_S+R_{F1})$, respectively. As a result, the resistance R_{K2} looking into the drain of M1 is given by

$$R_{K2} = \frac{V_{O1}}{I_{K2}} = \left(\frac{R_S+R_{F1}}{R_S G'_{m1}G'_{m2}R_{S2}}\right)\|(R_{\text{sub1}}\|R_{\text{bias}}). \tag{23a}$$

Therefore, the output resistance is given by

$$R_{\text{out}} = R'_{\text{out}}\|(R_{\text{sub2}}\|R_{CC}) = \frac{R_{F2}+R_{K2}}{1+G'_{m2}R_{K2}}\|(R_{\text{sub2}}\|R_{CC}). \tag{23b}$$

2) Frequency Responses of S_{21}, S_{11}, S_{22}, and S_{12}: Once the two poles and dc (or mid-band) gain of the voltage-gain transfer function are known, the frequency responses of S_{21} can be determined easily. That is

$$S_{21} = 2\times(\text{voltage gain}) = \frac{2A_{VSF}}{\left(1+\frac{s}{\omega_{pn1}}\right)\left(1+\frac{s}{\omega_{pn2}}\right)} \tag{24a}$$

where A_{VSF} is the voltage gain with the global feedback at dc (or mid-band) frequency. It is known that all S-parameters have the same poles, and the zeros of S_{11} (ω_{Z1} and ω_{Z2}) and S_{22} (ω_{Z3} and ω_{Z4}) can be obtained by replacing R_S and R_L with

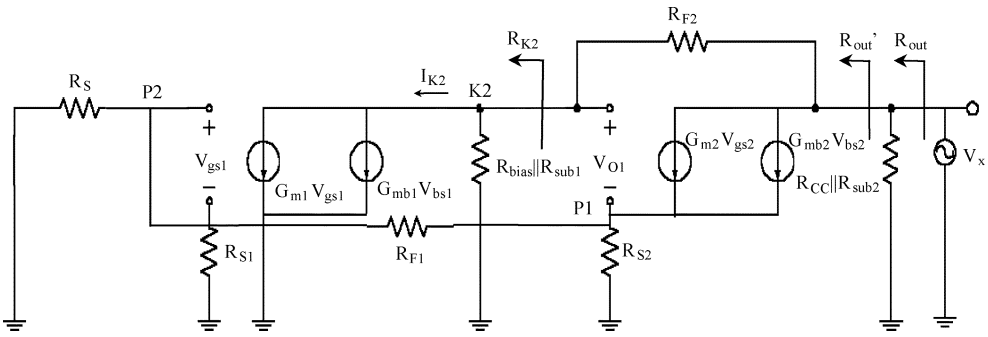


Fig. 7. Small-signal equivalent circuit for calculating output resistance at dc frequency.

$-R_S$ and $-R_L$, respectively, in the expression of poles [13]. Therefore, S_{11} and S_{22} can be expressed as follows:

$$S_{11} = \frac{Z_{\text{in}} - R_S}{Z_{\text{in}} + R_S} = \frac{R_{\text{in}} - R_S}{R_{\text{in}} + R_S} \cdot \frac{\left(1 + \frac{s}{\omega_{Z1}}\right) \cdot \left(1 + \frac{s}{\omega_{Z2}}\right)}{\left(1 + \frac{s}{\omega_{pn1}}\right) \cdot \left(1 + \frac{s}{\omega_{pn2}}\right)} \quad (24b)$$

$$S_{22} = \frac{Z_{\text{out}} - R_L}{Z_{\text{out}} + R_L} = \frac{R_{\text{out}} - R_L}{R_{\text{out}} + R_L} \cdot \frac{\left(1 + \frac{s}{\omega_{Z3}}\right) \cdot \left(1 + \frac{s}{\omega_{Z4}}\right)}{\left(1 + \frac{s}{\omega_{pn1}}\right) \cdot \left(1 + \frac{s}{\omega_{pn2}}\right)}. \quad (24c)$$

S_{12} is the reverse voltage gain, which can be found easily once R_{out} is known as follows:

$$S_{12} = 2\left\{\left[G'_{m1}\left(R_{F2} + \left(\frac{R_S + R_{F1}}{G'_{m1}G'_{m2}R_{S2}R_S} \| (R_{\text{bias}} \| R_{\text{sub1}})\right)\right)\right] \cdot \left(1 + \frac{R_L}{R_{CC} \| R_{sub2}}\right) + R_L \frac{R_S + R_{F1}}{R_{S2}R_S} + G'_{m1}R_L\right\}^{-1} \cdot \frac{\left(1 + \frac{s}{\omega_{Z5}}\right)}{\left(1 + \frac{s}{\omega_{pn1}}\right) \cdot \left(1 + \frac{s}{\omega_{pn2}}\right)} \quad (24d)$$

where $\omega_{Z5} = 1/(C_{g1}R_{S1})$ is the zero caused by C_{g1} and R_{S1}.

B. Experimental Results and Discussions

The circuit parameters of the designed CMOS broad-band amplifier are indicated in Fig. 5. This circuit was fabricated with a 0.25-μm CMOS process, and the size of M1 and M2 was both 0.24 μm$\times$320 μm. The total power dissipation was only 25 mW. The values of the resistors were as follows: $R_{\text{bias}} = 350\ \Omega$, $R_{CC} = 150\ \Omega$, $R_{F1} = 80\ \Omega$, $R_{F2} = 650\ \Omega$, and $R_{S2} = 14.5\ \Omega$. The capacitance C_{S2} was 7 pF. The die photograph of the finished circuit is shown in Fig. 8. Note that the circuit only occupied a small area of 600 μm $\times$ 700 μm because no inductor was used, which is an advantage of the resistive feedback amplifier.

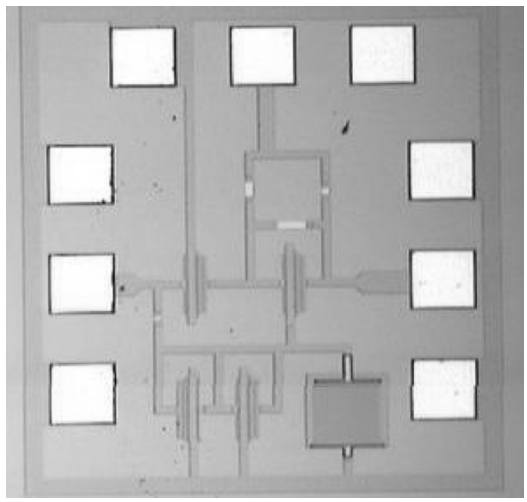


Fig. 8. Die photograph of the dual-feedback broad-band amplifier fabricated with a 0.25-μm CMOS technology. The chip size is $600\ \mu\text{m} \times 700\ \mu\text{m}$.

An HP8510 network analyzer in conjunction with the Cascade probe station was used to measure the characteristics of this broad-band amplifier. In addition, Advanced Design System (ADS) of Agilent technologies was used to generate the simulation results. The simulated, measured, and predicted results of $|S_{11}|$, $|S_{22}|$, and $|S_{21}|$ are shown in Fig. 9(a), 9(b), and 10, respectively. Clearly, the calculated S-parameters are all in good agreement with the simulated results, which verifies the validity of our proposed theory.

As can be seen, in Fig. 9(a) and (b), the measured in-band return losses $|S_{11}|$ and $|S_{22}|$ were smaller than -10 dB. The simulated results are in good agreement with the measured values. In Fig. 10, the measured $|S_{21}|$ exhibited a flat response with a 3-dB bandwidth of 1.7 GHz. The predicted $|S_{21}|$ at low frequencies with the method we propose was 12.8 dB, which was in good agreement with the simulated $|S_{21}|$ (12.3 dB). The measured result was about 2 dB lower than what had been predicted and simulated. In addition, the predicted bandwidth was 2.1 GHz, comparable to the simulated result of 2.0 GHz but higher than the measured result of 1.7 GHz. Because the foundry guarantees the CMOS SPICE models with error rates within a 10% range, the discrepancies between the measured results and the simulated and calculated results should mainly result from the SPICE modeling errors. In particular, the parasitic silicon substrate effect was not fully included in the SPICE model of the CMOS process that we used.

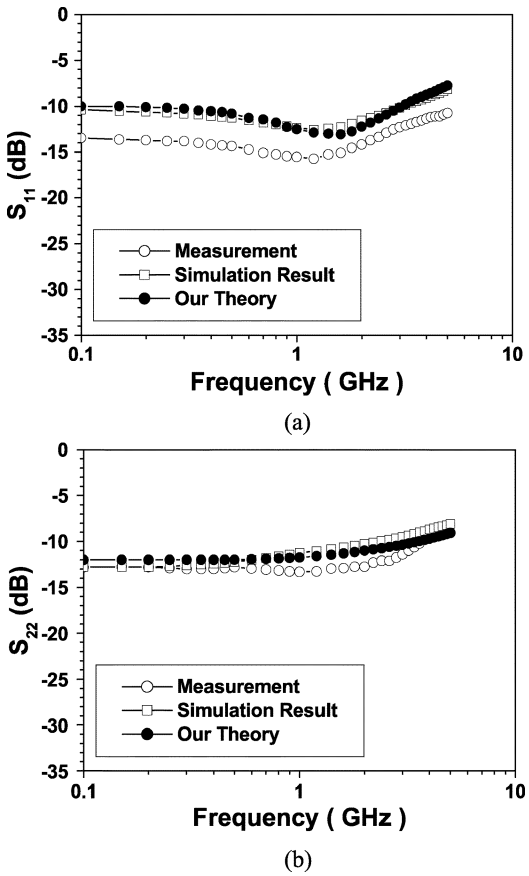


Fig. 9. Simulated, measured, and predicted results of (a) $|S_{11}|$ and (b) $|S_{22}|$ of the CMOS broad-band amplifier.

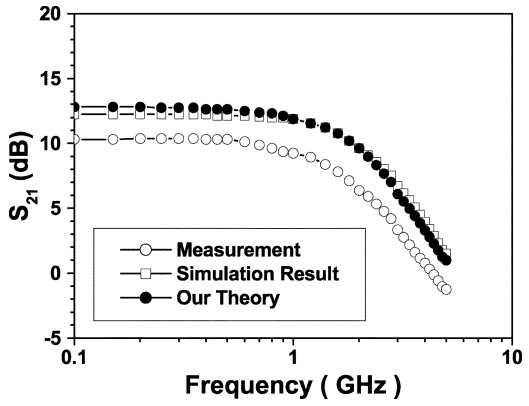


Fig. 10. Simulated, measured, and predicted results of S_{21} of the CMOS broad-band amplifier.

V. Conclusion

The methodology for the calculation of S-parameters from the denominator or poles of the voltage-gain transfer function is presented. First, S_{11} can be obtained by replacing R_S with $-R_S$ in the expression of the denominator or poles of the voltage-gain transfer function while S_{22} can be obtained by replacing R_L with $-R_L$. Second, the input impedance can be obtained by isolating R_S from the other terms in the expression of the denominator while the output impedance can be obtained by isolating R_L from the other terms. Third, S_{12} can be determined by finding the zeros and dc (or mid-band) gain of the "reverse circuit." Our theory has been applied to three circuits and the results of S-parameters and input/output impedance derived from our method are the same as those obtained from direct calculations. In addition, a broad-band amplifier with dual feedback loops fabricated with a 0.25-μm CMOS process was used to verify the proposed theory. The experimental results are consistent with those predicted from the analytic expressions of S-parameters determined from the poles of the voltage-gain transfer function. These results show that our proposed method is very applicable to RF IC design.

Acknowledgment

The authors would like to thank the chip implementation center (CIC) for chip fabrication and the nanometer device laboratory (NDL) for high-frequency measurements.

References

[1] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 4th ed. New York: Oxford Univ. Press, 1998, p. 601.
[2] A. B. Carlson, *Circuits*. Pacific Grove, CA: Brooks/Cole, 2000, pp. 162–169.
[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001, p. 166–195, 246-285.
[4] G. Gonzalez, *Microwave Transistors and Amplifiers Analysis and Design*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1984, p. 34.
[5] ——, *Microwave Transistors and Amplifiers Analysis and Design*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1984, p. 62.
[6] R. Goyal, "S-parameter output from the SPICE program," *IEEE Circuits Devices Mag.*, vol. 4, no. 2, pp. 28–29, Mar. 1988.
[7] R. G. Meyer and R. A. Blauschild, "A 4-terminal wide-band monolithic amplifier," *IEEE J. Solid-State Circuits*, vol. SC-16, no. 6, pp. 634–638, Dec. 1981.
[8] I. Kipnis *et al.*, "Silicon bipolar fixed and variable gain amplifier MMICs for microwave and lightwave applications up to 6 GHz," in *Microw. Symp. Dig., IEEE MTT-S Int.*, vol. 1, June 1989, pp. 109–112.
[9] K. W. Kobayashi and A. K. Oki, "A DC-10 GHz high gain-low noise GaAs HBT direct-coupled amplifier," *IEEE Microw. Guided Wave Lett.*, vol. 5, no. , pp. 308–310, Sep. 1995.
[10] K. W. Kobayashi *et al.*, "Low dc power high gain-bandwidth product InAlAs/InGaAs-InP HBT direct-coupled amplifiers," in *Proc. IEEE GaAs IC Symp.*, Nov. 1996, pp. 141–144.
[11] C. D. Hull and G. B. Meyer, "Principle of monolithic wideband feedback amplifier design," *Int. J. High Speed Electron.*, vol. 3, pp. 53–93, Feb. 1992.
[12] M. C. Chiang *et al.*, "Analysis, design, and optimization of InGaP-GaAs HBT matched-impedance wide-band amplifiers with multiple feedback loops," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 694–701, Jun. 2002.
[13] S. S. Lu *et al.*, "A novel interpretation of transistor S-parameters by poles and zeros for RF IC circuit design," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 2, pp. 406–409, Feb. 2001.
[14] F. T. Chien and Y. J. Chan, "Bandwidth enhancement of transimpedance amplifier by capacitive-peaking design," *IEEE J. Solid-State Circuits*, vol. 34, no. 8, pp. 1167–1170, Aug. 1999.

Shey-Shi Lu (S'89–M'9l–SM'99) was born in Taipei, Taiwan, R.O.C., on October 12, 1962. He received the B.S. degree from National Taiwan University, Taipei, in 1985, the M.S. degree from Cornell University, Ithaca, NY, in 1988, and the Ph.D. degree from the University of Minnesota at Minneapolis-St Paul in 1991, all in electrical engineering. His M.S. thesis was related to the planar doped barrier hot-electron transistor, while his doctoral dissertation concerned the uniaxial stress effect on the AlGaAs–GaAs quantum-well/barrier structures.

In August 1991, he joined the Department of Electrical Engineering, National Taiwan University, where he is currently a Professor. His current research interests are in the areas of RF integrated circuit/monolithic microwave integrated circuits and micromachined RF components.

Yo-Sheng Lin (M'02) was born in Puli, Taiwan, R.O.C., on October 10, 1969. He received the Ph.D. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1997. His Ph.D. dissertation was on the fabrication and study of GaInP–InGaAs/GaAs doped-channel field-effect transistors and their applications to monolithic microwave integrated circuits (MMICs).

He joined Taiwan Semiconductor Manufacturing Company (TSMC) in 1997 as a Principle Engineer for 0.35/0.32 DRAM and 0.25 embedded DRAM technology developments in the Integration Department of Fab-IV. Since 2000, he has been responsible for 0.18/0.15/0.13—μm CMOS low-power device technology development in the Department of Device Technology and Modeling, R&D. He was promoted to Technical Manager in 2001. In August 2001, he joined the Department of Electrical Engineering, National Chi-Nan University, Puli, Taiwan, where he is currently an Associate Professor. His current research interests are in the areas of characterization and modeling of radio frequency (RF) active and passive devices, and RF integrated circuits/MMICs.

Hung-Wei Chiu was born in Taipei, Taiwan, R.O.C., in 1976. He received the B.S. degree from National Chiao-Tung University, HsinChu, Taiwan, R.O.C., in 1998, and the M.S. and Ph.D. degrees from National Taiwan University, Taipei, in 2000 and 2003, respectively, all in electrical engineering.

In 2004, he joined the Taiwan Semiconductor Manufacturing Company, HsinChu, as a Designer with the Mixed-Mode and RF Library Division. Since then he has worked in the area of the automation of mixed-mode and RF circuit design.

Yu-Chang Chen was born in Taipei, Taiwan, R.O.C., on February 19, 1978. He received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, in 2000 and 2002, respectively.

In 2002, he joined Airoha Technology, Taipei, as a Designer with the Mixed-Mode Division. His current research interests include mixed-signal IC design and architectures for wireless communication.

Chin-Chun Meng (M'92) received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C. in 1985, and the Ph.D. degree from the University of California, Los Angeles, in 1992, both in electrical engineering. He demonstrated the first CW operation of multiquantum well IMPATT oscillator at 100 GHz in his Ph.D. work.

After completing his Ph.D., he joined the Hewlett Packard Component Group, Santa Clara, CA, in 1993 as a Member of Technical Staff. His area of research and development included HBT, MESFET, and PHEMT for microwave and RF power-amplifier application. He is now an Associate Professor with the Department of Communications Engineering at National Chiao-Tung University, HsinChu, Taiwan. His current research interests are in the areas of RF integrated circuits, high-frequency circuits, and high speed devices.