Analysis of the Scaling Effect on NAND Flash Memory Cell Operation

R. Shirota, and H. Watanabe

Department of Electrical and Computer Engineering, National Chiao Tung University, 1001Ta Hsueh Road, Hsinchu, 30010, Taiwan

In recent years, the enormous success of NAND Flash memory technology in realizing multi-gigabyte memory chips has evidently triggered a lot of difficulties concerning its cell operation, such as parasitic neighbouring cell coupling, FN-tunnelling statistics, Vt distribution widening by RTN, et al. In this paper, two kinds of phenomena are shown. One is the increase of the interface state density after write/erase cycles, which will degrades the sub-threshold swing (SS) of the memory cell in the NAND string. The other is the increase of the programmed Vt distribution after programming, which also reduces the cell operation margin. It is revealed that Vt distribution widening closely depends on the floating gate doping concentration of Phosphorus. These phenomena become more serious as cell size smaller.

Introduction

Generally, NAND cell scaling degrades the cell reliability (1, 2) and reduces the program operation margin (3). These degradations are likely limit the scaling of NAND Flash memory. It has been known that oxide degradation by program/erase cycling comes from high electric field in the gate oxide (more than 10MV/cm), which damage the oxide interface and also generate the hole injection into oxide. Thus, after repeating program/erase cycling, programmed and erased Vt shift occurs and subthreshold swing increases. In this paper, the detail analysis is done by concerning the interface trap density after program/erase cycling. The subthreshold swing degradation well corresponds to the increase of the interface trap density. Next, the programmed Vt distribution widening is discussed related to the floating gate (FG) phosphorus doping. It is shown that lower FG doping brings deep depletion area and wider band bending in FG during programming. As the programming time is prolonged, band bending value reduces due to the hole generation in the FG. Combined with FN-tunneling current statistics, time dependence of FG band bending causes the wide Vt distribution. The cell Vt distribution widening becomes more serious as cell size scaling.

Analysis of interface density of states depends on W/E endurance cycles

We analyze the degradation of floating-gate type NAND cells by examining the generation of the interface with the aid of charge pumping method. 8KB NAND string cell array with 70, 50 and 40nm ground rule are used to investigate the effect of program/erase cycling stress. As the size of devices shrinks, the shift of the erased threshold voltage and relevant sub-threshold swing (SS) become more severe. Through

the charge pumping measurement, we study the trend of the cycling dependence of the interface and their energy distributions in depth.

In this work, NAND Flash memory array is applied the write and erase cycling, and followed by a charge pumping measurement to investigate the behavior of the interface state. During charge pumping measurement, only one word line connected to source side cells is applied charge-pumping AC pulse and other word lines are programmed and cut off, as shown in Fig. 1. The charge pumping current of the source side cells are measured at the fixed erase states. Also, by extracting the charge pumping current with variety of rise-time and fall-time of the control gate pulse (4, 5), the energy level distribution of the interface state into depth are analyzed.

Result and discussion of interface density of states

Figure 2 demonstrates the stability of threshold voltage and their cycled dependence with various device sizes, which are 70nm, 50nm, and 40nm channel-length NAND Flash memory arrays. From the figure, there is slight difference between devices of channel length with 70nm and 50nm long. However, the cell with 40nm channel length possesses the huge erased threshold shift after 100k cycling times. The larger Vt shift may be caused by the generation of interface state and bulk trap within the tunnel oxide. Fig. 3 shows the sub-threshold swing (S.S) as a function of W/E cycles. All of S.S of 70, 50, 40nm rule devices increase after W/E cycling. However, degradation rate is getting more serious as cell size scaling from 70 to 50nm, 50nm to 40nm, gradually. Especially, S.S of 40nm case shows serious increase same as that of erased Vt shift by W/E cycling.

In order to study the relation between the degradation S.S and interface state, interstate density is measured depend on W/E cycles between 70 and 50nm devices. Fig. 4 shows the density of the interface state which contribute to the charge pumping current. We can see three important characteristics. One is, the interface state increases monotonically as W/E cycling. Second is, the ratio of interface state increase by W/E cycling is larger in the case of 50nm device as compared with that of 70nm devices. The third is, the increases of S.S by W/E cycling have strong correlations with the increases of interface states in both devices of 70nm and 50nm.

Fig.5 and 6 show the energy distribution of the interface state relevant to W/E cycles by altering the value of rising and falling time of charge pumping pulse. The energy distribution can be extracted as;

$$dQ_{it}/dt_f = qA_G D_{it}(E_{it})dE_{it}/dt_f \qquad [1]$$

, where A_G is the effective gate area and t_f is the fall time. The magnitude of the interface state above the intrinsic level increases after numbers of cycling, which is more apparent than the case below intrinsic level. That implies the electron traps in the interface states between intrinsic level and conduction band should be responsible for the degradation of sub-threshold swing. The phenomena are more obvious in 50nm devices as compared with the case of 70nm device. These results are consistent with the measured data of sub-threshold swing. The reason of larger interface increase by W/E cycling at the smaller cell size is not clear. However, it is supposed to be related to the active channel area edge effect. When the channel width becomes smaller, relatively channel edge portion increases.
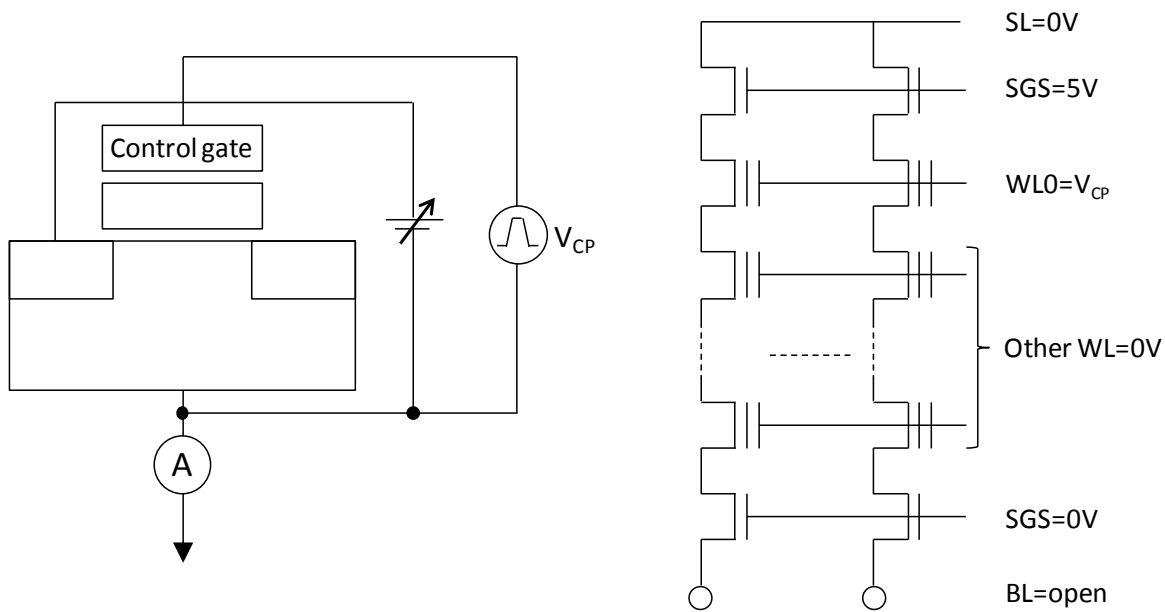
Fig.1. Schematic of charge pumping measurement using NAND Flash memory cell array.
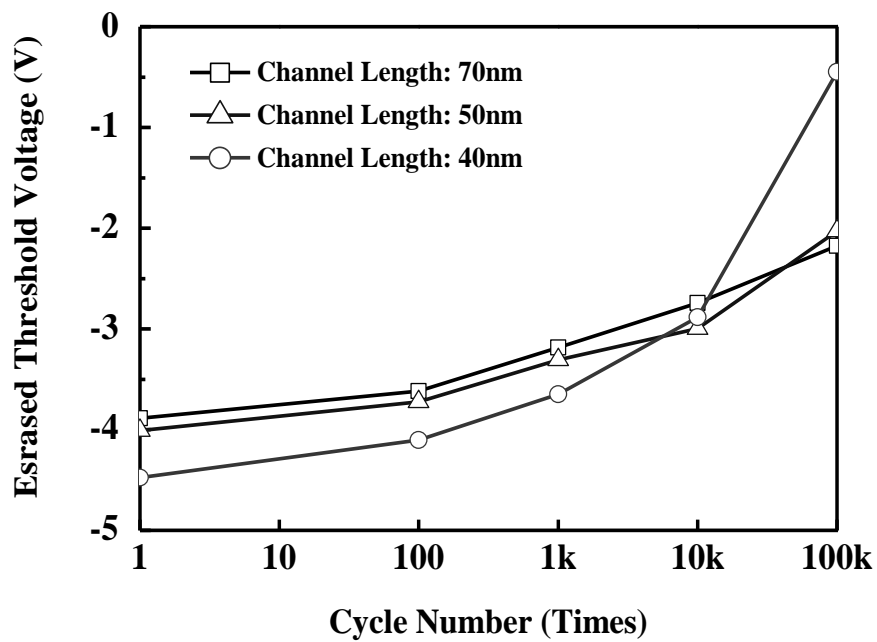
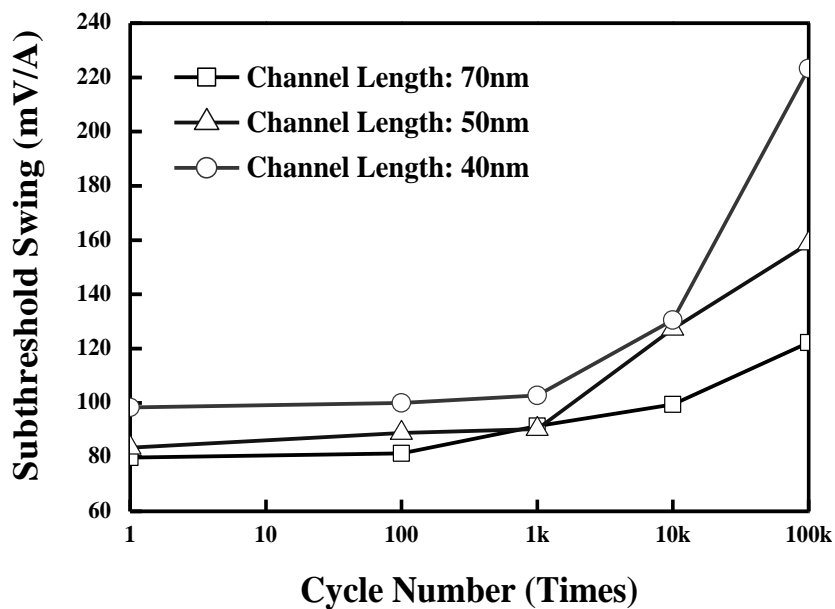Fig.2. The shift of erased threshold voltage and relevant cycling dependence.

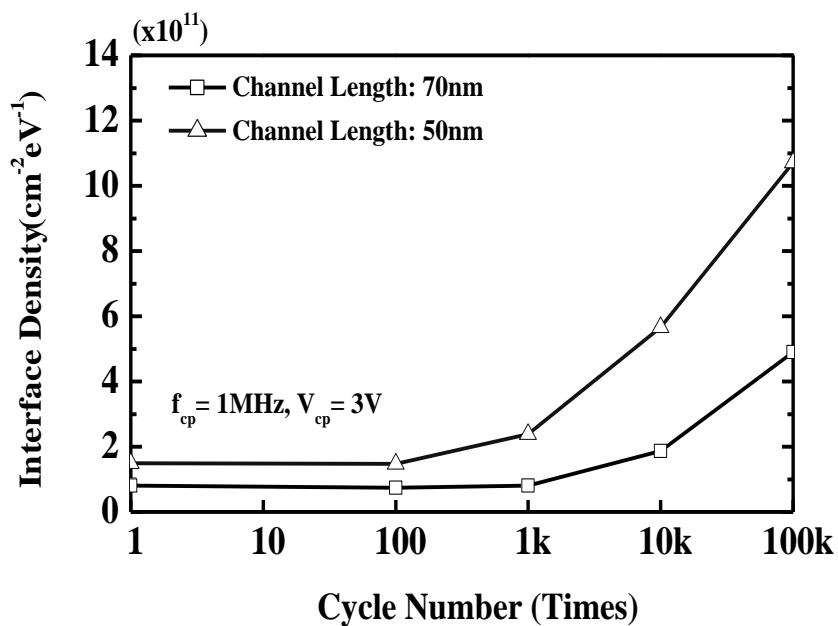Fig.3. Cycling dependence of sub-threshold swing in various size of devices

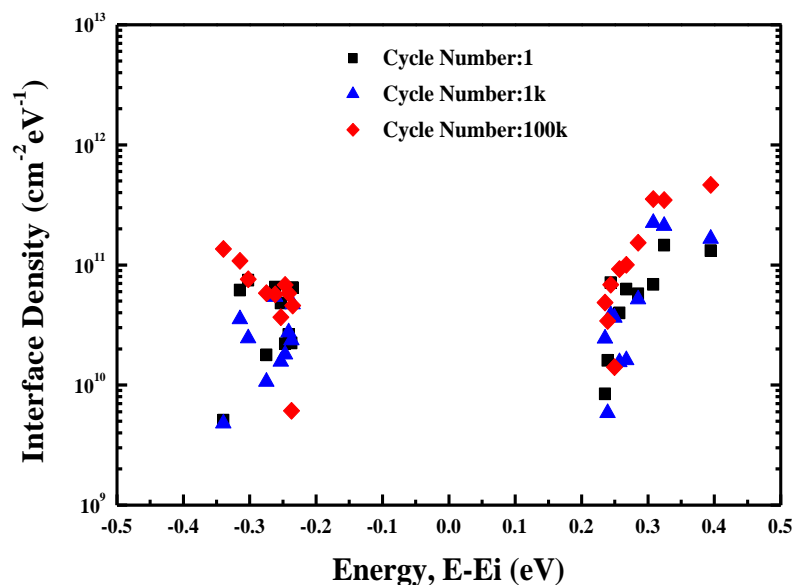Fig.4. Cycling dependence of interface density with various size of devices.

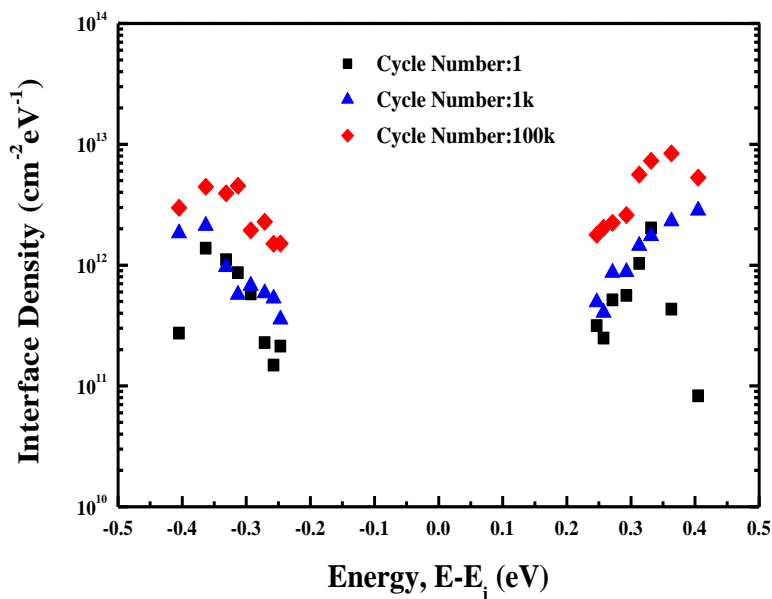Fig.5. Cycling dependence of energy distribution of interface with 70nm NAND cells

Fig. 6. Cycling dependence of energy distribution of interface with 50nm NAND cells

Analysis of Vt distribution depends on FG impurity doping in NAND Flash

In NAND Flash memory, FN−tunneling mechanism has been used for programming and erasing operation (6). In order to secure the tight threshold voltage (Vt) distribution for programming, step up program scheme is commonly used to serve a constant FN−current per each step, shown in Fig.7 (7). Due to the low probability of electron tunneling, the FN−tunneling probability is considered to follow sub-Poisson statistics (3).

The effect of electron tunneling current fluctuation is becoming serious as cell size scaling due to the reduction of the capacitance between the control gate (CG) to the floating gate (FG).

The effect of the activated FG impurity concentration on the programmed Vt distribution is newly investigated and analyzed (8). The lower FG impurity concentration leads to a wider Vt distribution, which is explained by the time dependent tunnel oxide electric field enhancement effect induced by the reduction of depletion region in FG as the programming time is lengthened. Initially, FG is deeply depleted at the interface of the tunnel oxide, shown in Fig.8-1. However, as the programming time is prolonged, electrons by FN tunneling in FG generate electron−hole pairs and generated holes are gathered at the interface of the tunnel oxide, which reduces the depletion region and enhance the oxide electric filed, shown in Fig.8-2. The enhancement effect of the electric field for the tunnel oxide is coupled to the FN−tunneling statistics and enlarges the distribution of programmed Vt. This effect is more clearly observed at the lower FG impurity concentration, which gives the limitation of the minimum impurity concentration in FG. Monte−Carlo simulation considering both the tunnel oxide electric field enhancement effect and FN−tunneling statistics were carried out and showed good agreement with the experiments, shown in Fig.9. Fig. 10 shows this Vt distribution widening effect becomes more serious as cell size scaling, due to the reduction of the capacitance between FG to CG. These results suggest that FG doping need to be optimized carefully, as cell size scaling.
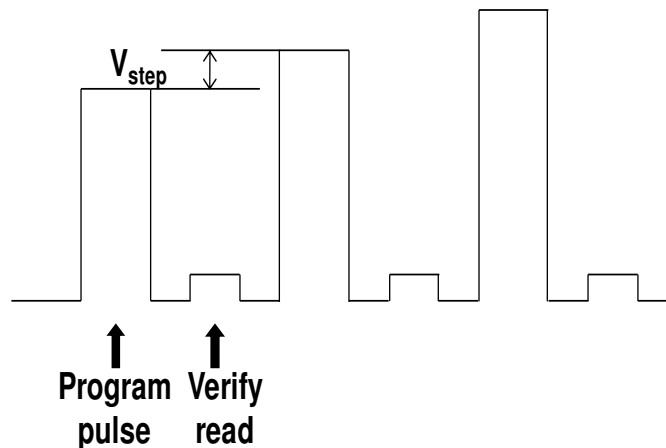

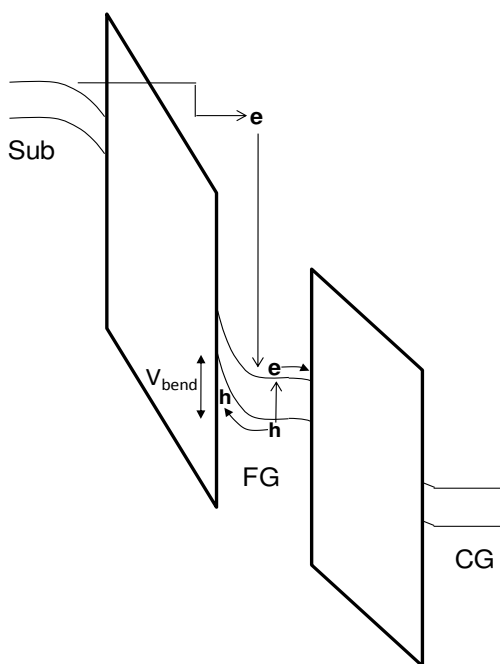Fig.7. NAND Flash program sequence with increment step up pulse
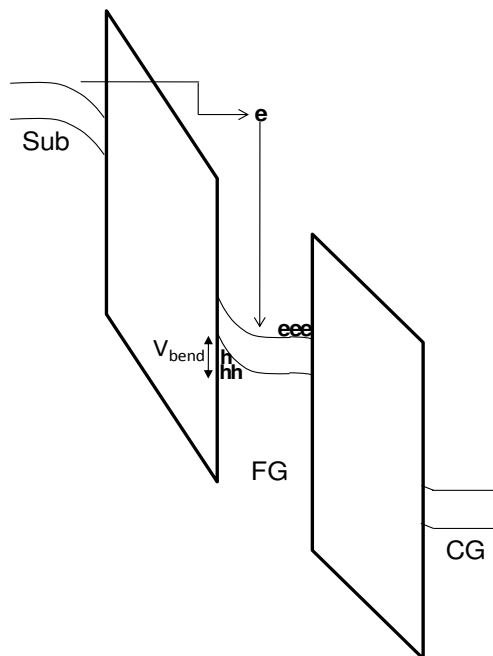
Fig.8-1. Band at the beginning of Program.　　Fig.8-2. After program time passed.
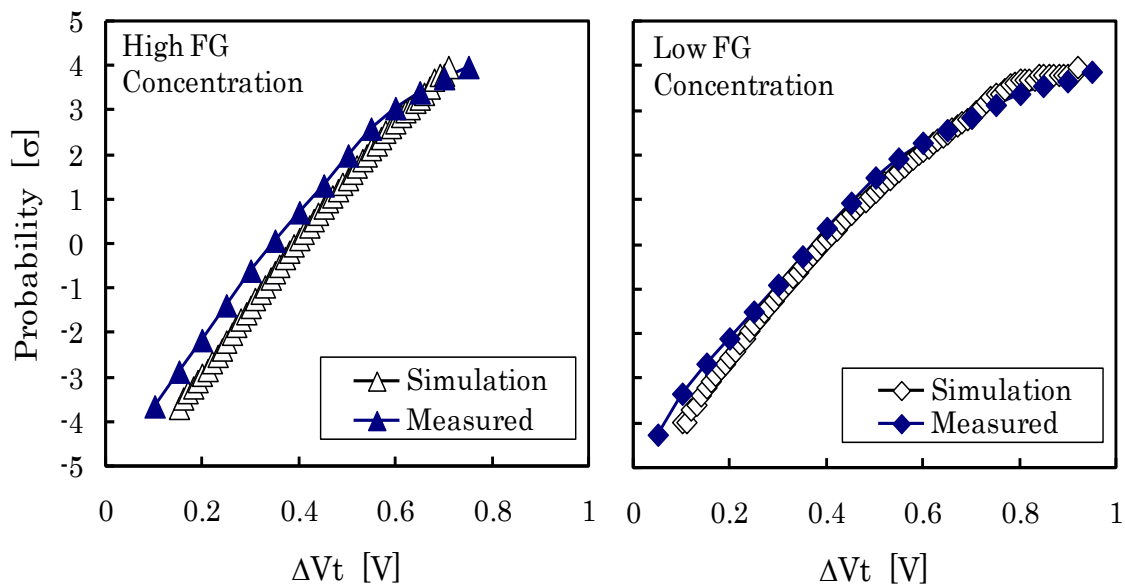

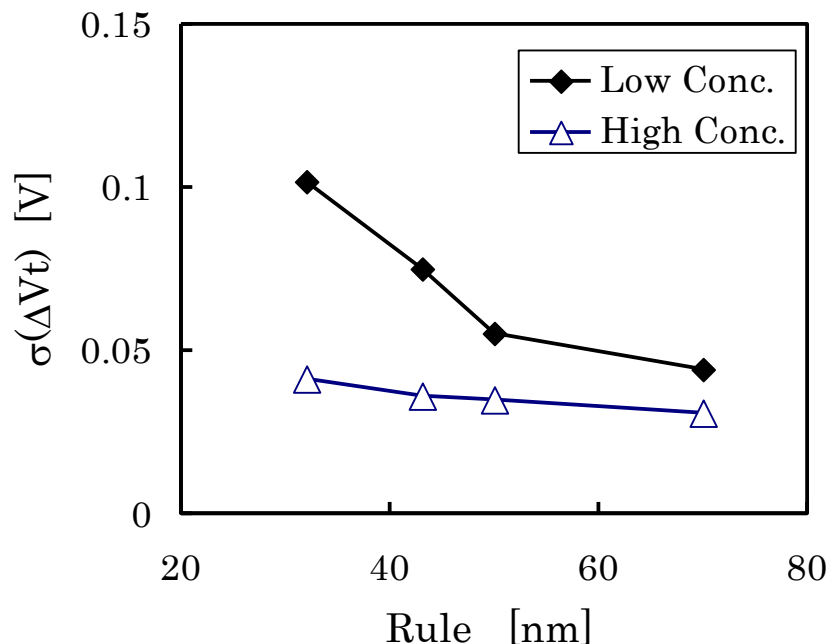Fig.9. Measured and simulated Vt distribution (high & low FG doping)

Fig.10. Cell scaling effect of the dispersion of Vt distribution

Conclusion

As cell size scaling, cell reliability degraded and also program operation margin decreases. Concerning to the reliability issues, the interface trap states increases by program/erase cycling. The increase of the interface trap states is enhanced more seriously, as cell size scaling. It is supposed that this phenomenon will be closely related to the degradation of the oxide quality at the edge of the active area. Regarding to the programmed cell Vt distribution, band width becomes widen as FG doping is lower. This distribution widening is also enhanced as cell size scaling.

Acknowledgments

References

1. J-T. Liang, C-H. Shih, W. Chang, Y-X. Luo, M-K. Huang, N-D. Chien, W-F. Wu, S-M. Wu, C. Lien, R. Shirota, C-T. Huang, S. Lu, and A. Wang, IEEE Trans. Electron Devices, **58**, 1257 (2011).
2. A. S. Spinelli, C. M. Compagnoni and D. Ielmini, European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, tutorial (2010).

3. C. M. Compagnoni, A. S. Spinelli, R. Gusmeroli, S. Beltrami, A. Ghetti, and A. Visconti, IEEE Trans. Electron Devices, **55**, 2695 (2008).
4. G. Groeseneken, H. E. Maes, N**.** Beltran and R. F. Keersmaecker, IEEE Trans. Electron Devices**, 31**, 42 (1984).
5. P. Heremans, J. Witters, G. Groeseneken and H. E. Maes, IEEE Trans. Electron Devices**, 35**, 1318 (1989).
6. R. Kirisawa, S. Aritome, R. Nakayama, T. Endoh, R. Shirota and F. Masuoka, VLSI sympo. Tech, Dig, 129 (1990).
7. G. J. Hemink, T. Tanaka, T. Endoh, S. Aritome and R. Shirota, VLSI sympo. Tech, Dig, 129 (1995).
8. R. Shirota, Y. Sakamoto, H−M. Hsueh, J−M. Jaw, W−C. Chao, C−M. Chao, S−F.Yang and H. Arakawa, IEEE Trans. Electron Devices, **58**, 3172 (2011).