ESD Protection Design for Mixed-Voltage I/O Buffer With Substrate-Triggered Circuit

Ming-Dou Ker, *Senior Member, IEEE,* and Hsin-Chyh Hsu, *Student Member, IEEE*

***Abstract*—A substrate-triggered technique is proposed to improve the electrostatic discharge (ESD) robustness of a stacked-nMOS device in the mixed-voltage I/O circuit. The substrate-triggered technique can further lower the trigger voltage of a stacked-nMOS device to ensure effective ESD protection for mixed-voltage I/O circuits. The proposed ESD protection circuit with substrate- triggered design for a 2.5-V/3.3-V-tolerant mixed-voltage I/O circuit has been fabricated and verified in a 0.25-μm salicided CMOS process. The substrate-triggered circuit for a mixed-voltage I/O buffer to meet the desired circuit application in different CMOS processes can be easily adjusted by using HSPICE simulation. Experimental results have confirmed that the human- body-model (HBM) ESD robustness of a mixed-voltage I/O circuit can be increased $\sim$60% by this substrate-triggered design.**

***Index Terms*—Electrostatic discharge (ESD), stacked nMOS, substrate-triggered technique, mixed-voltage I/O.**

I. Introduction

With the process evolutions, gate oxide thickness has been scaled down to improve circuit operating speed and performance. The power supply voltages in CMOS ICs have also been scaled downwards to follow the constant-field scaling requirement and to reduce power consumption. Thus, most computer architectures require the interfacing of semiconductor chips or subsystems with different internal power supply voltages.

In the mixed-voltage I/O interface of an IC with a single power supply, only a low VDD power supply is provided for internal circuits. Therefore, the I/O circuits are designed to be tolerant of, and protected from, high-voltage input signals. Typically, a chip, that operates with I/O signals ranging from 0 to 3.3 V, may have an internal supply voltage of only 2.5 or 1.8 V. The chip-to-chip interface I/O circuits must be designed to avoid electrical overstress on the gate oxide [1] and to prevent undesirable current leakage paths between the chips [2], [3]. The ESD protection circuit also has to meet these constraints for providing robust ESD protection in such a mixed-voltage application.

In advanced deep-submicron CMOS technology, some fabrication processes provide both high- and low-voltage transistors to overcome this issue [4], [5]. In such processes, the high-voltage transistors which have thicker gate oxides can be used for the protection circuits with reliability consideration, and the low-voltage transistors with thinner gate oxides used for the internal circuits for high-speed and high-performance consideration. However, some processes with only a single gate-oxide thickness do not provide this capability. Thus, the ESD protection circuit for such a mixed-voltage I/O interface must be designed by only using the thin-oxide MOS devices, which have the same oxide thickness as those used in the interior of the chip.

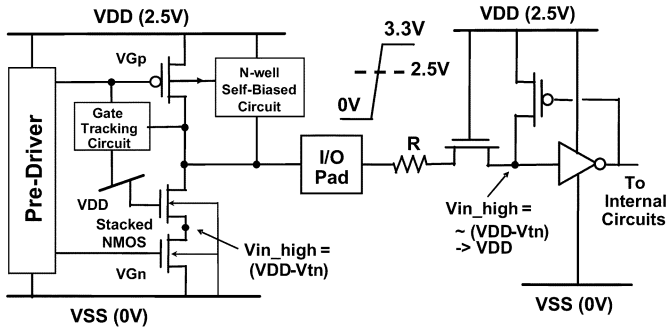

Fig. 1. Typical mixed-voltage I/O circuit with the stacked nMOS and the self-biased-well pMOS to avoid the leakage current path and the gate oxide reliability issue.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process (called dual gate oxide in some CMOS processes), the stacked-nMOS structure had been widely used in the mixed-voltage I/O buffer [6]–[11]. The typical 2.5-V/3.3-V-tolerant mixed-voltage I/O circuit is shown in Fig. 1. The pull-up pMOS, connected from the I/O pad to the VDD power line, has the gate tracking circuits for tracking the gate voltage and the n-well self-biased circuits for tracking the n-well voltage, which are designed to ensure that the pull-up pMOS does not conduct current when the 3.3-V input signals enter the I/O pad.

ESD stresses on an I/O pad have four basic pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode), ESD stress conditions [12]–[15]. To have a sufficiently high ESD robustness of the CMOS output buffer, the CMOS buffer is generally drawn with larger device dimensions and a wider spacing from the drain contact to the poly gate, which often occupies a larger layout area in the I/O cell. Without increasing device dimensions in the I/O cells, the VDD-to-VSS ESD clamp circuits across the power lines of CMOS ICs had been used to successfully improve the ESD robustness of CMOS I/O buffers [16], [17]. The ESD current paths along the traditional CMOS output buffer under the positive-to-VSS ESD stress condition is illustrated by the dashed

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The authors are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: mdker@ieee.org; m8911550@alab.ee.nctu.edu.tw).

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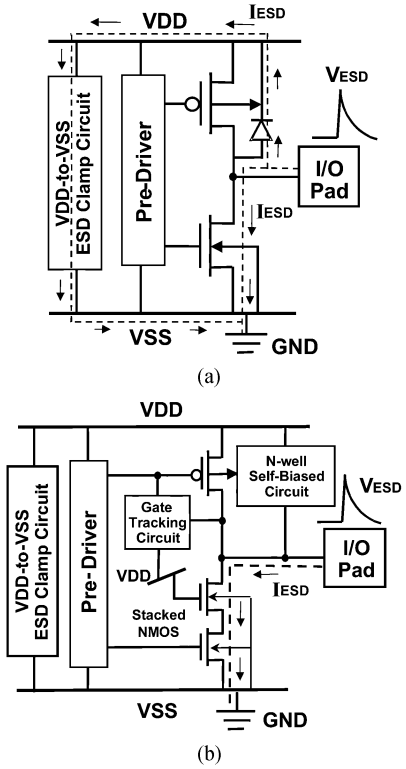


Fig. 2. The ESD current paths along (a) the traditional CMOS output buffer and (b) the mixed-voltage output buffer, under the positive-to-V_{SS} ESD stress condition.

lines in Fig. 2(a), where almost all ESD current is discharged through the parasitic diode of the pMOS and the VDD-to-VSS ESD camp circuit to ground. Therefore, the traditional CMOS output buffer can sustain a higher ESD stress. However, due to the leakage current issue in the mixed-voltage I/O buffer, there is not any parasitic diode connected from the I/O pad to VDD power line. Because of the limitation of placing a diode from the pad to VDD in the mixed-voltage I/O circuits, the positive-to-VSS ESD voltage zapping on the I/O pad cannot be diverted from the pad to VDD power line and cannot be discharged through the additional power-rail (VDD-to-VSS) ESD clamp circuit. Such positive-to-VSS ESD current on the I/O pad is totally discharged through the stacked-nMOS in the snapback breakdown condition. The ESD current, under this positive-to-VSS ESD stress condition, along the mixed-voltage output buffer is shown by the dashed line in Fig. 2(b). Besides, the nMOS in a stacked configuration has a higher trigger voltage (Vt1), a higher snapback holding voltage (Vsb), and a lower secondary breakdown current (It2) as compared to the single nMOS. Therefore, such mixed-voltage I/O circuits with stacked nMOS often have much lower ESD level, as compared to the I/O circuits with a single nMOS [18], [19]. Thus, the mixed-voltage I/O circuit often has the worst ESD level (often $<$2 kV in the human-body-model (HBM) ESD test) under the positive-to-VSS ESD stress condition. Without the parasitic diode connected from the I/O pad to VDD power line, the mixed-voltage I/O circuit also has a lower ESD level under the positive-to-VDD ESD stress condition. Therefore, ESD protection design on the mixed-voltage I/O circuits is mainly focused to improve the ESD level under the positive ESD stress conditions.

Although stacked-nMOS devices solve the gate-oxide reliability issue in the mixed-voltage I/O buffer circuits, unfortunately, the high holding voltage characteristic of stacked-nMOS devices causes degradation of its ESD robustness. The substrate-triggered technique, realized by special circuit design, is therefore applied to improve ESD robustness of a stacked nMOS in the mixed-voltage I/O buffer. Recently, a low-leakage diode-string circuit has been reported to implement the special substrate-triggered design to improve ESD robustness of a mixed-voltage I/O circuit in a 0.25-μm CMOS process [20]. In this paper, a new substrate-triggered design is proposed to reduce trigger voltage and holding voltage of a lateral n-p-n bipolar junction transistor (BJT) in the stacked-nMOS device, and therefore to enhance ESD robustness of mixed-voltage I/O circuits. Moreover, an nMOS device with a higher local substrate potential had been confirmed to provide better ESD robustness [21]–[23]. The new proposed ESD protection circuit, which combines the stacked-nMOS device with a substrate-triggered circuit for general mixed-voltage I/O circuits without causing the gate-oxide reliability problem, is fully process-compatible with the general subquarter-micron CMOS processes. Without using the thick gate oxide, but with better ESD robustness, the proposed ESD protection design for a 2.5-V/3.3-V-tolerant mixed-voltage I/O buffer has been successfully verified in a 0.25-μm CMOS process [24].

II. Stacked nMOS With Substrate-Triggered Design

A. Stacked nMOS Device

Fig. 3(a) and (b) shows the finger-type layout pattern and the corresponding cross-sectional view of the stacked-nMOS structure for a mixed-voltage I/O circuit, which includes one pair of nMOS transistors connected in a stack configuration. The stacked-nMOS device is often used as both of the pull-down stage and the ESD protection device for the I/O circuit. This nMOS transistor pair includes a first transistor Ms1 (top nMOS transistor), having a drain connected to an I/O pad, and a gate (Vg1) connected to the VDD power supply. A second nMOS transistor Ms2 (bottom nMOS transistor) of the nMOS transistor pair is merged into the same active area of the first transistor, having a gate (Vg2) connected to the predriver of the mixed-voltage I/O circuit. The drain of the bottom nMOS and the source of the top nMOS are constructed together by sharing the common n+ diffusion region.

The voltage (Vg1) of the top nMOS is biased at the low VDD voltage (e.g., 2.5 V in a 2.5-V/3.3-V interface). The voltage (Vg2) of the bottom nMOS is biased at VSS provided by the predriver to avoid leakage current through the stacked-nMOS structure, when the I/O circuit has a high-voltage input signal. With a high-voltage input signal at the pad (e.g., 3.3 V in a 2.5-V/3.3-V interface), the shared common diffusion region has approximately a voltage level of VDD–V_{th} ($\sim$2.7 V). The V_{th} ($\sim$0.6 V) is the threshold voltage of the nMOS device. Therefore, the stacked nMOS can be operated within the safe range for both dielectric and hot carrier reliability limitations.

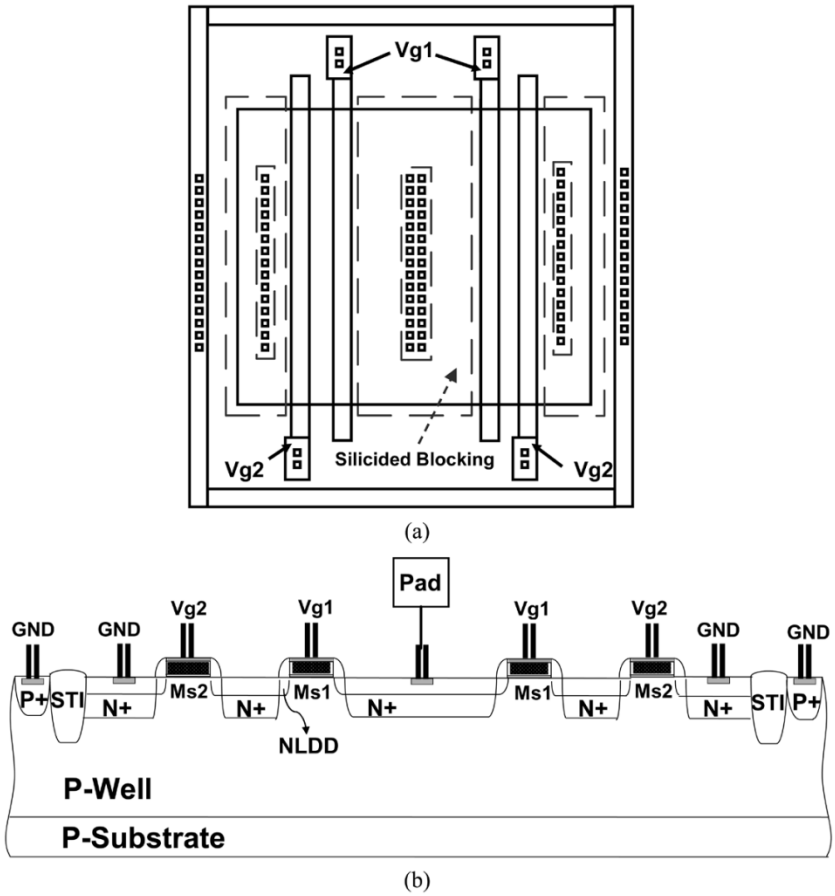


Fig. 3. (a) Finger-type layout pattern and (b) the corresponding cross-sectional view of the stacked-nMOS device in a P-substrate CMOS process.

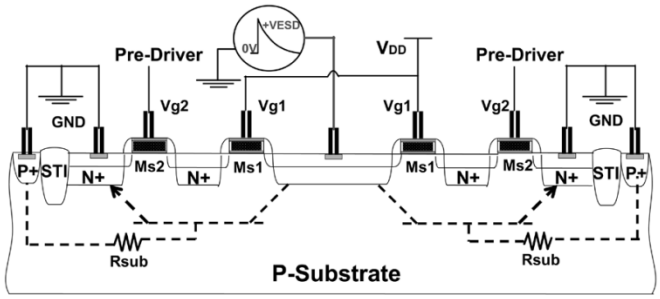


Fig. 4. Cross-sectional view of the stacked-nMOS device indicating the bipolar effect during the positive-to-VSS ESD-stress condition.

Under the positive-to-VSS ESD-stress condition (with VSS grounded but VDD floating), the stacked-nMOS device operates in snapback breakdown, with the bipolar effect taking place between the drain of the top nMOS and the source of the bottom nMOS. Fig. 4 shows a device cross-sectional view of a stacked-nMOS device indicating the bipolar effect during the positive-to-VSS ESD-stress condition [25], [26]. These two diffusions act as bipolar emitter and collector, respectively. Their spacing determines the base width and turn-on efficiency of the lateral n-p-n bipolar transistor in the stacked-nMOS device.

The snapback mechanism of a stacked-nMOS device for conducting a large amount of ESD current involves both avalanche breakdown and turn-on of the parasitic lateral n-p-n bipolar transistor. The hole current (Isub) generated from drain avalanche breakdown, drifting through the effective substrate resistance (Rsub) to ground, may elevate the substrate potential locally to the emitter–base junction of the n-p-n shown in Fig. 4. The voltage level, which the local substrate potential is elevated, depends on the relative proximity to the avalanching junction. When the emitter–base junction of lateral n-p-n bipolar transistor begins to weakly forward bias due to the increase of local substrate potential, additional electron current through the bipolar device acts as a "seed current" to drive a significant increase in the multiplication rate and avalanche current generation at the collector–base junction of the lateral n-p-n BJT. Therefore, a "snapback" is seen, and the lateral n-p-n BJT enters strong bipolar conduction.

B. Substrate-Triggered Stacked-nMOS Device

As shown in Fig. 4, the snapback operation of the stacked-nMOS device depends on the substrate current (Isub), which is created at the reversed-biased drain/p-substrate junction, to forward bias the substrate/source junction. Hence, the substrate resistance (Rsub) and substrate current (Isub) are the important design parameters for ESD protection [27]. The substrate-triggered circuit technique can be used to generate the substrate current to improve the turn-on speed of the lateral n-p-n BJT in the stacked-nMOS device during ESD stress event. With the substrate-triggered current, the trigger voltage (Vt1) of the stacked-

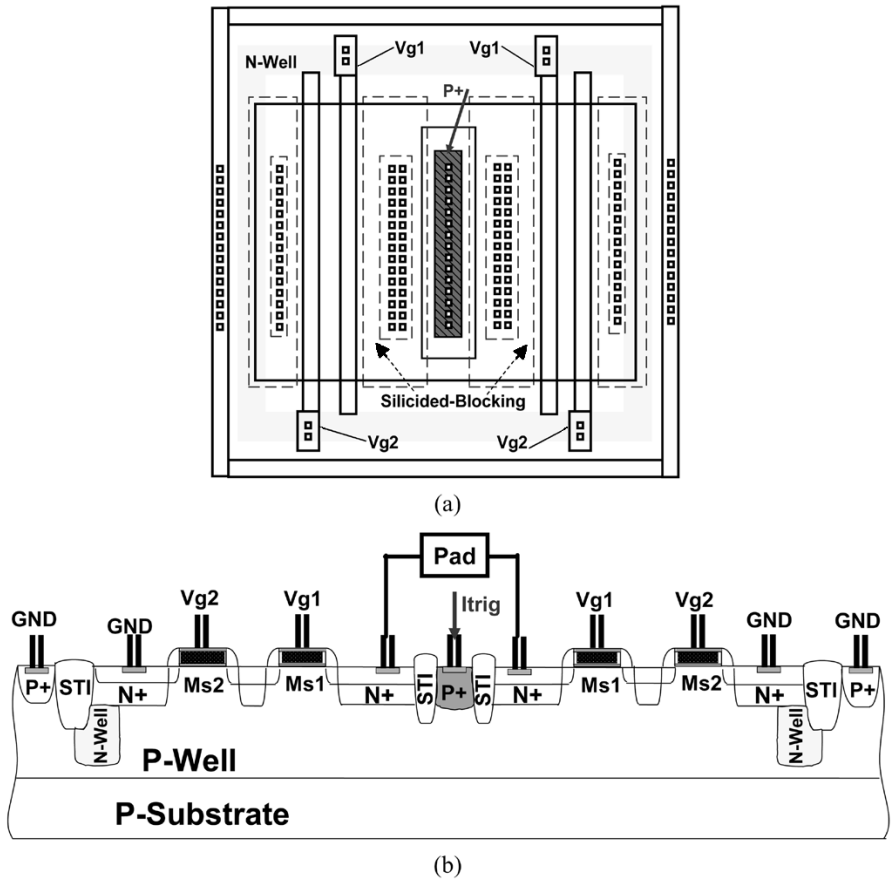


Fig. 5. (a) The finger-type layout pattern and (b) the corresponding cross-sectional view of the substrate-triggered stacked-nMOS device in a P-substrate CMOS process.

nMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection.

The substrate-triggered technique shows an obvious improvement of the ESD level of the large-dimension nMOS devices. In this study, the substrate-triggered stacked-nMOS device that combines the substrate-triggered circuit with the stacked-nMOS device is proposed. The finger-type layout pattern and the corresponding cross-sectional view of the new proposed substrate-triggered stacked-nMOS device are shown in Fig. 5(a) and (b), respectively. In Fig. 5(b), the p+ diffusion is inserted into the center region of the stacked-nMOS device as the substrate-triggered region. The trigger current (Itrig) is provided by the special ESD detection circuit. An n-well structure is further diffused under the source region of this device to form a higher equivalent substrate resistance to improve turn-on efficiency of the lateral n-p-n BJT in the stacked-nMOS device.

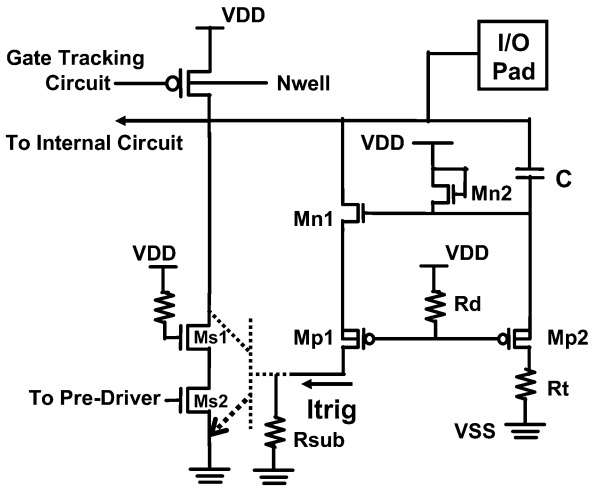


Fig. 6. Proposed on-chip ESD protection design for a mixed-voltage I/O circuit with the substrate-triggered stacked-nMOS device.

III. ESD Protection Circuit Design

The ESD protection design including the substrate-triggered stacked-nMOS device, the substrate-triggered circuit, and the corresponding cross-sectional view are shown in Figs. 6 and 7, respectively. The substrate-triggered circuit, composed of the pMOS (Mp1) and nMOS (Mn1), provides the substrate current for triggering on the parasitic lateral n-p-n bipolar junction transistor contained in the stacked-nMOS device, while the ESD voltage is zapping on the I/O pad. The drain of Mn1 and the capacitance C in the substrate-triggered circuit, as well as the collector of the parasitic n-p-n BJT in the stacked-nMOS device, are connected to the I/O pad. The gates of the pMOS (Mp1 and Mp2) are connected together to the VDD power line through a resistor Rd, which is an n+ diffusion resistance with a parasitic n+/p-sub diode used as an antenna diode to solve the antenna effect [28], [29] during the fabrication process. Fig. 7 shows

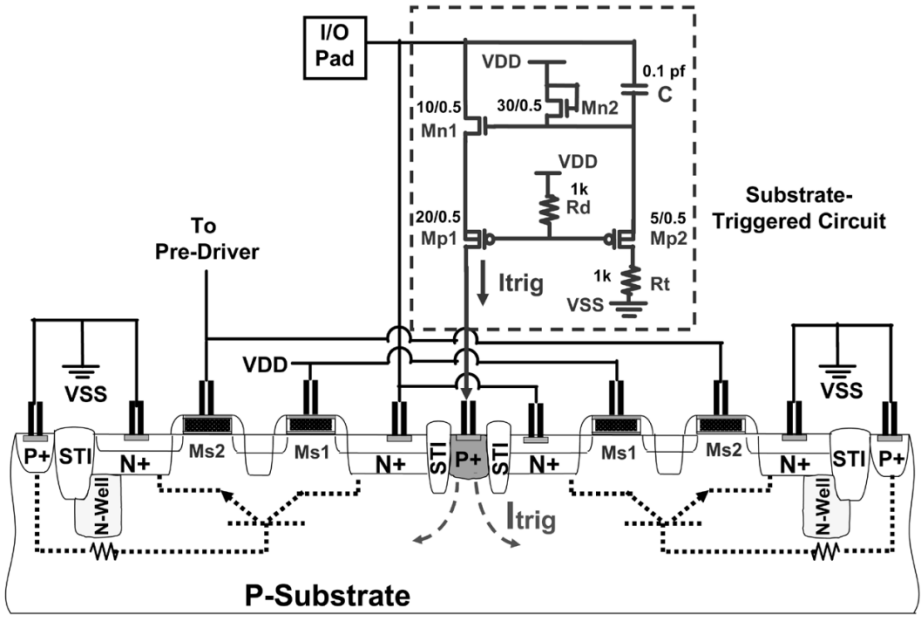


Fig. 7. Cross-sectional view of the stacked-nMOS device with the proposed substrate-triggered circuit.

the cross-sectional view of the stacked-nMOS device with a substrate-triggered circuit for protecting the mixed-voltage I/O circuits.

A. Operating Principles

The purpose of the substrate-triggered circuit is to provide the suitable trigger current into the substrate of the stacked-nMOS device under ESD stress condition. Under normal circuit operating conditions, the substrate-triggered circuit should be kept off and no trigger current should flow into the substrate of the stacked-nMOS device. So, the substrate-triggered circuit does not interfere with the normal voltage levels of the I/O pad.

Under the normal circuit operating conditions, for the 2.5-V/3.3-V mixed-voltage IC application, the input signal of 3.3 V applied to the I/O pad and a 2.5-V voltage supply is biased at VDD in the chip. The Ms1 (first nMOS of stacked nMOS) in Fig. 7 is biased at the voltage level of VDD. However, the gate of Ms2 (second nMOS of stacked nMOS) is biased at VSS by the predriver circuit. When the I/O pad is applied with a high input voltage of 3.3 V, the center common n+ region between the Ms1 and Ms2 transistors has a voltage level of VDD–Vtn (where Vtn is the threshold voltage of nMOS). The gates of Mp1 and Mp2 are biased with 2.5-V VDD supply in the substrate-triggered circuit, as showed in Fig. 7. When the input voltage on the I/O pad transfers from 0 to 3.3 V, the coupled gate voltage of Mn1 through the capacitor C increases. However, the Mn2 and Mp2 clamp the gate voltage of Mn1 within VDD$-$Vtn $\sim$ VDD $+$ |Vtp| (where Vtp is the threshold voltage of pMOS). Once the gate voltage of Mn1 is over VDD$+$|Vtp|, the Mp2 turns on to discharge the over-coupled voltage and keep the gate voltage within VDD$+$|Vtp|. Since the upper boundary on the gate voltage of the Mn1 is within VDD$+$|Vtp|, the source voltage of Mp1 is clamping below VDD, which keeps the Mp1 always off within the normal circuit operation condition.

So, these two pMOSs (Mp1 and Mp2) are kept off during normal circuit operating conditions. The substrate-triggered circuit is in an inactive state and no trigger current flows into the base of the lateral n-p-n BJT in the stacked-nMOS device. With a suitable design of the substrate-triggered circuit, the lateral n-p-n BJT in a stacked-nMOS device can be kept off under normal circuit operating conditions. Moreover, the Mn2 and Mp2 can further clamp the gate voltage of Mn1 and keep the Mp1 off to avoid the gate-oxide reliability issue in the substrate-triggered circuit, even if the I/O pad has a high input voltage level.

On the other hand, under the positive-to-VSS ESD-stress condition, a positive ESD voltage is applied to the I/O pad with VSS relatively grounded, and the VDD power line and other pins are floating with an initial voltage level of 0 V. The gates of pMOS (Mp1 and Mp2) have an initial voltage level of $\sim$0 V, so the Mp1 is initially turned on. Moreover, the ESD transient voltage on the I/O pad is coupled through the capacitance C (by dV/dt) to bias the gate of Mn1 and causes the Mn1 in the ON state. In this situation, both of the Mn1 and Mp1 are operated in the turn-on state. Therefore, the substrate-triggered circuit will conduct some ESD current from the I/O pad through Mn1 and Mp1 into the base of later n-p-n BJT in the stacked-nMOS device as the trigger current (Itrig), as shown in Fig. 7. For a given Rsub, the substrate-triggered circuit must supply enough trigger current (Itrig) to raise the substrate potential. So, $V_{BE}(=$ Isub $\times$ Rsub$)$ can become greater than 0.6 V to trigger the lateral n-p-n BJT in the stacked-nMOS device. Once the parasitic lateral n-p-n BJT is turned on, ESD current is mainly discharged from the I/O pad through the lateral n-p-n BJT to the grounded VSS. With an appropriate Itrig, the substrate potential is raised high enough to trigger on the lateral n-p-n BJT and therefore to reduce its trigger voltage.

The stacked-nMOS device with a substrate-triggered technique can successfully protect thin gate oxide in the mixed-

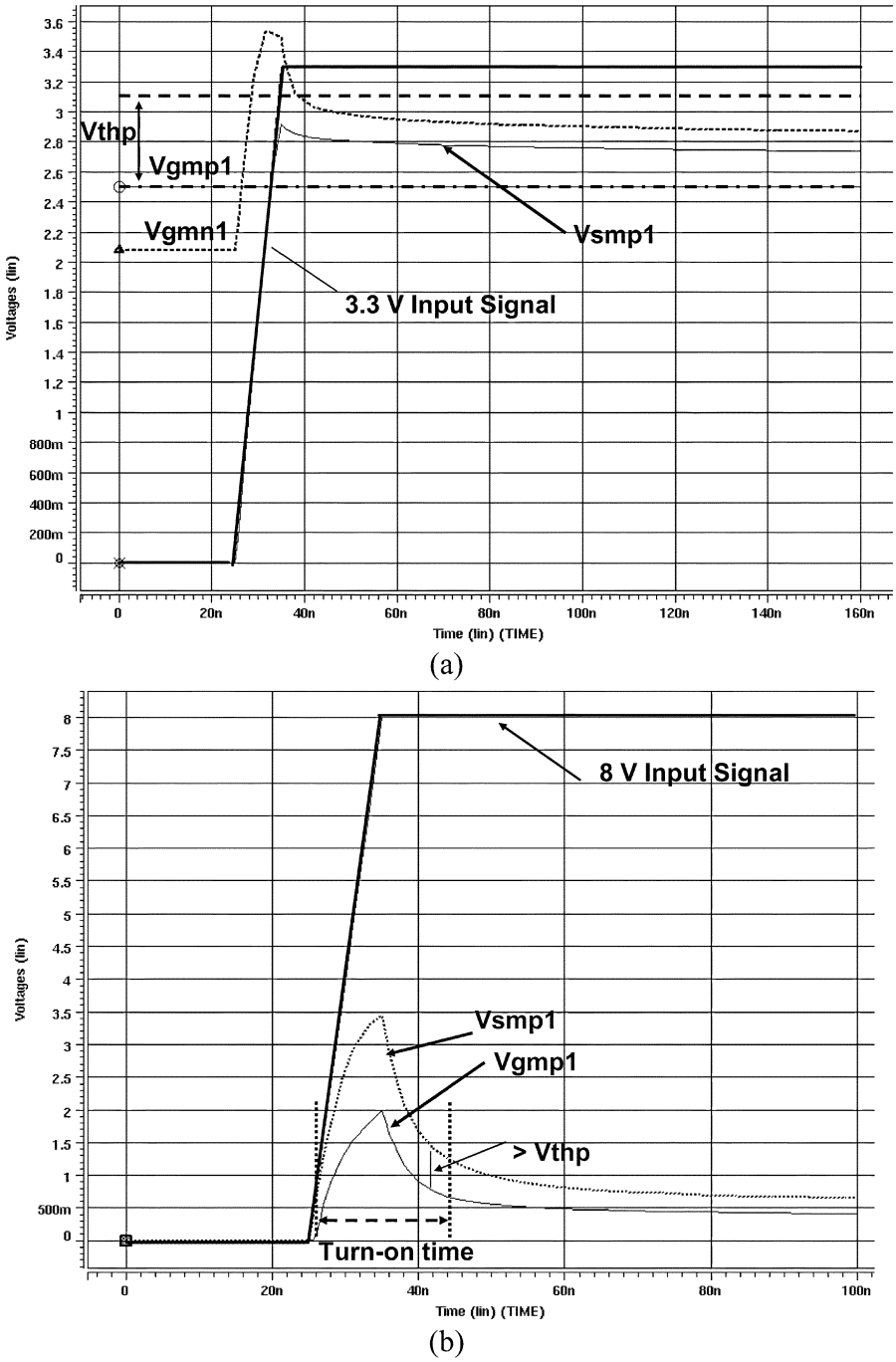


Fig. 8. HSPICE-simulated results on a mixed-voltage I/O buffer with the proposed substrate-triggered circuit under (a) the normal circuit operating conditions with a 3.3-V input signal and (b) the ESD stress condition with an 8-V input signal.

voltage I/O circuits to have much higher ESD robustness within a smaller silicon area.

B. Simulation Results

The purpose of the substrate-triggered circuit is to provide a suitable trigger current into the substrate of the stacked-nMOS device under ESD stress conditions. Under normal circuit operating conditions, the substrate-triggered circuit should be turned off and no trigger current should flow into the substrate of the stacked-nMOS device. To obtain a suitable trigger current, it is important to determine the values of the coupling capacitor C and the device dimensions of Mn1 and Mp1. Based on the above operation principle, the suitable device dimensions of the trigger circuit to meet the desired circuit application in different CMOS processes can be adjusted by HSPICE simulation.

The device dimensions of the substrate-triggered circuit and the turn-on time period of the substrate-triggered circuit, shown in Fig. 7, can be investigated by HSPICE simulation. The device dimensions are chosen as follows, Mn1 at 10 μm/0.5 μm, Mp1 at 20 μm/0.5 μm, Mn2 at 30 μm/0.5 μm, Mp2 at 5 μm/0.5 μm, C at 0.1 pF, and Rd $=$ Rt at 1 kΩ. A 0–3.3-V input waveform with a rise time of 10 ns is used to simulate a 3.3-V input signal applied to the I/O pad, when the mixed-voltage I/O circuit is

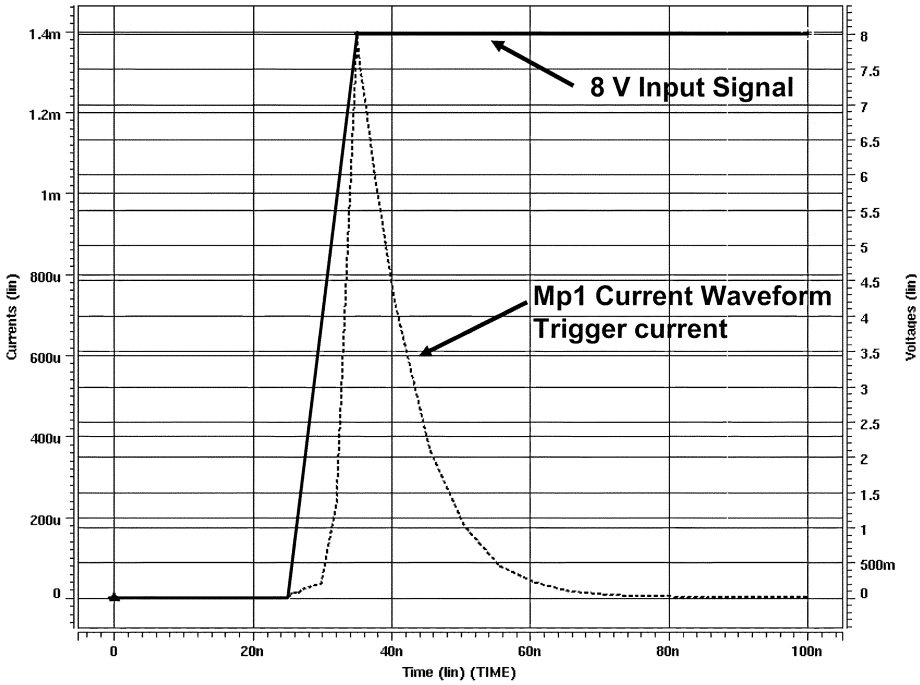


Fig. 9. HSPICE-simulated results of the substrate-triggered current waveform generated by the substrate-triggered circuit under the ESD stress condition with an 8-V input signal.

under normal circuit operating conditions with VDD biased at 2.5 V, as shown in Fig. 8(a). In Fig. 8(a), even if the 3.3-V input signal with a rise time of 10 ns, the voltage difference between Vgmp1 (the gate voltage of the transistor Mp1) and Vsmp1 (the source voltage of the transistor Mp1) can be kept within Vtp (the threshold voltage of the transistor Mp1) during the input transition period. The Mp1 is kept off, and no current is conducting to trigger the stacked nMOS. So, the stacked nMOS can be guaranteed to be off under the normal circuit operating conditions in the mixed-voltage I/O buffer.

Under the ESD stress condition, a positive 0–8 V voltage with a rise time of 10 ns is applied to the I/O pad with V_{SS} grounded but VDD floating. As shown in Fig. 8(b), under the 8-V input signal with the rise time of 10 ns, the voltage difference between Vgmp1 (the gate voltage of the transistor Mp1) and Vsmp1 (the source voltage of the transistor Mp1) can be over Vtp. The Mp1 is turned on to generate a 1.4-mA triggering current into the substrate of the stacked nMOS, as shown in Fig. 9. By adding the substrate-triggered circuit into the mixed-voltage I/O buffer, it becomes very easy and feasible to determine the device dimensions of the trigger circuit by HSPIC simulation.

IV. Experimental Results

The stacked nMOS with substrate-triggered design for mixed-voltage I/O circuit had been fabricated in a 0.25-μm CMOS process with silicided-blocking mask. The I–V characteristics of the stacked-nMOS devices with different substrate-triggered currents are measured by the curve tracer (*Tek370A*). The ESD simulator (*ZapMaster*) is used to evaluate ESD robustness of the devices with the failure criterion of 1-μA current leakage under a 3.3-V bias.

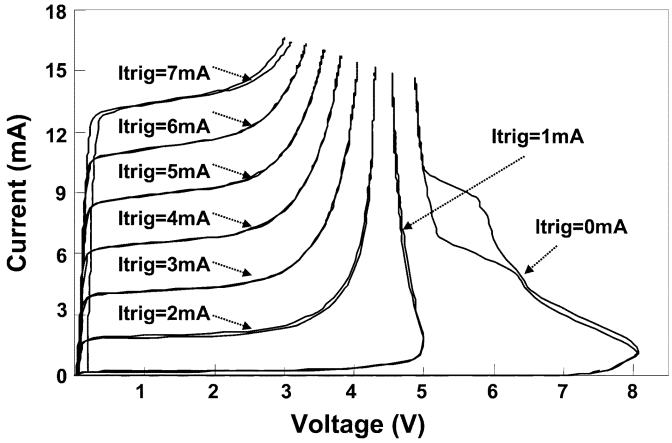


Fig. 10. Measured I–V characteristics of stacked-nMOS device under different substrate-triggered currents.

A. Characteristics of the Substrate-Triggered Stacked-nMOS Device

The measured I–V characteristics of the stacked-nMOS device under different substrate-triggered currents are shown in Fig. 10. The trigger voltage of the stacked-nMOS device decreases when the substrate-triggered current increases. The trigger voltage can be reduced to only $\sim$3.1 V, when the Itrig is 7 mA. Based on the above experimental results, effective ESD protection design can be achieved by the substrate-triggered circuit to generate the substrate current to further increase ESD robustness of the stacked-nMOS device in the mixed-voltage I/O buffer.

To investigate the device behavior during high ESD current stress, the transmission line pulsing (TLP) technique [30] has

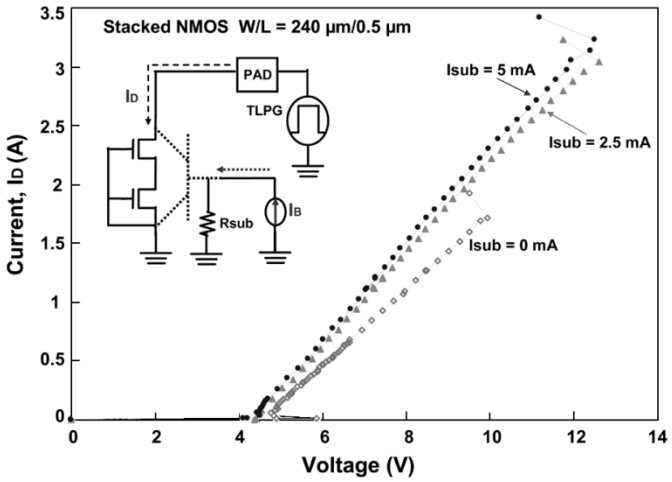


Fig. 11. TLP-measured I–V curves of the stacked-nMOS devices fabricated in a 0.25-μm salicided CMOS process with different substrate-triggered currents.

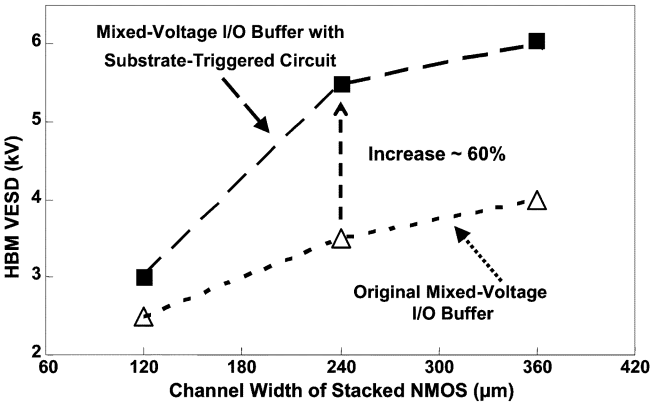
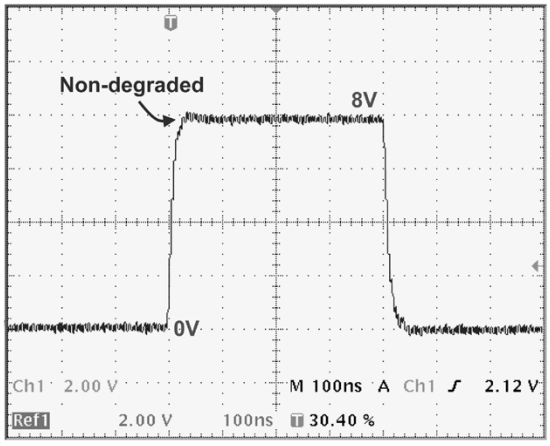
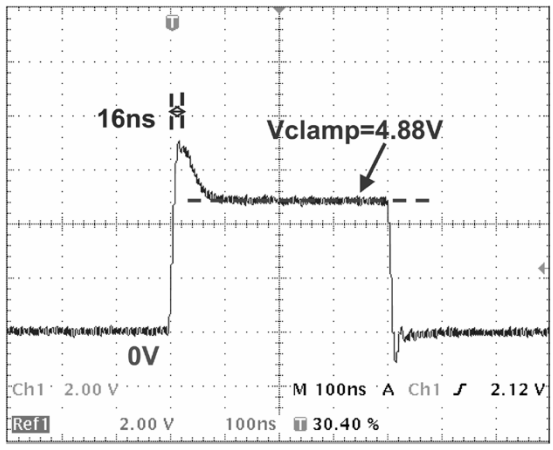


Fig. 12. The positive-to-V_{SS} HBM ESD levels of the mixed-voltage I/O buffers with or without the substrate-triggered circuit in a 0.25-μm CMOS process.



(a)



(b)

Fig. 13. Voltage waveforms of the mixed-voltage I/O circuit zapped by a 0–8-V voltage pulse (a) without the substrate-triggered design and (b) with the substrate-triggered design. (Y axis $=2$ V/div., X axis $=100$ ns/div.).

been widely used to measure the second breakdown characteristics of devices. The TLP generator (TLPG) with a pulse width of 100 ns is used to find the second breakdown current (It2) of the fabricated stacked-nMOS devices under different substrate-triggered currents. The TLP-measured I–V characteristics of the substrate-triggered stacked-nMOS devices with the device dimension (W/L) of 240 μm/0.5 μm, under substrate-triggered currents of 0, 2.5, and 5 mA are shown in Fig. 11. The It2 of the stacked-nMOS device without substrate-triggered current is only 1.7 A, but it can be increased up to 3.3 A, while the stacked-nMOS device with a substrate-triggered current of 5 mA. With a higher It2, the stacked-nMOS can sustain a higher ESD level.

B. ESD Robustness

The original mixed-voltage I/O buffers with different stacked-nMOS channel widths are also fabricated in the same test chip and tested as a reference. All stacked-nMOS devices with different channel widths have the same channel length of 0.5 μm for both the first and second nMOS (Ms1 and Ms2), and the n+ diffusion layout spacing between the two poly gates in the stacked-nMOS device is fixed at 0.4 μm. The HBM ESD levels of the mixed-voltage I/O circuits with or without the proposed substrate-triggered design are compared in Fig. 12. For the stacked-nMOS device with a channel width of 240 μm, it can sustain the HBM ESD level of 3.5 kV. However, if such a stacked-nMOS device is designed with the proposed substrate-triggered circuit, its ESD level can be increased up to 5.5 kV. It has a ~60% improvement from its origin value by this substrate-triggered design. This has verified the effectiveness of the proposed substrate-triggered design to improve the ESD level of mixed-voltage I/O circuits.

C. Turn-On Verification

A voltage pulse, generated from a pulse generator with a pulse height of 8 V and a rise time of 10 ns, is used to simulate the rising edge of an ESD pulse. Such a voltage pulse is applied to mixed-voltage I/O buffers with or without the proposed substrate-triggered design under the positive-to-VSS ESD stress condition to verify their turn-on behaviors. When the 0–8 V voltage pulse is applied to the pad of the mixed-voltage I/O buffer without the substrate triggered design, the voltage waveform on the pad is observed and shown in Fig. 13(a), where

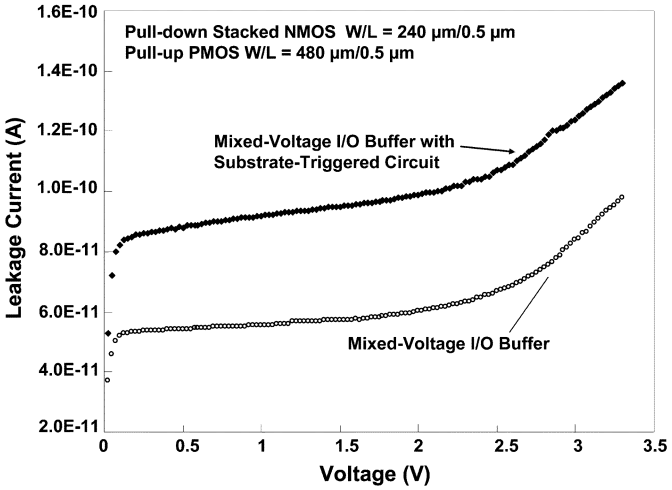


Fig. 14. Comparison of the leakage current between the mixed-voltage I/O buffers with or without the proposed substrate-triggered circuit.

there is no degradation of the voltage waveform. This means that the lateral n-p-n BJT in the stacked-nMOS device is not triggered by such a voltage pulse. On the contrary, when such a 0–8-V voltage pulse is applied to the pad of the mixed-voltage I/O buffer with the substrate-triggered design, the voltage waveform on the pad is observed and shown in Fig. 13(b), where the voltage waveform of the pad is clamped to ~4.88 V within a short turn-on time of about ~16 ns. This means that the lateral n-p-n BJT in the stacked-nMOS device can be triggered on by such a voltage pulse. Thus, during the ESD stress condition, the stacked-nMOS device in the mixed-voltage I/O buffer with the substrate-triggered design can be quickly and fully turned on to discharge ESD current. Therefore, it can provide more effective ESD protection to the thinner gate oxide of mixed-voltage I/O circuits in the subquarter-micron CMOS processes.

D. Leakage Current

The leakage current under normal circuit operating conditions is a concern for an ESD protection circuit connected to an I/O pad. The leakage currents of the fabricated mixed-voltage I/O buffers with or without the proposed substrate-triggered circuit are measured and compared in Fig. 14. In the mixed-voltage I/O buffer, the device dimension (W/L) of a stacked nMOS is $240\ \mu\text{m}/0.5\ \mu\text{m}$ and that of the pull-up pMOS is $480\ \mu\text{m}/0.5\ \mu\text{m}$. The leakage current is measured (using HP 4155) by applying a voltage ramp from 0 to 3.3 V to the I/O pad under the V_{DD} biased at 2.5 V and V_{SS} grounded. In Fig. 14, the maximum leakage current of a mixed-voltage I/O buffer with (without) the proposed substrate-triggered circuit under 3.3-V bias at the I/O pad is 137 (84) pA. The increase of the leakage current from the proposed substrate-triggered circuit is only 54 pA, which is still small enough for general I/O circuit applications.

V. Conclusion

To improve ESD robustness of stacked-nMOS devices in mixed-voltage I/O circuits, a new ESD protection design has been proposed and successfully verified in a 0.25-μm CMOS process. The HBM ESD level of the mixed-voltage I/O circuit with a stacked-nMOS device of 240-μm channel width can be improved from the original 3.5 up to 5.5 kV (increase of ~60%) by the proposed substrate-triggered design. Without using the thick gate oxide, this new proposed ESD protection design is fully process compatible with general subquarter-micron CMOS processes for effectively protecting the mixed-voltage interface circuits on the input and output pins. This design can be also applied to the I/O interfaces with the voltage levels of 1.8 V/3.3 V, 1.8 V/2.5 V, or other different voltage levels.

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Ming-Dou Ker (S'92–M'94–SM'97) received the B.S. degree and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1986, 1988, and 1993, respectively.

In 1994, he joined the VLSI Design Department, Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Taiwan, R.O.C. In 1998, he was the Department Manager of the VLSI Design Division, CCL/ITRI. In 2000, he became an Associate Professor with the Department of Electronics Engineering, National Chiao-Tung University. He has been invited to teach or help ESD protection design and latchup prevention by hundreds of design houses and semiconductor companies in the Science-Based Industrial Park, Hsinchu, Taiwan, and in the Silicon Valley, San Jose, CA. His research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed or mixed-voltage I/O interface circuits, especially sensor circuits, and semiconductors. He has published over 200 technical papers in international journals and conferences in the field of reliability and quality design for CMOS integrated circuits. He holds over 180 patents on reliability and quality design for integrated circuits, including 81 U.S. patents. His inventions on ESD protection design and latchup prevention method have been widely used in modern IC products.

Dr. Ker has served as a member of the Technical Program Committee and as Session Chair of many international conferences. He was elected the first President of the Taiwan ESD Association in 2001. In 2003, he was selected as one of the Ten Outstanding Young Persons in Taiwan by Junior Chamber International (JCI).

Hsin-Chyh Hsu (S'03) received the B.S. degree in physics from National Taiwan University, Taipei, Taiwan, R.O.C., in 1999 and the M.S. degree in electrical engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2002, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include ESD physics, semiconductor devices, and ESD protection design in deep-submicron CMOS technologies.