Modeling Mechanical Stress Effect on Dopant Diffusion in Scaled MOSFETs

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***Abstract*—The effect of shallow trench isolation mechanical stress on MOSFET dopant diffusion has become significant, and affects device behavior for sub-100-nm technologies. This paper presents a stress-dependent dopant diffusion model and demonstrates its capability to reflect experimental results for a state-of-the-art logic CMOS technology. The proposed stress-dependent dopant diffusion model is shown to successfully reproduce device characteristics covering a wide range of active area sizes, gate lengths, and device operating conditions.**

***Index Terms*—Dopant diffusion, mechanical stress, modeling, MOSFET, shallow trench isolation (STI), simulation, strain.**

I. Introduction

As a result of the aggressive downscaling of CMOS technology, shallow trench isolation (STI)-induced mechanical stress increases in magnitude with reduced device active areas, causing a nonnegligible impact on device performance [1]–[4]. Both experimental work and numerical simulations have been conducted to calculate the STI stress magnitude and distribution encountered in scaled MOSFETs [5]–[9]. The results show that the silicon stress level near the STI region is high. As design rules or layout dimensions scale down, the high-stress region encroaches further into the MOSFET channel. Thus, STI mechanical stress has a significant influence on state-of-the-art device performance.

Earlier work studying the mechanical stress effect has been focused on the MOSFET drive current shift, either in the form of localized or planar stress conditions [1]–[3], [6], [10]–[14]. Several studies have been performed to link STI mechanical stress to mobility changes while accounting for the observed current shift [2], [12], [13], although no threshold voltage shift mechanism has been investigated. Scott *et al.* [14] have investigated both the drive current and threshold voltage shift, suggesting a difference in stress-induced diffusivity as the plausible origin of the threshold voltage shift. So far, however, there has been no further elaboration on this aspect. On the other hand, there has been a great deal of work devoted to dopant diffusion behavior in silicon under the influence of mechanical stress [15]–[19]. Cowern *et al.* [15] proposed a strain-induced dopant diffusivity model of boron diffusion in SiGe. Ahn *et al.* [17] concluded that in the presence of high-stress nitride film, phosphorus diffusion in the silicon was retarded, whereas antimony diffusion was enhanced. Aziz [18] established a relationship between hydrostatic pressure and biaxial strain via thermodynamic formulation, while accommodating calculation of the activation energy shift due to strain. Based on Azizs and Cowerns theoretical work [15], [18], Zangenberg *et al.* [19] critically reviewed the findings over the past ten years and further identified the strain effect on boron and phosphorus diffusion in SiGe. However, most studies in the area of mechanical stress-induced dopant diffusion changes remain in fundamental research, i.e., at the silicon material level, and have not yet been extended to semiconductor device characterization and modeling.

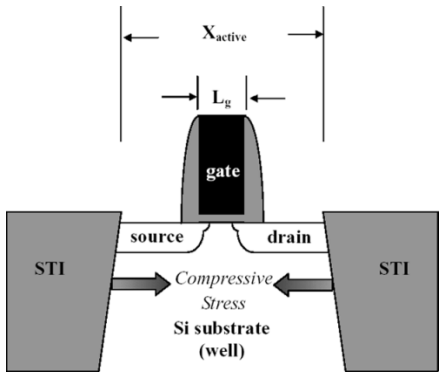

Fig. 1. Schematic cross section of the device along channel length direction with active area size $X_{\rm active}$ and gate length L_g both as parameters. The stress condition is compressive mainly because of the lower thermal expansion rate of STI oxide compared to silicon, and the thermal gate oxidation-induced volume expansion at the STI edge.

It is well recognized that the key MOSFET parameters, such as threshold voltage, drain-induced barrier lowering, body factor, and subthreshold swing, are all strongly dependent on dopant distribution details. Thus, it is crucial to examine stress-dependent dopant diffusion for scaled MOSFETs under mechanical stress.

In this paper, we present a stress-dependent diffusion model and incorporate it into a two-dimensional (2-D) process simulation environment to assess the doping distribution effect in scaled MOSFETs. The proposed model is corroborated by extensive experimental data in a sub-100-nm CMOS technology.

Manuscript received June 14, 2004. This work was supported by the National Science Council under Contract NSC 93-2215-E-009-024. The review of this paper was arranged by Editor C.-Y. Lu.

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Digital Object Identifier 10.1109/TED.2004.841286

II. Stress-Dependent Diffusion Model and Modeling Methodology

A. Stress-Dependent Diffusion Model

Several approaches dealing with dopant diffusion dependencies on strain are briefly described in the preceding section. The general concept of these approaches is to express dopant diffusion under mechanical stress in an Arrhenius form [15], [18], [19]. For example, in the case of a compressively strained SiGe layer where Cowern studied boron diffusion [15], the stress condition is regarded as biaxial and the dopant diffusion dependence follows the Arrhenius form

$$D_S = D_I \exp\left[-\frac{sQ'}{kT}\right] \tag{1}$$

where D_S is the dopant diffusivity under strain, D_I is the dopant diffusivity without strain, s is the biaxial strain in the plane of the SiGe layer, and Q' is the activation energy per strain.

Analogous to the above strained SiGe layer, we develop a stress-dependent dopant diffusion model for dopant diffusion under STI mechanical stress, named the volume-change-ratio-induced diffusion activation energy shift model (VIDAESM). The volume change ratio $V_{\rm cr}$ is a function of position due to nonuniform stress distributions. In this paper, the MOSFET width is large enough to allow the three-dimensional stress effect to be reduced to the 2-D one. The activation energy involved is the product of a dopant-dependent coefficient and volume change ratio, meaning that (1) can be rewritten in the case of dopant diffusion under STI mechanical stress

$$D_S(T,x,y) = D_I(T) \exp\left[-\frac{\Delta E_S V_{\rm cr}(T,x,y)}{kT}\right] \tag{2}$$

where D_S is the dopant diffusivity under strain, D_I is the dopant diffusivity without strain, $V_{\rm cr}$ is the volume change ratio due to stress, ΔE_S is the activation energy per volume change ratio depending on the dopant species, and T is the temperature. When the strain is small, the volume change ratio can be expressed as

$$V_{\rm cr}(T,x,y) \cong \varepsilon_t(T,x,y) \equiv \varepsilon_{xx}(T,x,y) + \varepsilon_{yy}(T,x,y) + \varepsilon_{zz} \tag{3}$$

where ε_{xx} is the strain along the channel length direction, ε_{yy} is the strain in the direction perpendicular to the silicon surface, ε_{zz} is the strain along the channel width direction, and ε_t is the strain summation of ε_{xx}, ε_{yy}, and ε_{zz}. Note that ε_{zz} is zero in the 2-D simulation due to wide structures adopted. Therefore, (2) becomes

$$D_S(T,x,y) = D_I(T) \exp\left[-\frac{\Delta E_S \varepsilon_t(T,x,y)}{kT}\right]. \tag{4}$$

A 2-D numerical process simulator TSUPREM4 is chosen to perform the process simulation. TSUPREM4 is capable of simulating intrinsic dopant diffusion, three-stream dopant-point defect pairing diffusion, the oxidation-enhanced diffusion

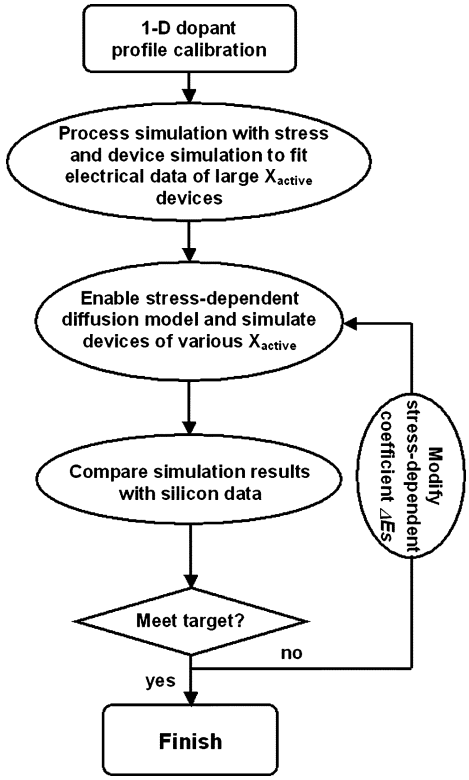

Fig. 2. Flow chart of the modeling procedure.

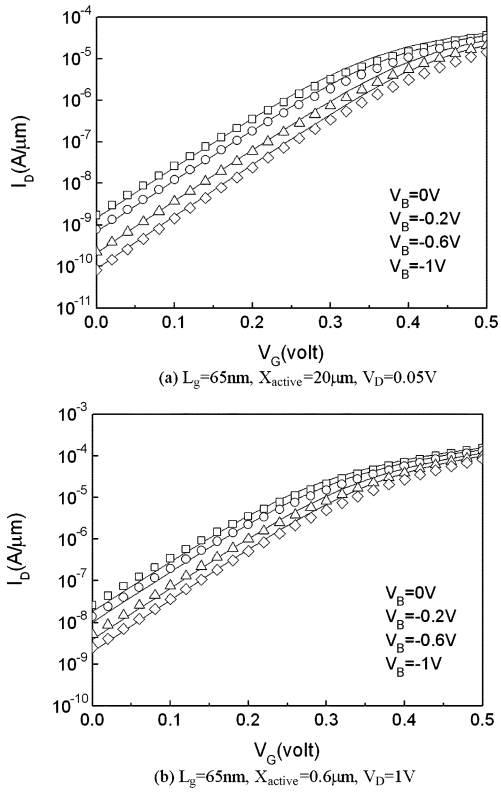

Fig. 3. *I–V* calibration result of a short-channel nMOSFET with large $X_{\rm active}$ for (a) $V_D = 0.05$ V and (b) $V_D = 1$ V. $L_g = 65$ nm and $X_{\rm active} = 10$ μm. Symbols stand for the silicon data. Solid lines are the calibrated simulation result.

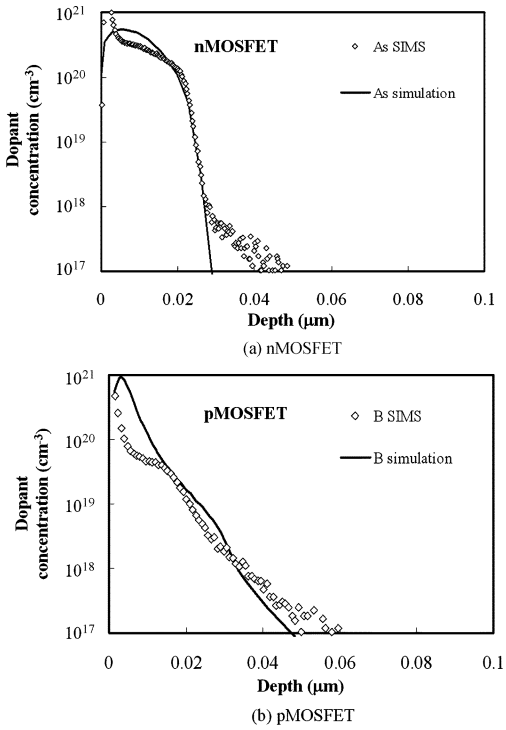

Fig. 4. SIMS and calibration results of 1-D dopant profile for (a) nMOSFET and (b) pMOSFET.

effect, the dopant clustering effect, and the dislocation loop effect. For assessment of mechanical stress, the simulator also simultaneously solves force balance equations while taking into account thermal expansion, intrinsic stress, geometry rearrangement after etch and deposition processes, and the thermal oxidation process [20]. The stress-dependent diffusion model VIDAESM has been incorporated into the simulator through the user-specified equation interface to adaptively calculate stress-dopant diffusivity during the process simulation.

B. Modeling Methodology

To model stress-dependent dopant diffusion for various stress levels, we designed and fabricated a series of MOSFETs with various active area sizes. Fig. 1 schematically shows the cross section view of a test device along the channel direction. The mechanical stress effect was explored here with active area size, $X_{\rm active}$, and gate length L_g, both used as the main structural parameters.

The flow chart of the modeling procedure is shown in Fig. 2. First, the one-dimensional (1-D) dopant profiles were processed using blanket control wafers, which covered the range of the process conditions of the device wafers. The results were then taken as stress-free dopant profiles and used to calibrate the dopant diffusion parameters without stress-dependent models.

Second, 2-D MOSFET structures were simulated using the mechanical stress model. Calibrated diffusion parameters were employed to simulate a large $X_{\rm active}$ MOSFET, where the stress level is low. All front-end major process steps from the STI

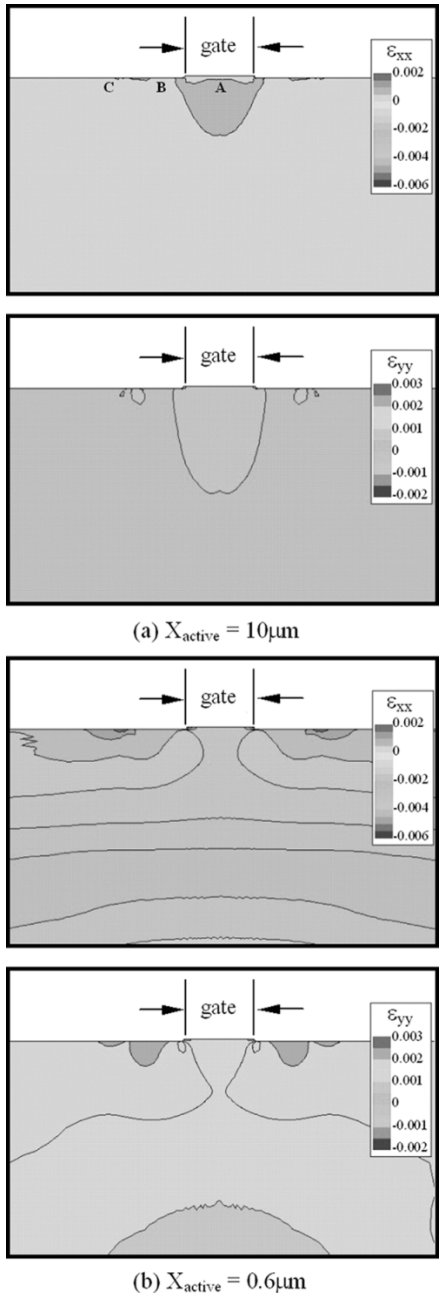

Fig. 5. Simulated strain distribution in the silicon of entire front-end process for Lg= 65 nm, (a) $X_{\rm active} = 10\ \mu$m, (b) $X_{\rm active} = 0.6\ \mu$m. A small $X_{\rm active}$ causes a much higher strain.

to the source/drain anneal were considered. The corresponding simulation geometries were calibrated using transmission electron microscope cross-sectional images. Some fine tuning of the 2-D dopant profile parameters, such as implant lateral straggles and segregation factors, are needed to fit the silicon device current–voltage (*I–V*) characteristics. Fig. 3 shows the calibration result of a short-channel nMOSFET *I–V* with a large $X_{\rm active}$.

Next, with the stress distribution known, the stress-dependent diffusion models were introduced to simulate MOSFETs with varying $X_{\rm active}$ values. After implementing the stress-dependent diffusion model, process simulation results were used

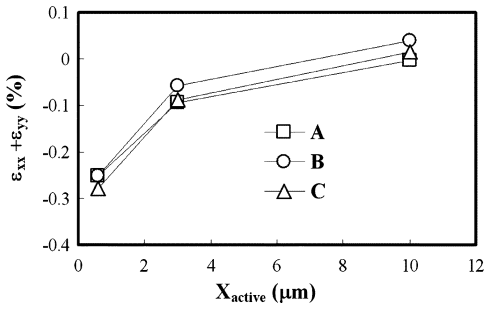

Fig. 6. Magnitude of strain versus $X_{\rm active}$ corresponding to three points **A**, **B**, and **C** in Fig. 4.

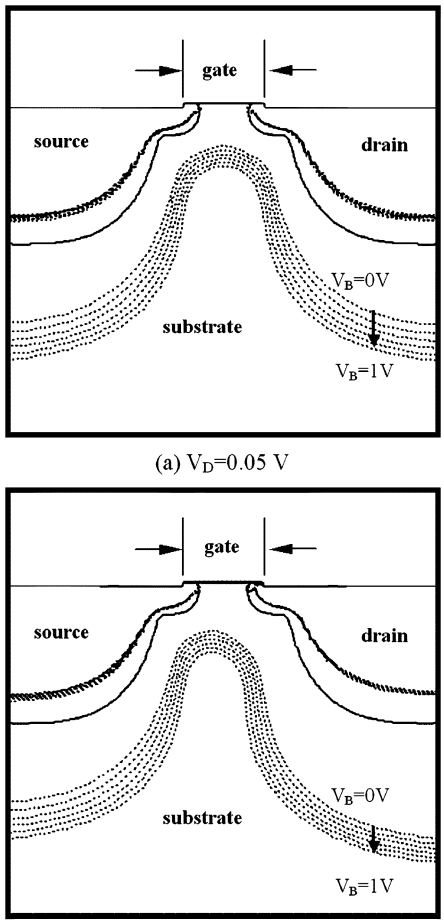

Fig. 7. Depletion region boundaries with substrate bias $V_{\rm B}$ for 65-nm nMOSFET at (a) $V_D = 0.05$ V and (b) $V_D = 1$ V.

as device simulation inputs. MEDICI was chosen as the numerical device simulator. The device modeling parameters, such as carrier mobility, work function, and silicon/oxide interface charges were calibrated to fit the *I–V* of large $X_{\rm active}$ MOSFETs. Then, device simulations with various $X_{\rm active}$ values were performed and compared with silicon device data. The above procedure was iterated from process to device cycle until the current-voltage data was all satisfactorily reproduced in all cases. The ΔE_S values from the previous work [15] were employed as the initial guess values. It is worth noting that the numerical convergence and simulation speed were not greatly

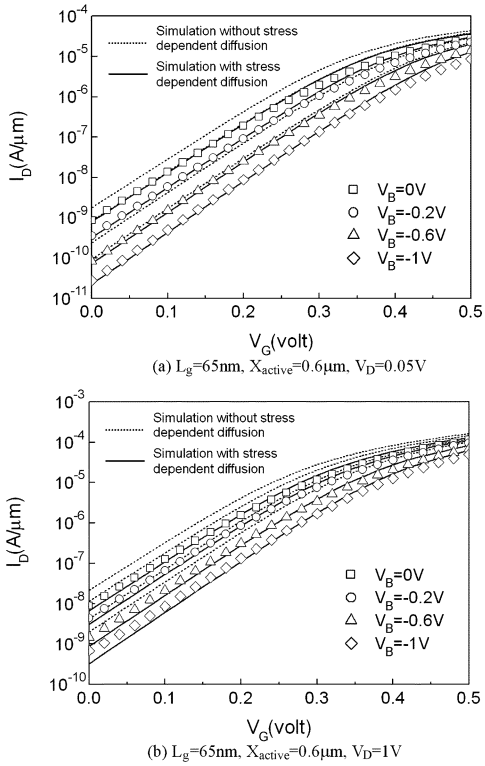

Fig. 8. *I–V* comparison among experimental data, simulation without stress-dependent diffusion model, and simulation with stress-dependent diffusion model for a small $X_{\rm active}$ MOSFET at (a) $V_D = 0.05$ V and (b) $V_D = 1$ V. $L_g = 65$ nm and $X_{\rm active} = 0.6$ μm. Symbols stand for the silicon data. Dashed lines are the simulation without stress-dependent diffusion model. Solid lines are the simulation with stress-dependent diffusion model.

influenced after implementing VIDAESM. The simulation time incorporating VIDAESM increases by about 7% compared to that without VIDAESM.

III. Experimental and Comparisons

The silicon wafers were fabricated using novel CMOS processes. The control wafers for 1-D SIMS analysis were processed using the same thermal steps as device wafers. Fig. 4 displays SIMS results for both n– and pMOSFET. The implant conditions were BF_2 2 keV 1×10^{15} cm^{-3} and As 2 keV 1×10^{15} cm^{-3} for ultrashallow junction calibration and the junction depths are around 260 angstroms for both devices. The calibrated simulation profile is also plotted in Fig. 4. The calibration procedure included the fine-tuning of implant damage, dopant-point defect pairing diffusion, silicon-oxide dopant segregation, oxidation enhanced diffusion models, dopant clustering models, dopant-defect clustering models, and intrinsic diffusion models.

The stress simulation involved the main process steps, which are STI formation, gate oxidations, and poly-gate formation in sequence. Viscoelastic oxidation model was used to simulate the stress-dependent oxide growth. The Youngs moduli used were 1.87×10^{12} dyne/cm^2 for the silicon and 6.6×10^{11} dyne/cm^2 for the oxide layers. The intrinsic stress used is -1.5×10^9 dyne/cm^2 for the STI oxide and 3.3×10^8 dyne/cm^2 for gate spacer oxide. The other parameters follow the default values in the TSUPREM4 manual [20].

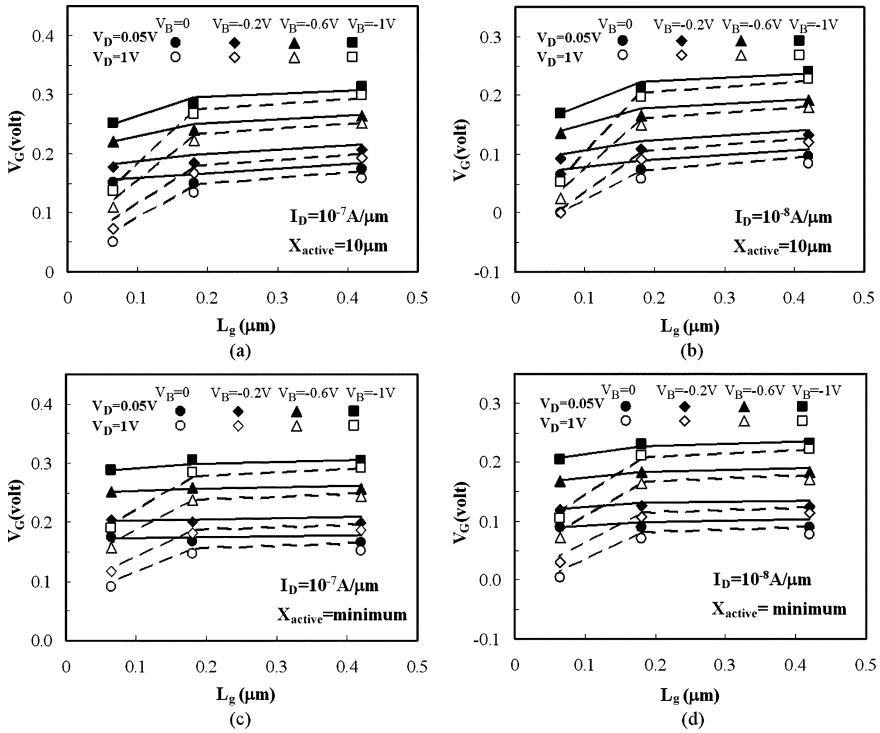

Fig. 9. Comparison of experimental and simulated nMOSFET $V_{\rm G}$ at different I_D level for various L_g and $X_{\rm active}$. Minimum $X_{\rm active}$ for Lg $= 65$ nm is 0.6 μm, for Lg $= 0.18$ μm is 0.74 μm, and for Lg $= 0.42$ μm is 1 μm. Final set of dopant diffusion parameters can model MOSFETs of different $X_{\rm active}$ under various drain voltages and substrate biases. Symbols stand for silicon data. Solid lines represent simulations with stress-dependent diffusion model. (a) $I_D = 10^{-7}$ Aμm, $X_{\rm active} = 10$ μm; (b) $I_D = 10^{-8}$ Aμm, $X_{\rm active} = 10$ μm; (c) $I_D = 10^{-7}$ Aμm, $X_{\rm active} =$ minimum; (d) $I_D = 10^{-8}$ Aμm, $X_{\rm active} =$ minimum.

The stress distribution results for different $X_{\rm active}$ values are given in Fig. 5. It can be seen that the polarity of the strain $\varepsilon_{\rm xx}$ in the lateral direction is negative, meaning that the MOSFET core area experiences a compressive stress. On the other hand, strain ε_{yy} in the vertical direction is tensile with a magnitude much smaller than $\varepsilon_{\rm xx}$. In particular, Fig. 5(b) reveals that ε_{xx} drastically increases in magnitude with decreasing $X_{\rm active}$ values. Three reference points **A**, **B**, and **C** are chosen to inspect the value of the strain. **A** is at the center of the gate, **B** is 75 nm away from the gate center and **C** is 150 nm from the gate center. The depth of these points is 20 nm from the silicon surface. Fig. 6 highlights the magnitude of the strain versus the $X_{\rm active}$ value at points **A**, **B**, and **C** in Fig. 5. The negative polarity of the strain means that the general strain conditions in the active area are compressive, and the magnitude increases rapidly as the value of $X_{\rm active}$ decreases. The compressive stress mainly comes from lower thermal expansion rate of the STI oxide compared to silicon, and the thermal gate oxidation-induced volume expansion at the STI edge. As $X_{\rm active}$ decreases, the STI approaches the MOSFET core region and increases the magnitude of compressive stress.

The MOSFET channel width in the silicon experiment was fixed at 10 μm, large enough to ensure that the stress along the channel width direction is negligible. Simulations were conducted to evaluate the mechanical stress along the channel width direction. The results showed that the average strain level for channel width $W = 10$ μm is around -0.02%, which is at least two orders of magnitude lower than the peak strain level used in this paper. The MOSFET design set consisted of $X_{\rm active}$ values from 0.6 to 10 μm and L_g from 65 nm to 0.42 μm. It has been recognized that boron and phosphorus diffusion are retarded by compressive strain [15], [19], [21]. The stress simulation results show that the MOSFET channel stress and strain magnitudes for $X_{\rm active} = 10$ μm are around -1×10^8 dyne/cm^2 and -0.04%, respectively. As the $X_{\rm active}$ value shrinks to 0.6 μm, the corresponding stress and strain magnitudes become around -5×10^9 dyne/cm^2 and -0.4%, respectively. The compressive strain level in the channel region is quite close to the strain produced by 10% germanium in silicon, which falls within the range of Cowern's and Zangenberg's studies [15], [19].

In the present paper, the impurities introduced to form nMOSFET are boron, indium, arsenic, and phosphorus, while pMOSFET employed boron and arsenic. Boron, arsenic, and phosphorus were all retarded by STI stress as encountered in fitting the silicon MOSFET *I–V* data. Indium was not considered as a fitting variable because it was observed to be almost immobile during the thermal process, meaning that a dopant profile change due to mechanical stress would hardly be observed. As will be mentioned later, the nMOSFETs threshold voltage was observed to increase as the $X_{\rm active}$ value decreases. The subthreshold *I–V* with a low drain bias is strongly dependent on the accurate doping profile of the MOSFET shallow core region, which is mainly related to arsenic source/drain extension doping and boron halo doping. In high drain bias cases, the subthreshold *I–V* depends significantly on the deeper part of the MOSFET doping profile, which is related to phosphorus source/drain, indium halo, and boron halo tail doping profiles. As the gate length varies, the extent of the superposition of

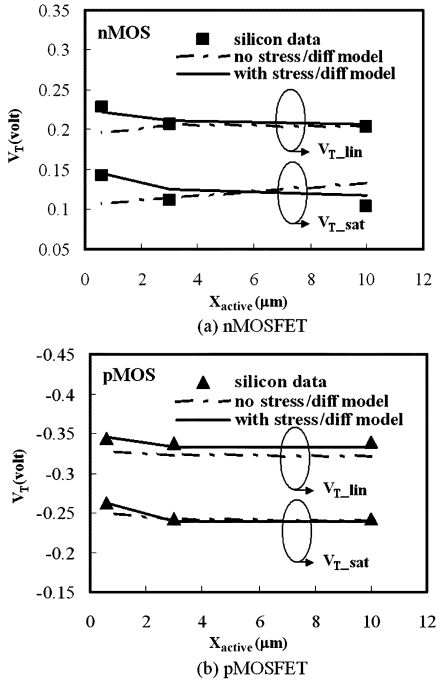

Fig. 10. Experimental and simulated threshold voltage dependence on X_{active} of (a) nMOSFET and (b) pMOSFET. NMOSFET threshold voltage V_T is more dependent on X_{active} than the p-type counterpart. Simulation with stress-dependent diffusion model is able to describe stress-induced V_T shift.

tilt-implanted halo doping varies accordingly. Moreover, as the substrate bias increases in magnitude, the depletion region further extends into the substrate from the source, channel and drain regions, considerably influencing subthreshold *I–V* characteristics. Thus, biasing the MOSFET substrate can serve as a means of verification for the stress-dependent diffusion model. Fig. 7 shows the depletion region boundaries of a 65-nm nMOSFET for low and high drain voltages.

After numerical iterations were completed, the effects of gate lengths, gate voltages, drain voltages, and substrate biases simultaneously matched with the nMOSFET subthreshold *I–V* data. This is sufficient to claim that the resulting dopant distributions for the whole device core region are correct. To assess the creditability of this model, device *I–V* simulations with and without VIDAESM were performed and compared. Fig. 8 shows the detailed *I–V* comparison for a small X_{active} MOSFET with and without VIDAESM. In the absence of VIDAESM, the simulation fails to correctly describe the *I–V* dependency on X_{active}. Fig. 9 displays a series of comparisons with measured gate voltage at different drain current levels for different combinations of gate lengths, active area sizes, drain voltages, and substrate biases. Remarkably, the extracted diffusion parameter set is able to reproduce all the silicon data well. The broad range of gate lengths, active areas, drain voltages and substrate biases employed in this experiment confirm that the VIDAESM model is indeed suited for modeling the mechanical stress effect on scaled MOSFETs. To further ensure the extracted parameter set also valid for pMOSFETs, threshold voltage dependence on X_{active} is simulated and compared with silicon data for both nMOSFETs and pMOSFETs. Fig. 10 shows the final results. It can be seen that the nMOSFET threshold voltage increases with decreasing X_{active} values while pMOSFET threshold voltage is relatively insensitive to X_{active}. The trends for both nMOSFETs and pMOSFETs are adequately described by the extracted parameter set.

TABLE I
IMPURITY ΔE_S VALUES EXTRACTED IN THE STUDY

Impurity	Boron	Phosphorus	Arsenic
ΔE_S(eV/volume shift ratio)	-7	-30	-14

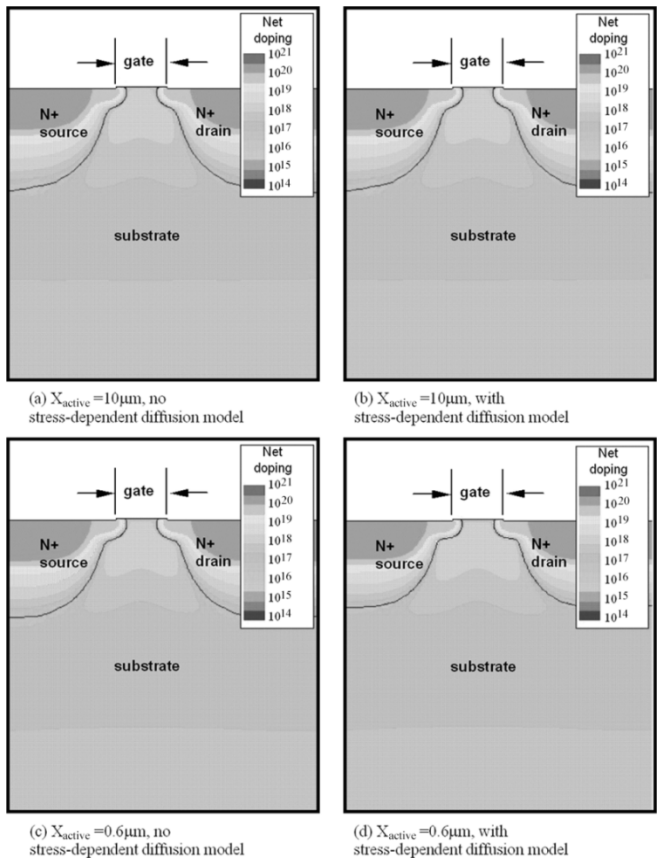

Fig. 11. Net doping contours for (a) $X_{\text{active}} = 10\ \mu$m, no stress-dependent model, (b) $X_{\text{active}} = 10\ \mu$m, with stress-dependent model, (c) $X_{\text{active}} = 0.6\ \mu$m, no stress-dependent model, and (d) $X_{\text{active}} = 0.6\ \mu$m, with stress-dependent model. For $X_{\text{active}} = 0.6\ \mu$m, the source/drain junction is significantly shallower in the MOSFET core region when the stress-dependent diffusion model is turned on. The gate length is 65 nm.

Finally, Table I lists the extracted ΔE_S values for all impurities involved. The ΔE_S for phosphorus is -30 eV per volume shift ratio and is largest among the impurities. The ΔE_S for arsenic is -14 eV per volume shift ratio, whereas the ΔE_S for boron is -7 eV. These coefficients confirm diffusion retardation by the compressive stress in pure silicon, excluding the Ge chemical effect in strained SiGe experiments. Fig. 11 illustrates the 2-D contour of the nMOSFET net doping concentration for a gate length of 65 nm. As shown in the figure, for $X_{\text{active}} = 10\ \mu$m, the dopant contours with and without the stress-dependent model are comparable, while the source/drain junction for $X_{\text{active}} = 0.6\ \mu$m is significantly shallower and effective gate length is longer in the MOSFET core region when the stress-dependent diffusion model is introduced. To more

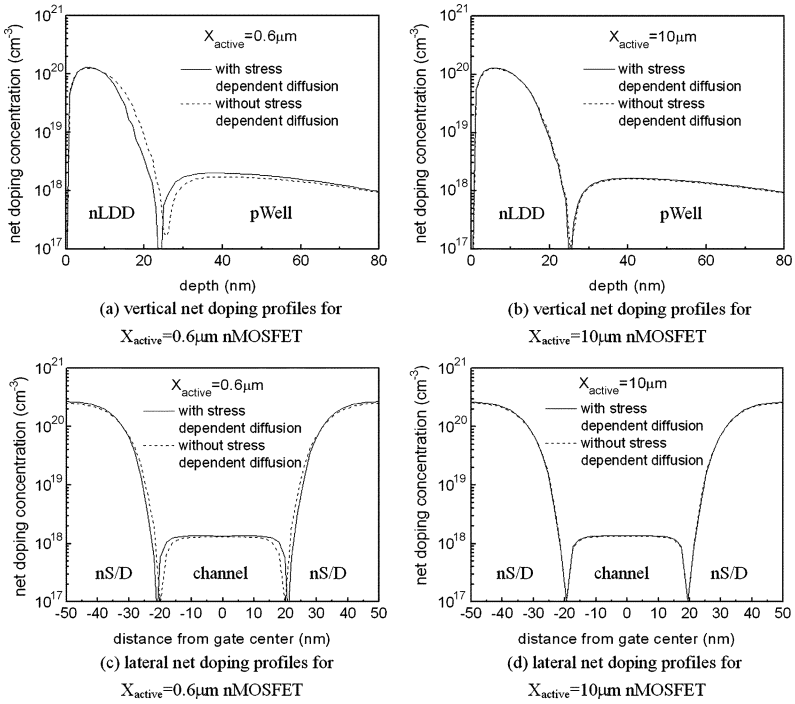

Fig. 12. Dopant profiles of (a) vertical direction for $X_{\rm active} = 0.6\ \mu$m nMOSFET, (b) vertical direction for $X_{\rm active} = 10\ \mu$m nMOSFET, (c) lateral direction for $X_{\rm active} = 0.6\ \mu$m nMOSFET, and (d) lateral direction for $X_{\rm active} = 0.6\ \mu$m nMOSFET. The vertical profiles are taken at gate edge and the lateral profiles are taken at 15-nm-deep cutlines of the device. Solid lines are simulation with stress-dependent diffusion model and dashed lines are without stress-dependent diffusion model. $X_{\rm active} = 0.6\ \mu$m with stress-dependent model device exhibits significant retardation of dopant diffusion.

clearly visualize the effect of the stress-dependent model, one can inspect the dopant profile along specific cutlines. Fig. 12 displays corresponding vertical and lateral doping profiles for a 65 nm gate length nMOSFET with $X_{\rm active}$ as a parameter. As can be seen, significant dopant diffusion retardation prevails at small $X_{\rm active}$ values and this explains an increase in threshold voltage as the $X_{\rm active}$ decreases.

IV. Conclusion

This paper has proposed an accurate stress-dependent dopant diffusion model. The model has been implemented into process and device simulators and has been validated by the extensive experimental data. A complete set of MOSFET devices with various gate lengths and active areas have been designed and fabricated from state-of-the-art sub-100-nm process for model verification. Retarded dopant diffusion for phosphorus, boron, and arsenic has been observed and explained by calibrated dopant profiles while accurately accounting for silicon threshold voltage changes and *I–V* behaviors. The major benefit of this model is that only a single set of physically based diffusion parameters is required to reproduce device subthreshold characteristics for different active areas, gate lengths, drain voltages, and substrate biases. The proposed model therefore can serves as a compact and accurate method for practically dealing with STI mechanical stress-dependent dopant diffusion in ultralarge scale devices.

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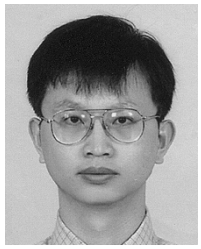

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