Fast Charging and High Efficiency Switching-Based Charger With Continuous Built-In Resistance Detection and Automatic Energy Deliver Control for Portable Electronics

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***Abstract*—The continuous built-in resistance detection (CBIRD) is proposed in the switching-based charger system to achieve fast charging. Corresponding to built-in resistance (BIR) variation of Li-ion battery and charging current limitation from input energy, the CBIRD dynamically adjusts the transition voltage at the constant current (CC) mode. As a result, the transition timing from CC mode to the constant voltage (CV) mode can be postponed. Rated large charging current and extended period in CC mode effectively reduce charging time. Besides, the proposed automatic energy deliver control (AEDC) technique considers both loading system and battery status simultaneously to manage charging current according to the loading system's requirement and input supply energy for high efficiency charging. The proposed switching-based charger system was fabricated in 0.25 μm CMOS process and occupied 3 mm² silicon area. The charger system can save up to 40% of charging time. The charger system achieves 87% of peak power efficiency at a rated 1 A charging current.**

***Index Terms*—Automatic energy deliver control (AEDC), charger system, constant current and constant voltage (CC and CV), continuous built-in resistor detector (CBIRD), fast charging, power delivery path, power management system, switching-based charger.**

I. Introduction

PORTABLE devices such as smart phones and tablets have become popular and ubiquitous. Battery-powered portable devices require multiple DC-DC converters to supply many different chipsets and functionalities. Fast and high-efficiency battery charging has become important to meet complex power-supply requirements. Thus, embedded power management systems (PMS) [1] are often demanded in portable devices to fulfill different power requirements, as shown in Fig. 1(a). An energy deliver controller in the PMS is used to arrange power paths to optimally distribute energy to each block. After that, multiple DC-DC converters convert different supplies for various functional blocks. A charger circuit manages the battery charging procedure. As a result, stable and continuous energy from the power supply and battery supports multiple DC-DC converters to provide adequate and distributive power to different functional blocks. Considering the design of charger systems, low drop-out (LDO) regulator-based or switching regulator-based structures are commonly used, as illustrated in Fig. 1(b). The LDO-based charger has the advantages of being ripple-free, having compact size and high accuracy, but suffers from low efficiency due to large drop-out voltage [2]–[8]. In contrast, the switching-based charger can guarantee high efficiency over a wide input and output voltage range [9]–[14] with the drawback of extra external components.

In portable appliances, the Lithium-ion (Li-ion) battery is the most common choice due to its small size, large capacity, and recharging ability [15]. Owing to the characteristics of Li-ion battery packs, the whole Li-ion battery charging system inherently has several parasitic resistances including contact resistance (R_{CONTACT}), fuse resistance (R_{FUSE}), PCB wire trace resistance (R_{PCB}) and cell in series resistance (R_{CELL}), as depicted in Fig. 2(a). All parasitic resistances can be collectively called the built-in resistance (BIR) R_{BIR}. In a Li-ion battery charger system, R_{BIR} may vary from 100 mΩ to 500 mΩ according to different types of the Li-ion battery and PCB layout. As well, the BIR has some influence on the charging process. A large charging current will result in a large voltage drop across the BIR. Therefore, this influence is called the BIR effect, which is related to the BIR value and the charging current as shown in (1):

$$V_{\mathrm{BIR}} = I_{\mathrm{charge}} \times R_{\mathrm{BIR}}. \tag{1}$$

Generally speaking, the standard charging procedure of Li-ion battery includes trickle current (TC) mode, constant-current (CC) mode, and constant-voltage (CV) mode [2], [6]. CC mode is the main charging procedure due to large rated charging current. Conventionally, the transition among different charging modes depends on the battery voltage V_{BAT}. When V_{BAT} reaches the voltage V_{FULL}, which is the transition voltage close to the full voltage of the battery, the charger changes the charging mode from CC mode to CV mode. In CV mode, the charging current will be reduced to

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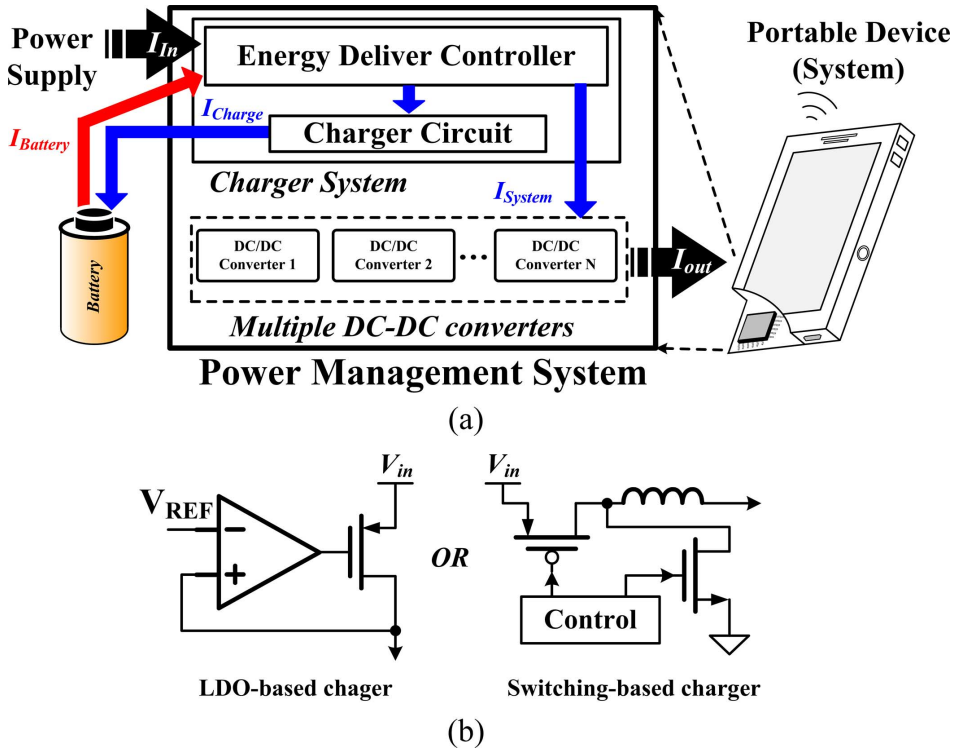


Fig. 1. (a) Architecture of the embedded power management system (PMS). (b) Charger structures in the PMS.

let the battery slowly achieve the rated voltage V_{FULL} and to prevent the battery from being overcharged. Fig. 2(b) depicts the charging profile including typical CC and CV modes under the BIR effect. During the charging procedure, the battery voltage V_{BAT} is the sum of the voltage across the BIR V_{BIR} and the voltage V_{BATO} which exactly represents the energy stored in the battery. However, the battery voltage can only be sensed on the point of V_{BAT}. Owing to the BIR effect, early transition time happens from CC mode to CV mode. Too early transition will cause a shortened period in CC mode and prolong the charging time. This is due to the charging current in CV mode is much smaller than that in CC mode. In other words, fast charging can be achieved if the duration in CC mode can be extended.

In order to determine a proper transition point, named as $V_{\mathrm{FULL,COMP}}$ in this paper, for fast charging, there are many previous works proposed to cancel the BIR effect by extending CC charging time [6]–[8], [16]. If the value of BIR with the information of charging current can be estimated, the voltage drop across the BIR can be determined. Thus, an adequate transition point from CC mode to CV mode can be precisely derived to extend the period of CC mode to get large energy and fast charging. By generating a compensated voltage $V_{\mathrm{FULL,COMP}}$ instead of the conventional transition voltage V_{FULL}, CC mode period is extended as shown in Fig. 2(b).

In [6] and [8], the BIR compensation method is designed for a LDO-based charger. The charger adjusts the charging current on the BIR detection sampling timing. According to the relationship between the charging current and the battery output voltage, the BIR information can be obtained. Prior arts for alleviating the BIR effect are done simply by one-time BIR detection in the charging procedure. Unfortunately, the BIR effect is temperature, voltage, and environment dependent. As shown in Fig. 3(a), the R_{BIR} in a Li-ion battery varies under different environmental conditions and especially at different temperatures. During the charging process, large current flows into the battery and causes the battery to heat up. The R_{BIR} is temperature dependent, therefore one-time detection may result in a wrong compensated value. The alleviation of BIR effect will not be obvious. More seriously, improperly compensated BIR effect may result in overcharging, even permanent damage to or explosion of the battery. In other words, one-time detection cannot handle such uncertain environmental variations during the charging process. Adaptive compensation for the R_{BIR} tracks the variation of temperature and achieves precise compensation, as depicted in Fig. 3(b). Thus, real-time detection of the BIR is needed to accurately alleviate the BIR effect [9].

In this paper, a switching-based charger system with the proposed automatic energy delivery control (AEDC) is presented for fast charging and high efficiency. The AEDC is designed to control energy delivery between the input energy, multiple DC-DC converters, and the charger system. The proposed charger system automatically senses the loading system's power consumption. The AEDC supplies the input power to the loading system first and gives the rest of the available power to charge the battery. The proposed continuous BIR detector (CBIRD) dynamically monitors the BIR value to determine the proper transition point, $V_{\mathrm{FULL,COMP}}$[9]. In the whole charging process, the CBIRD will adjust the transition point in real time in case of any small variation in the BIR to achieve fast and safe charging.

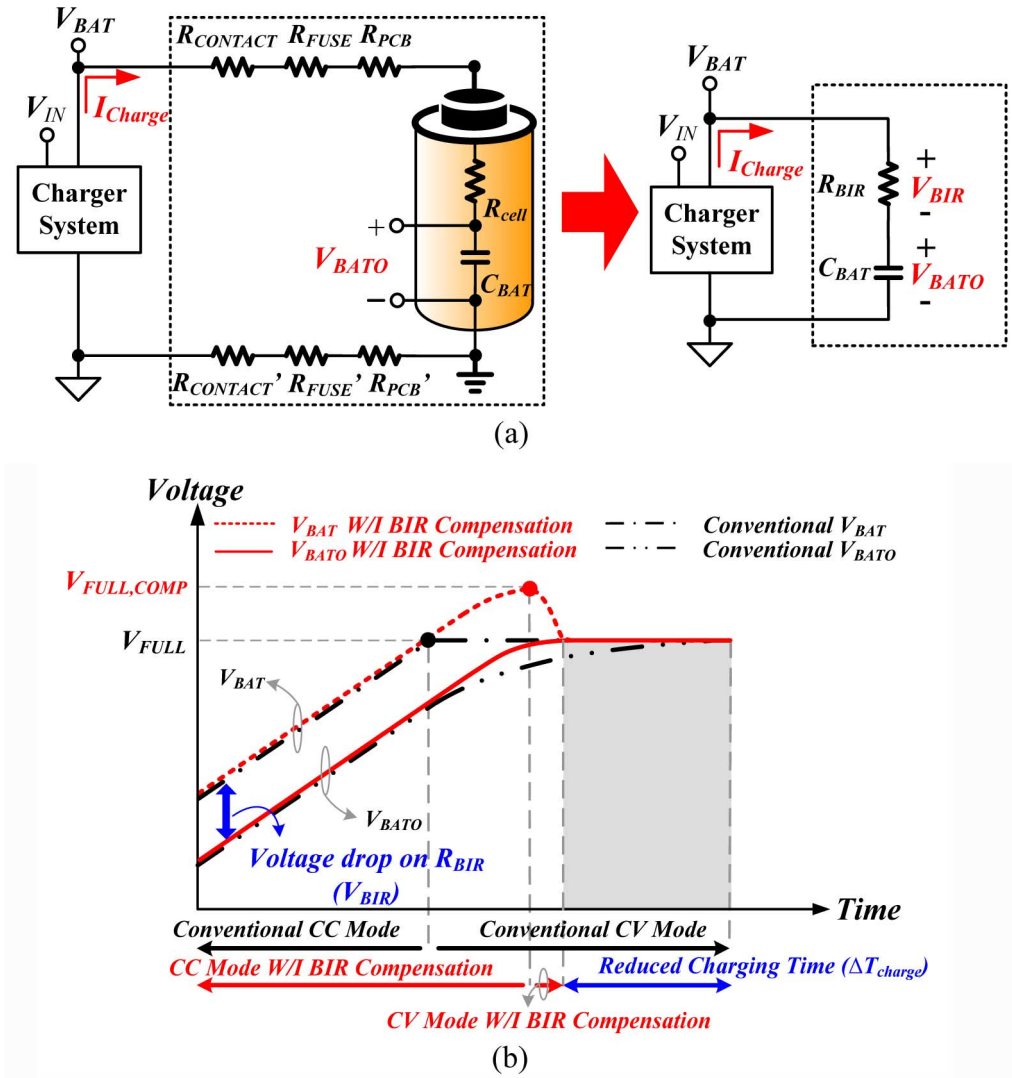


Fig. 2. (a) Equivalent parasitic resistances cause the BIR in the charger system. (b) Charging profile with the BIR effect.

II. Structure of Proposed Charger System With AEDC

The architecture [13]–[15], [17] of the switching-based charger system includes the AEDC and the charger circuit shown in Fig. 4. The delivery paths in the AEDC is composed of the power switches, M_{S1}–M_{S5}. The portable system can be supplied by batteries or external power sources (adaptor, Universal Serial Bus (USB), etc.). According to different power conditions, the AEDC must decide a suitable power delivery path through the power stage to balance the input energy and system loading. If external power sources have enough energy to drive the loading system, in the meantime, battery charging can proceed to rated charging. On the other hand, if the energy source is not sufficient to satisfy both charging and loading requirements, the charging process varies with the system loading. The BIR effect should be alleviated by the proposed CBIRD in the charger circuit adaptively.

To satisfy all the power conditions, there are four operation states in the AEDC. These four operation states are pure charge state, direct supply state, plug off state, and charge and supply (CAS) state. Fig. 5 shows the power path in each state. Each state corresponds to different input and output relationships. In general, the input power source has its maximum power limitation. Thus, the first priority for the charging system is to keep the sequent system working normally. According to constraints of input power and system loading information, the energy delivery control circuit in the AEDC will generate gate control signals to inform the power stage and the charger system to execute a suitable power state. The charger circuit will collaborate with the AEDC circuit and simultaneously adjust the charging current for battery charging. Detailed descriptions of each operation state are shown as follows.

A. Pure Charge State

When the loading system is shut down or disconnected to the charger system, the only loading is the battery. The energy from the input power source completely delivers to the battery and constitutes a pure charging state. In the meantime, the charging current is limited by the battery's rated charging current.

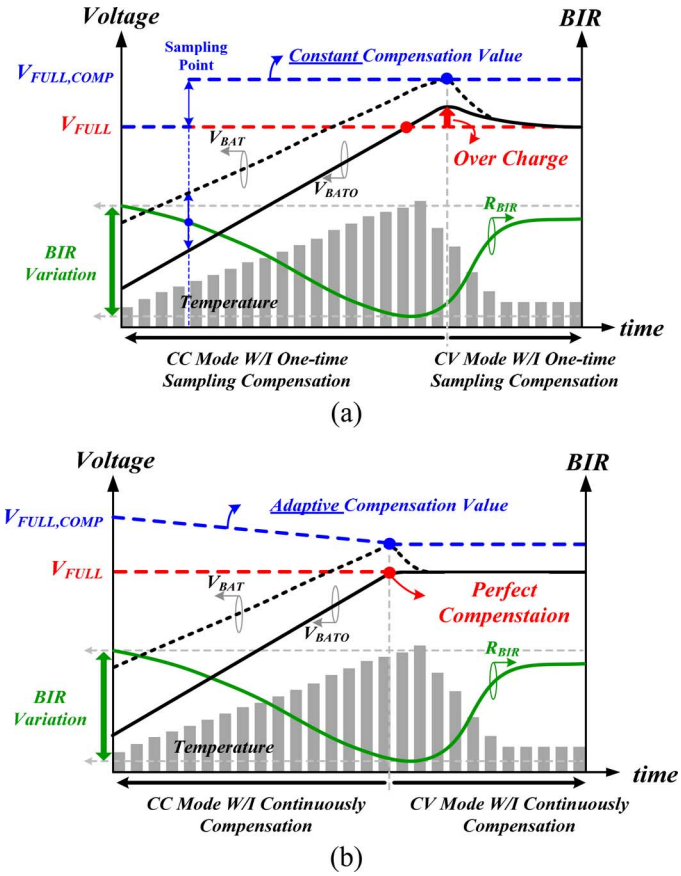


Fig. 3. BIR effect due to BIR variation. (a) One-time BIR detection if the BIR changes. (b) Real-time BIR detection if the BIR changes.

B. Direct Supply State

When the input power source connects to the charger system, the loading system can work normally even if the battery is removed. That is, the input power source can provide energy directly to the system. This condition may also happen when the battery is fully charged. The charger system keeps monitoring battery status. If the battery connects to the charger system again or the battery needs energy, the charging state will quickly switch to the CAS state.

C. Plug Off State

The portable system takes the battery as the power supply once the input power source is disconnected. Thus, the charger system needs to provide a power delivery path from the battery to the loading system. Moreover, the battery should be disconnected from the loading system once the battery voltage reaches its lower bound to protect the battery from being overdischarged.

D. CAS State

The charging function and normal system supplying operation can work at the same time if the energy provided by the input power source is larger than that needed from the loading system. Here, the maximum power provided by the input power source is defined as $P_{\mathrm{IN,max}}$, the power consumption of the loading system is P_{system}, and the battery charging power is P_{charge}. This state can be divided into two cases according to the relationship among $P_{\mathrm{IN,\,max}}$, P_{system} and P_{charge}. Firstly, if $P_{\mathrm{IN,\,max}} \geq P_{\mathrm{system}} + P_{\mathrm{charge}}$, the input power source can afford total power that is consumed by the loading system and the battery charging. Contrarily, if the total power consumption exceeds the maximum power, that is $P_{\mathrm{IN,max}} < P_{\mathrm{system}} + P_{\mathrm{charge}}$, the system's power consumption will have a higher priority than the charging function. The proposed CAS state reduces the battery charging current to satisfy the power demand for maintaining the loading system operation. Thus, the input power source can avoid being overloaded by adjusting the battery charging power from P_{charge} to P'_{charge}. That is, $P_{\mathrm{IN,max}} = P_{\mathrm{system}} + P'_{\mathrm{charge}}$. In other words, the battery charging current becomes I'_{charge} determined by the CAS state as expressed in (2):

$$I'_{\mathrm{charge}} = \left(\frac{V_{\mathrm{IN}}}{V_{\mathrm{BAT}}}\right) \cdot \left(I_{\mathrm{IN,max}} - I_{\mathrm{system}}\right). \tag{2}$$

In Fig. 6, the CAS state shows that the charging current is limited correspondingly to the I_{system}. That is to say, the charger system is not able to charge the battery with the rated current. The charging current will be a distributed result. The AEDC has to control the charging current carefully to extract the remaining power from $P_{\mathrm{IN,max}}$. Without affecting the loading system's requirement, the AEDC keeps I_{IN} below its maximum value.

In the proposed charger circuit of Fig. 4, there are three parallel loops: CC loop, CV loop, and CAS loop. These three loops will correspond to different charging operation modes. In the CC mode, the battery should be charged by a constant current. Thus, the CC loop consisting of a current sensor and an error amplifier (EA), which is the EA_CC, to adjust I_{charge} by the predefined current setting value of $V_{\mathrm{CC,SET}}$. The CV loop senses the V_{BAT} information by feedback resistors R_{FB1} and R_{FB2}. Conventionally, when V_{FB} equals V_{CV}, which represents a divided full voltage of the battery as shown in (3), the charger circuit enters CV mode.

$$V_{\mathrm{CV}} = \frac{R_{\mathrm{FB2}}}{R_{\mathrm{FB1}} + R_{\mathrm{FB2}}} V_{\mathrm{FULL}}. \tag{3}$$

However, under the BIR effect compensation, V_{CV} will be modified to $V_{\mathrm{CV,COMP}}$ by the CBIRD circuit. The CBIRD senses the V_{BAT} to calculate an appropriate $V_{\mathrm{CV,COMP}}$ to eliminate the BIR effect in the charger system. The CAS loop gets the supply current I_{IN} from the supply current sensor to limit the charging current. The reference voltage $V_{\mathrm{CAS,SET}}$ represents the maximum I_{IN}. When the loading system's current I_{system} rises and reaches the upper bound of I_{IN}, the CAS loop will start operation and control the total I_{IN} by adjusting the charging current I_{charge}. In the operation of the charger system, only one of the loops will activate at one time. Hence, the smooth transition loop selector (STLS) can change the loop smoothly during the transition among three loops [10]. No matter which loop dominates the charger system, only one shared EA with on-chip compensator ensures stability among all loops so that the extra components are reduced. Finally, the feedback signal generated by the EA is sent to the comparator to determine the duty. Logic circuits and driver block generate

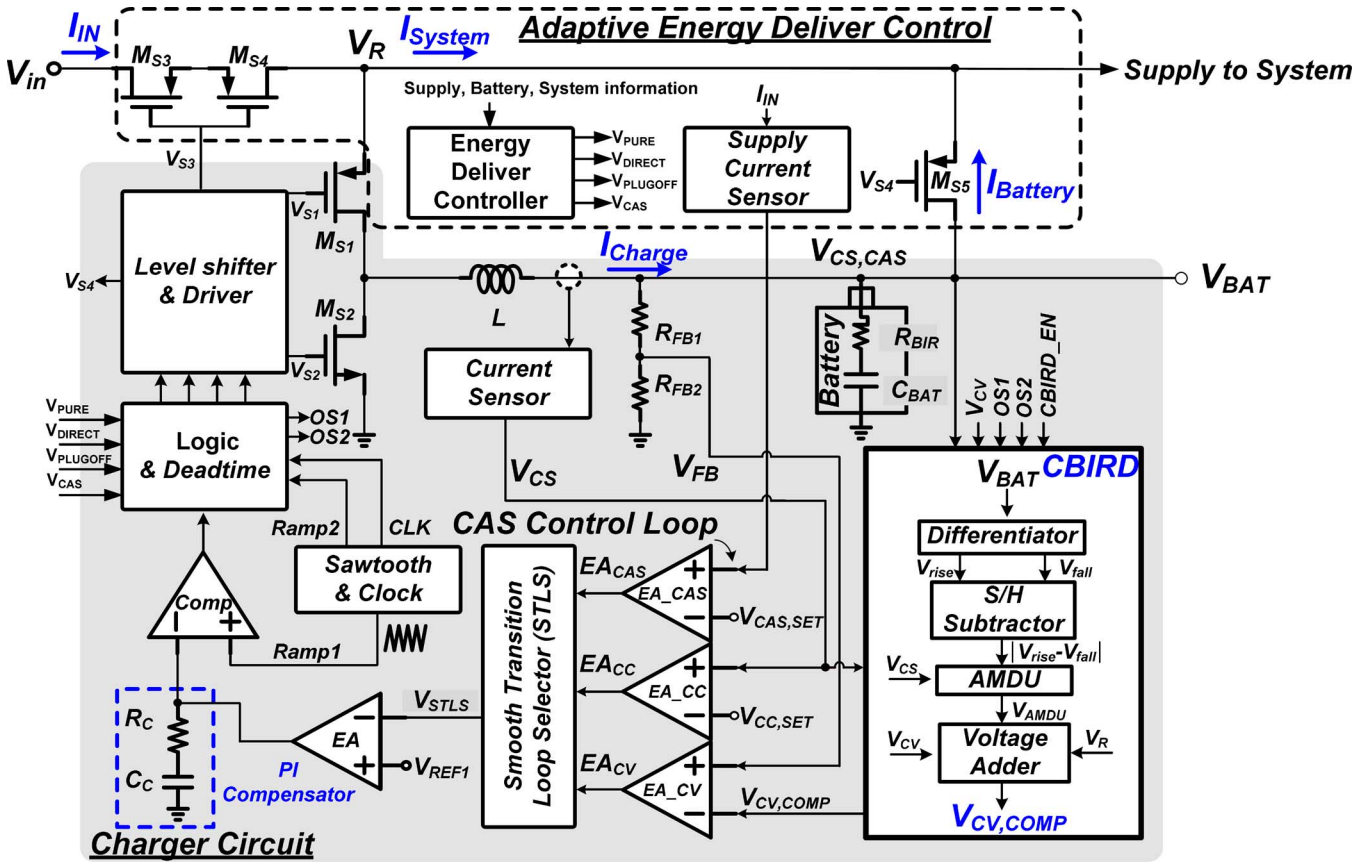


Fig. 4. Proposed switching-based charger system with AEDC and CBIRD.

the driving signals for power MOSFETs to avoid shoot-through current.

In the CAS state, Fig. 6, the $I_{\rm charge}$ is unpredictable due to the $I_{\rm system}$ varying with the loading system. This variation may cause the compensation of BIR effect to be more complicated during the charging process. To compensate BIR effect, the charger system should also take the charging current information into consideration. Conventional one-time detection methods, as shown in Fig. 7(a), will lead to wrong $V_{\rm CV,COMP}$ when the charger operates in the CAS state [6]–[8], [16]. It results in overcharge, even permanent damage of the battery. The charging current variation during the CAS mode and the BIR variation under different environmental conditions makes it necessary to adaptively adjust the compensation voltage $V_{\rm CV,COMP}$. This proposed CBIRD gathers the information of the recent charging current and continuously monitors the BIR value to generate an accurate and adaptively compensated $V_{\rm FULL,COMP}$. Fig. 7(b) shows that $V_{\rm FULL,COMP}$ follows the variation of the charging current. An optimal value can be achieved to accurately compensate the BIR effect and shorten the charging time for a Li-ion battery.

III. Operation and Circuit Implementation of Proposed CBIRD

A. CBIRD Operation

From the characteristic of the switching-based converter, as shown in Fig. 8, the output voltage $V_{\rm BAT}$ is composed of two parts, DC voltage and AC ripple. Through the mathematical derivation, $V_{\rm BAT}$ can be expressed in (4):

$$V_{\rm BAT} = V_{\rm DC} + i_{\rm Charge}R_{\rm BIR} + \frac{1}{\rm C_{BAT}}\int i_{\rm Charge}dt. \quad (4)$$

The ripple is generated by the inductor current $i_{\rm charge}$ flowing through the battery including $R_{\rm BIR}$ and $C_{\rm BAT}$. Since the battery's equivalent capacitor $C_{\rm BAT}$ is large enough, the voltage ripple on $C_{\rm BAT}$ can be ignored. The output voltage ripple on the battery can be approximately seen as the $\Delta V_{\rm CV}$ in (5), which is determined by the BIR under the inductor current $i_{\rm charge}$.

$$\Delta V_{\rm CV} = i_{\rm Charge}R_{\rm BIR}. \quad (5)$$

To compensate the BIR effect, $\Delta V_{\rm CV}$ should be derived first. Then, the compensated $V_{\rm CV,COMP}$ can be generated continuously. The proposed detection and compensation method will not interrupt the charging process compared to prior arts [6]–[8]. The proposed CBIRD method derives $\Delta V_{\rm CV}$ from the $V_{\rm BAT}$'s AC ripple which will not affect the charging process. The continuous detection can achieve adaptive compensation.

The switching-based charger operates similar to a continuous conduction mode buck converter [17]. Two inductor current slopes in charging and discharging phases constitute AC voltage ripple at $V_{\rm BAT}$, which can be used to disclose the information of BIR. By differentiation, the DC part of $V_{\rm BAT}$ will be eliminated and the slope of voltage ripple across BIR could be derived as (6) where the V_R indicates the voltage value after the

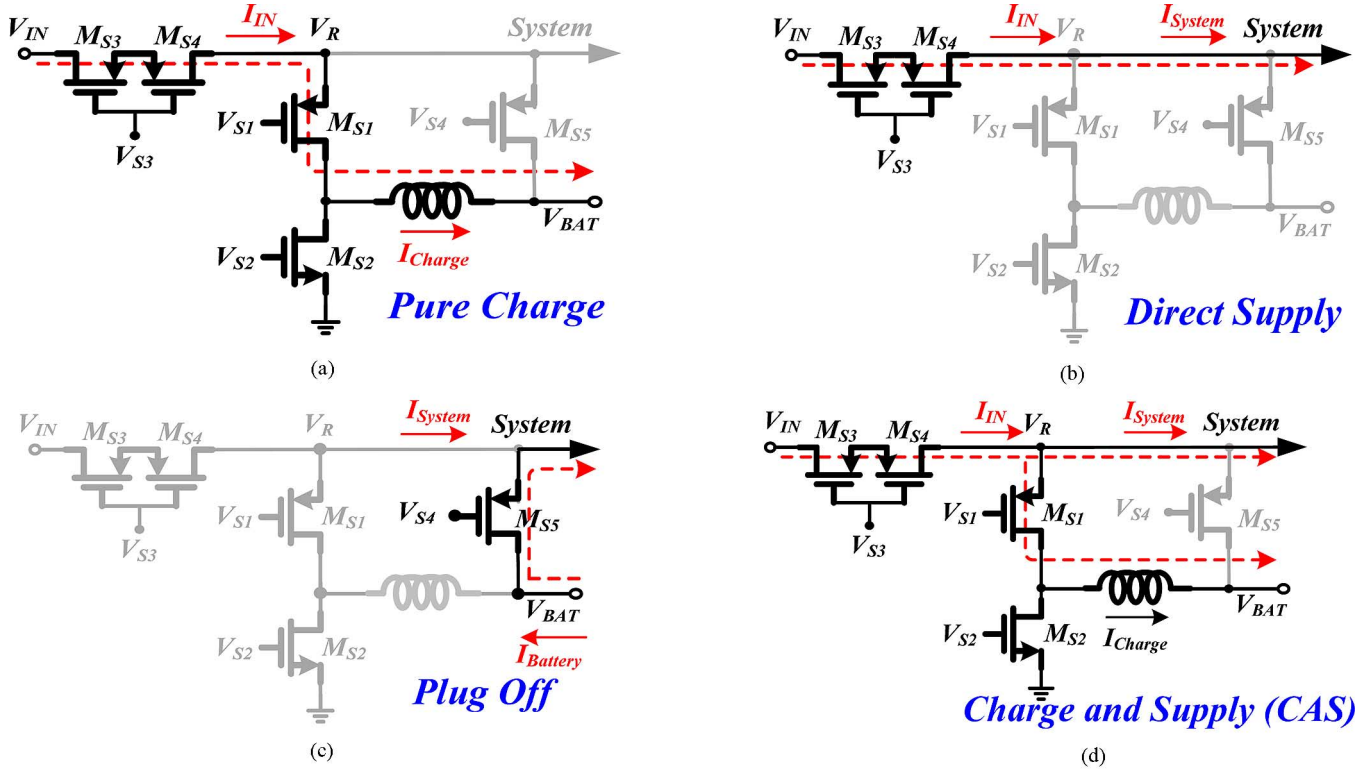


Fig. 5. Power delivery paths in the proposed charger system. (a) Pure charge state. (b) Direct supply state. (c) Plug off state. (d) CAS state.

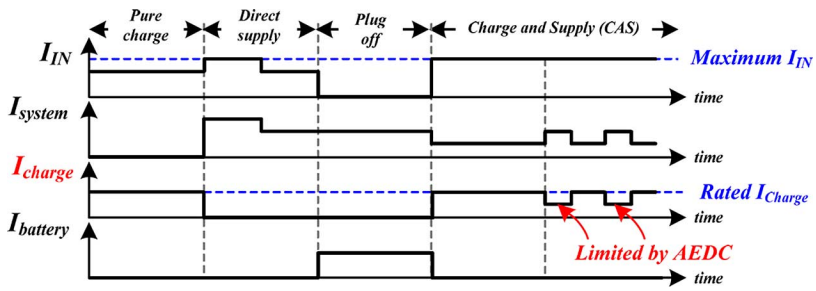


Fig. 6. Current delivery condition in different operation states.

input voltage $V_{\rm IN}$ across two cascading power switches $M_{\rm S3}$ and $M_{\rm S4}$ as shown in Fig. 4.

$$\begin{aligned} V_{\rm rise} &= K_1 \frac{dV_{\rm BAT}}{dt} \\ &= K_1 R_{\rm BIR} \frac{V_R - V_{\rm BAT}}{L} \text{ in charging phase,} \\ V_{\rm fall} &= K_1 \frac{dV_{\rm BAT}}{dt} \\ &= -K_1 R_{\rm BIR} \frac{V_{\rm BAT}}{L} \text{ in discharging phase.} \end{aligned} \quad (6)$$

$V_{\rm rise}$ and $V_{\rm fall}$ are the inductor current slopes in the charging and discharging phases, respectively. K_1 is the coefficient induced by the differentiator circuit. The difference between $V_{\rm rise}$ and $V_{\rm fall}$ includes the information of $R_{\rm BIR}$ as shown in (7):

$$|V_{\rm rise} - V_{\rm fall}| = K_1 R_{\rm BIR} \frac{V_R}{L}. \quad (7)$$

Moreover, the charging current $I_{\rm charge}$ can be found by the current sense circuit in Fig. 4 to derive $\Delta V_{\rm CV}$. The sensing ratio is designed as K_2 in this work. That is, $V_{\rm CS} = K_2 * I_{\rm charge}$. Thus, the function of $\Delta V_{\rm CV}$ can be derived by (8) through the product of the current sense signal $V_{\rm CS}$ and $|V_{\rm rise} - V_{\rm fall}|$. Owing to the constant value of K, $V_{\rm R}$, and L, the $\Delta V_{\rm CV}$ can be precisely calculated through the estimation of $V_{\rm CS}$, $V_{\rm rise}$, and $V_{\rm fall}$. Adding $\Delta V_{\rm CV}$ with a scaling factor $R_{\rm FB2}/(R_{\rm FB1} + R_{\rm FB2})$ to the original $V_{\rm CV}$, the precise transition point $V_{\rm CV,COMP}$ is derived as (9).

$$\begin{aligned} V_{\rm CS} \times |V_{\rm rise} - V_{\rm fall}| &= K_2 \cdot I_{\rm charge} \times K_1 \cdot R_{\rm BIR} \cdot \frac{V_{\rm R}}{L} \\ &= \Delta V_{\rm CV} \times K \frac{V_{\rm R}}{L} \\ \text{where } \Delta V_{\rm CV} &= I_{\rm charge} \cdot R_{\rm BIR} \text{ and } K = K_1 \cdot K_2 \end{aligned} \quad (8)$$

$$\begin{aligned} V_{\rm CV,COMP} &= \frac{R_{\rm FB2}}{R_{\rm FB1} + R_{\rm FB2}} \cdot V_{\rm FULL,COMP} \\ &= \frac{R_{\rm FB2}}{R_{\rm FB1} + R_{\rm FB2}} \cdot (V_{\rm FULL} + \Delta V_{\rm CV}) \\ &= V_{\rm CV} + \frac{R_{\rm FB2}}{R_{\rm FB1} + R_{\rm FB2}} \\ &\quad \times I_{\rm charge} \cdot R_{\rm BIR}. \end{aligned} \quad (9)$$

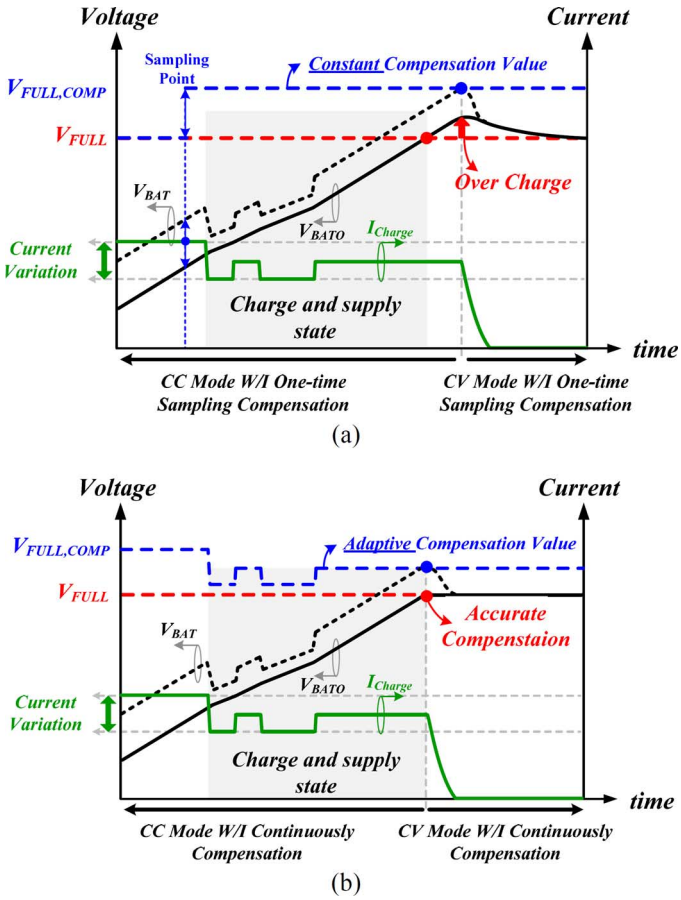


Fig. 7. BIR effect due to charging current variation. (a) One-time BIR detection versus charging current variation. (b) Continuous BIR detection versus charging current variation.

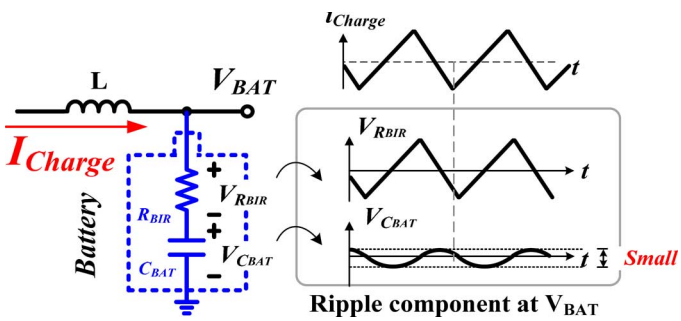


Fig. 8. Composition of the battery voltage ripple.

The proposed CBIRD circuit is designed to implement equations from (6)–(9). Fig. 9 depicts the circuit flow to realize the CBIRD function. It includes the differentiator, the sample-and-hold (S/H) subtractor, the analog multiplication–division unit (AMDU), and the voltage adder. First, the differentiator is used to obtain the AC ripple of $V_{\rm BAT}$ to get $V_{\rm rise}$ and $V_{\rm fall}$ in (6) after filtering out the DC voltage. The S/H subtractor samples $V_{\rm rise}$ and $V_{\rm fall}$ and holds their difference value in (7). Then, through the AMDU circuit, the multiplication function multiplies $V_{\rm CS}$ with $|V_{\rm rise} - V_{\rm fall}|$ and the division function derives $\Delta V_{\rm CV}$ in (8). Through the voltage adder, $\Delta V_{\rm CV}$ will be scaled down by the voltage divider ratio and then added to $V_{\rm CV}$ to accomplish $V_{\rm CV,COMP}$ in (9). Finally, $V_{\rm CV,COMP}$ is used as the reference

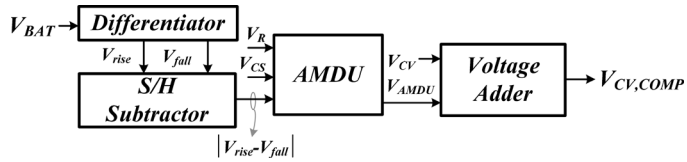


Fig. 9. Implementation of the CBIRD Circuit.

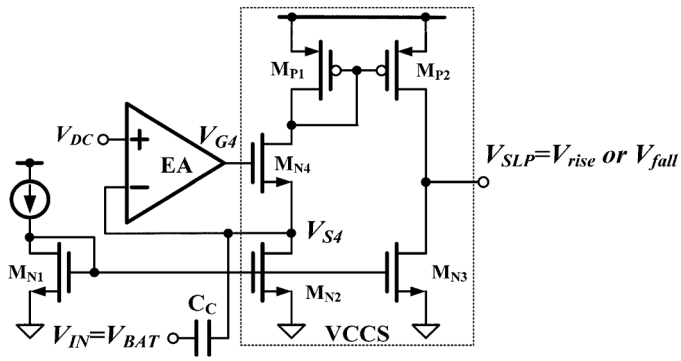


Fig. 10. Proposed differentiator circuit.

voltage to dynamically adjust the mode transition point for compensating the BIR effect.

B. CBIRD Circuit Implementation

1) Differentiator: The differentiator in Fig. 10 uses the coupling capacitor $C_{\rm C}$ to block the DC components and to get the AC information from $V_{\rm BAT}$. The EA and the transistor $M_{\rm N4}$ maintain a DC level at the input node of $V_{\rm S4}$. Therefore, only AC voltage information is converted to a current signal by the voltage-control current source (VCCS) circuit. The rising and falling voltage ripple information, $V_{\rm rise}$ and $V_{\rm fall}$, can be got at the node of $V_{\rm SLP}$. Corresponding to the charging and discharging phases, the differentiator outputs $V_{\rm rise}$ and $V_{\rm fall}$, respectively. $V_{\rm rise}$ and $V_{\rm fall}$ follow the equations in (6). Because the differentiator needs settling time to ensure the $V_{\rm SLP}$ changes its value between $V_{\rm rise}$ and $V_{\rm fall}$. Thus, the sampling timing of the S/H subtractor should match the operation of the differentiator to get correct and precise $V_{\rm rise}$ and $V_{\rm fall}$. The common mode level of $V_{\rm SLP}$ may vary due to process, voltage and temperature (PVT) variation. However, the common level will not affect differentiation result since only the difference between $V_{\rm rise}$ and $V_{\rm fall}$ will be sampled and calculated as the BIR information.

2) Sample-and-Hold (S/H) Subtractor: In Fig. 11, the S/H subtractor circuit samples the differentiator's outputs in charging and discharging phases. By selecting the sampling path during charging and discharging phases, the subtraction function in (7) can simultaneously be achieved. As shown in Fig. 12, the sampling clocks, *OS1* and *OS2* control the MOSFETs $M_{\rm N1}$ to $M_{\rm N4}$ to sample the $V_{\rm SLP}$. In the charging phase, $M_{\rm N1}$ and $M_{\rm N2}$ turn on and the $V_{\rm rise}$ is stored in the $C_{\rm FLY}$. In the discharging phase, $M_{\rm N3}$ and $M_{\rm N4}$ turn on and the C_{OUT} stores the value $V_{\rm fall}$–$V_{\rm rise}$, which is equal to $|V_{\rm rise}$–$V_{\rm fall}|$ according to the Kirchhoff voltage law (KVL).

3) Analog Multiplication-Division Unit (AMDU): Fig. 13(a) shows the basic structure and concept of the proposed AMDU

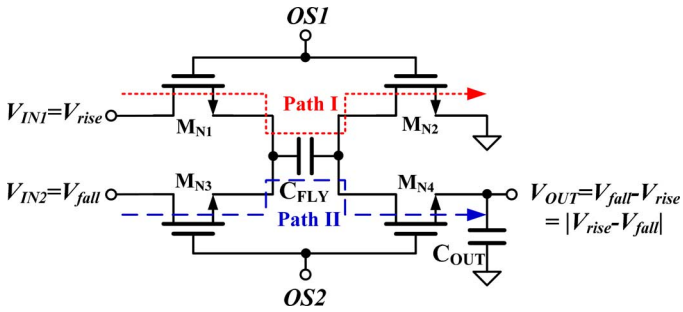


Fig. 11. Proposed S/H subtractor circuit.

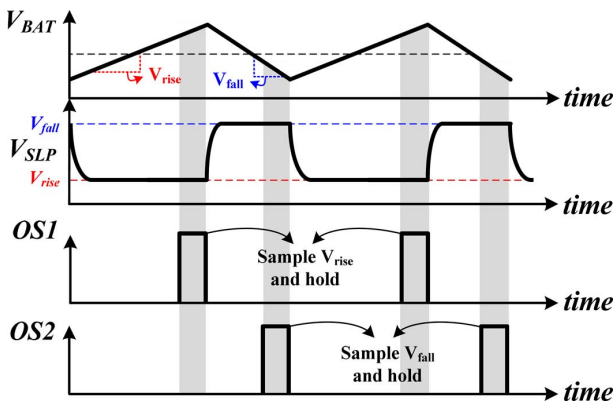


Fig. 12. Timing diagram for S/H subtractor circuit.

circuit, which is composed of two V-to-I converters (*V-to-*I_1 converter and *V-to-*I_2 converter), one comparator, and one switch $S_{\rm SW}$. The *V-to-*I_1 converter translates $V_{\rm IN1}$ to $K_1 I_1$ to charge C_1 with the charging slope m_1 in (10). Similarly, the *V-to-*I_2 converter translates $V_{\rm IN2}$ to $K_2 I_2$ to charge C_2 with the charging slope m_2 in (10):

$$m_1 = \frac{I_1}{\rm C_1} = \frac{K_1 V_{\rm IN1}}{\rm C_1} \text{ and } m_2 = \frac{I_2}{\rm C_2} = \frac{K_2 V_{\rm IN2}}{\rm C_2}. \quad (10)$$

K_1 and K_2 are the coefficients for the *V-to-*I_1 and the *V-to-*I_2 converters, respectively. Once the voltage storing in C_1 approaches to the value of $V_{\rm IN3}$, the output of the comparator becomes low to turn off the switch $S_{\rm SW}$. Hence, it can obtain a charging time Δt, which is related to $V_{\rm IN1}$ and $V_{\rm IN3}$, to realize division function as described in (11). Consequently, the charging time of C_2 can be determined by Δt. Finally, the $V_{\rm OUT}$ of the AMDU can be calculated by (12) to complete the function. The timing diagram of the AMDU is depicted in Fig. 13(b).

$$\Delta t = \frac{V_{\rm IN3}}{\rm M_1} = \frac{\rm C_1 V_{IN3}}{K_1 V_{\rm IN1}}, \quad (11)$$

$$V_{OUT} = m_2 \times \Delta t = \left(\frac{K_2 V_{\rm IN2}}{\rm C_2}\right) \times \left(\frac{\rm C_1 V_{IN3}}{K_1 V_{\rm IN1}}\right) = \frac{V_{\rm IN2} \times V_{\rm IN3}}{V_{\rm IN1}}. \quad (12)$$

The AMDU circuit is illustrated in Fig. 14. The cascode current mirror is used to avoid channel length modulation for ensuring accuracy. S_1 and S_2 are reset switches to reset the voltage on the capacitors after each calculation. By setting the same value and careful layout matching for the two V-to-I converters and capacitors, $C_1 = C_2$ and $K_1 = K_2$ can be guaranteed. The output voltage of the AMDU circuit is simply composed of $V_{\rm IN1}$, $V_{\rm IN2}$ and $V_{\rm IN3}$ as shown in (12). Consequently, substituting the parameters $V_{\rm CS}$, $|V_{\rm rise} - V_{\rm fall}|$ and V_R to $V_{\rm IN1}$, $V_{\rm IN2}$ and $V_{\rm IN3}$ in (12) can derive the $V_{\rm AMDU}$ in (13). To get $\Delta V_{\rm CV}$, $V_{\rm AMDU}$ should be modified by the voltage divide ratio through the voltage adder to correctly reflect the BIR effect.

$$V_{\rm AMDU} = V_{\rm CS} \times \frac{(|V_{\rm rise} - V_{\rm fall}|)}{V_R} = \Delta V_{\rm CV} \times \frac{K}{L}. \quad (13)$$

4) Voltage Adder: The voltage adder is depicted in Fig. 15, which includes a unit-gain buffer, a V-to-I circuit, and a cascode current mirror. The unit-gain buffer EA2 is used to keep the $V_{\rm CV}$. The V-to-I circuit transfers the $V_{\rm AMDU}$ to a current signal for easily signal processing. After that, the current signal is converted back a voltage signal across the resistor R_2 through the current mirror. R_1 and R_2 are used to provide a scaling ratio β as shown in (14):

$$V_{\rm CV,COMP} = V_{\rm CV} + \beta V_{\rm AMDU} = V_{\rm CV} + \Delta V_{\rm CV} \quad \text{where } \beta = \frac{R_2}{R_1} = \frac{R_{\rm FB2}}{R_{\rm FB1} + R_{\rm FB2}} \cdot \frac{L}{K}. \quad (14)$$

The relationship between the voltage divider, the inductor value, and the constant K in (8) can be established by setting the value of β, which can be adjusted by tuning the value of R_2 through 4-bit calibration digital codes to get a precise result. For the unavoidable mismatch on circuits, a trimming process is added to our design for getting an improved performance. In the beginning of the system operation, a known ESR value is used to adjust the value of the I-to-V resistor at output of voltage adder. Thus, non-ideal effects can be effectively eliminated. Besides, due to large difference between V_X and $V_{\rm CV,COMP}$, the cascode current mirror, $M_{\rm P1}$–$M_{\rm P4}$ is used to avoid channel-length modulation and ensure high accuracy in this operation. Finally, the voltage adder implements (14) and generates the compensated value $V_{\rm CV,COMP}$. The $V_{\rm CV,COMP}$ will be used as a new reference voltage for the charger transiting from CC mode to CV mode.

The BIR compensation shortens the charging time but may induce a stability issue about the transition between CC mode and CV mode. Most prior arts [6]–[8] did not discuss this issue, which is related to the releasing of $\Delta V_{\rm CV}$. When the charging mode enters CV mode, $\Delta V_{\rm CV}$ should be removed from $V_{\rm CV,COMP}$. Sudden change of the transition voltage results in fierce transition, or even oscillation among different charging modes. With the proposed CBIRD, $\Delta V_{\rm CV}$ releases smoothly and appropriately. According to (9), $\Delta V_{\rm CV}$ includes the information of charging current. Once the charger system enters CV mode, the charging current $I_{\rm charge}$ is gradually reduced by the CV loop regulation. Therefore, the $\Delta V_{\rm CV}$ smoothly decreases with the decreasing inductor current so as the $V_{\rm CV,COMP}$. Hence, smooth transition from CC mode to CV mode can be achieved.

IV. Frequency Response

In frequency response analysis, since there are three independent loops, CC, CV, and CAS loop, each loop should be analyzed separately. It can be said that the whole system is stable

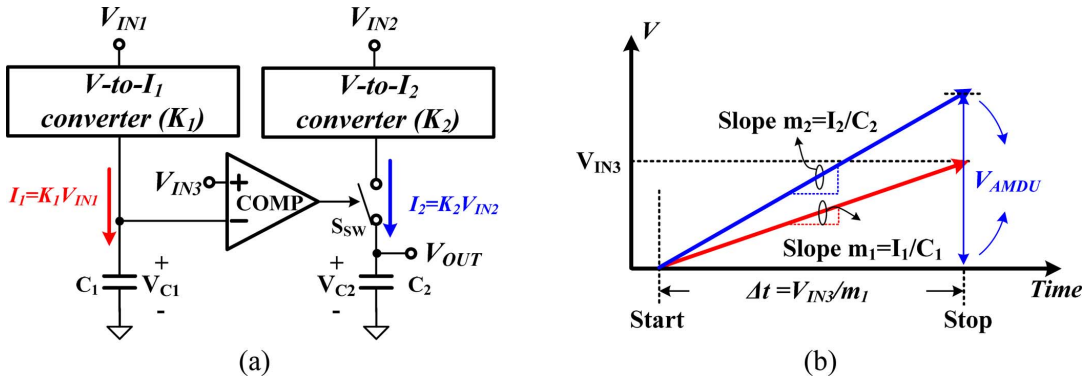


Fig. 13. (a) Concept of the proposed AMDU circuit. (b) Timing diagram of the AMDU circuit.

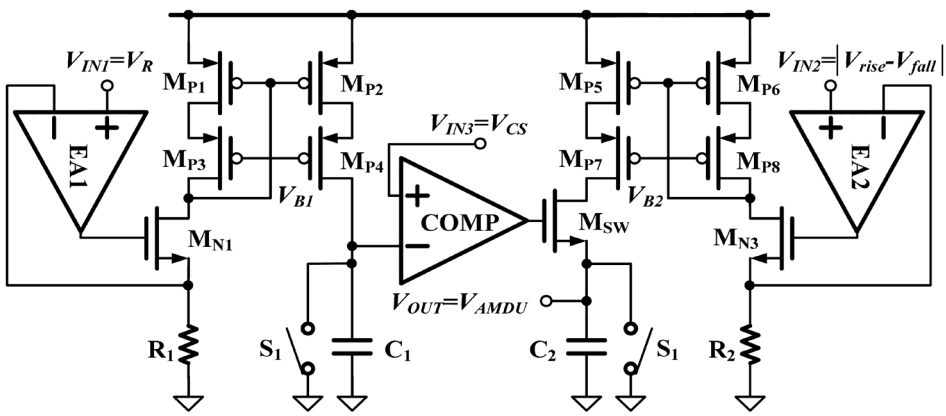


Fig. 14. Proposed AMDU circuit.

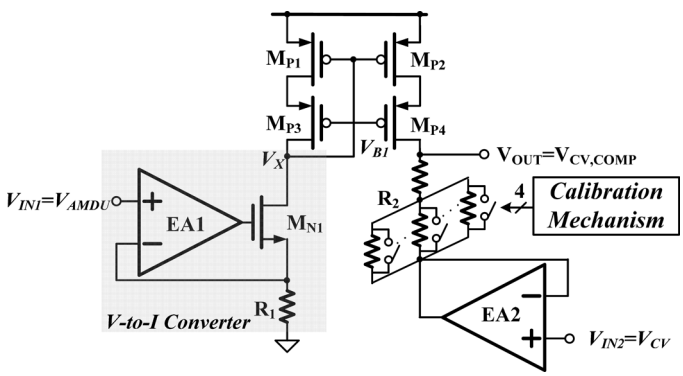


Fig. 15. Proposed voltage adder circuit.

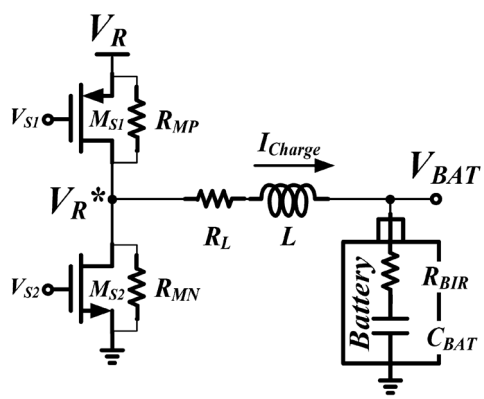


Fig. 16. Modeling of the power stage of the proposed switching-based charger.

if each individual loop is stable. It is important to ensure the charger is stable in each charging mode.

The analysis of the three loops is based on the modeling of a buck converter. The modeling of power stage is shown in Fig. 16 [17]. However, the output loads in the charger system are different from that of conventional buck converter. That is to say, the resistive load is replaced by the battery which is composed of one equivalent large output capacitance $C_{\rm BAT}$ and the BIR in series. Owing to large $C_{\rm BAT}$, the battery can be seen as a fixed voltage source in an AC modeling. Three loops of the charger system can be modeled as shown in Fig. 17 and the model parameters are listed in Table I. The power stage of the charger can be modeled as a one-pole system, $\Delta(s)$. To increase stability of the charger, the proportional–integral (PI) compensator with the transfer function $G_{\rm C}(s)$ is utilized [17]. The m is the divided ratio of the feedback resistors. $CS_{\rm CC}(s)$ and $CS_{\rm CAS}(s)$ represent the transfer function of the current sensing circuit in CC mode and the CAS mode, respectively. $1/V_{\rm M}$ is the transfer coefficient from the EA to duty [17]. In the CC loop and the CAS loop, the feedback signal is $I_{\rm charge}$ because the charger tracks the charging current. In the CV loop, the battery voltage $V_{\rm BAT}$ controls the charger's charging duty, thus the feedback signal is the battery voltage. Due to the total current limit function in the CAS loop, $I_{\rm system}$, which is the loading system's current, should be added with the charging current to form the total

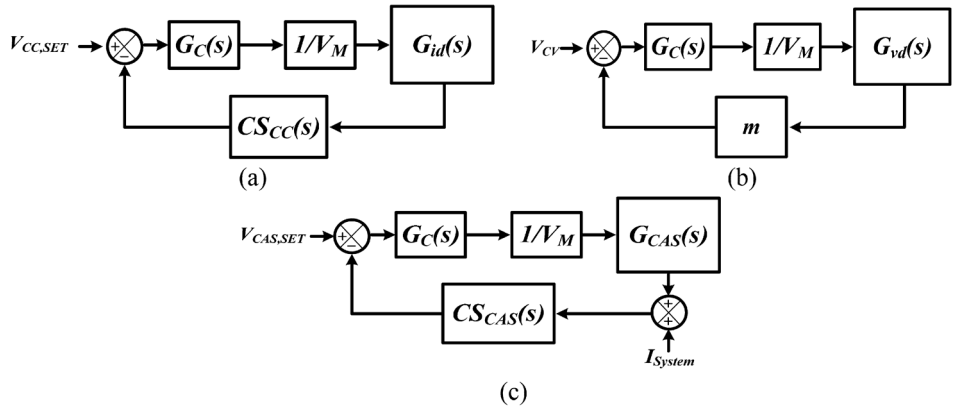


Fig. 17. Block diagram of (a) the CC loop (b) the CV loop and, (c) the CAS loop.

TABLE I
DEFINITION OF TRANSFER FUNCTIONS

Control to output transfer function	PI Compensation	Other parameters
$G_{id}(s)=\frac{V_R^*}{R_{BIR}}\times\frac{1}{\Delta(s)}$ $G_{vd}(s)=V_R^*\times\frac{1}{\Delta(s)}$ $G_{CAS}(s)=\frac{DV_R^*}{R_{BIR}}\times\frac{1}{\Delta(s)}$	$G_C(s)=\frac{A_v(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_p})}$	$V_R^*=D[V_R-(R_{MP}-R_{MN})I_L]$ $R_{eq}=R_L+DR_{MP}+(1-D)R_{MN}$ $\Delta(s)=1+\frac{R_{eq}}{R_{BIR}}+s(\frac{L}{R_{BIR}})$

input current. Different operation modes will affect the control-to-output transfer functions $G_{id}(s)$, $G_{vd}(s)$ and $G_{\rm CAS}(s)$ [12]. Combining the above parameters among the three loops in Table I, the transfer function of the three loops is obtained in (15)–(17):

$$T_{\rm CV}=mG_{\rm C}(s)\frac{1}{V_{\rm M}}G_{\nu d}(s)=\frac{mV_{\rm R}^*A_\nu(1+\frac{\rm S}{\omega_z})}{V_{\rm M}(1+\frac{\rm S}{\omega_{\rm P}})\left[1+\frac{R_{eq}}{R_{\rm BIR}}+s(\frac{L}{R_{\rm BIR}})\right]} \quad (15)$$

$$T_{\rm CC}=CS_{\rm CC}(s)G_{\rm C}(s)\frac{1}{V_{\rm M}}G_{id}(s)=\frac{V_R^*A_\nu(1+\frac{\rm S}{\omega_z})CS_{\rm CC}(s)}{R_{\rm BIR}V_{\rm M}(1+\frac{\rm S}{\omega_{\rm P}})\left[1+\frac{R_{eq}}{R_{\rm BIR}}+s(\frac{L}{R_{\rm BIR}})\right]} \quad (16)$$

$$T_{\rm CAS}=CS_{\rm CAS}(s)G_{\rm C}(s)\frac{1}{V_{\rm M}}G_{\rm CAS}(s)=\frac{DV_R^*A_\nu(1+\frac{\rm S}{\omega_z})CS_{\rm CAS}(s)}{R_{\rm BIR}V_{\rm M}(1+\frac{\rm S}{\omega_{\rm P}})\left[1+\frac{R_{eq}}{R_{\rm BIR}}+s(\frac{L}{R_{\rm BIR}})\right]}. \quad (17)$$

In (15)–(17), the charger could be simplified to the system with two poles and one zero. This approximation is made by considering that both $CS_{\rm CC}(s)$ and $CS_{\rm CAS}(s)$ will not affect the stability below the system's unit-gain frequency. Since the current sense circuit needs high bandwidth to track the inductor's current, the pole of $CS(s)$ and $CS_{\rm CAS}(s)$, appear higher than several hundred kilohertz. Hence, the unit-gain frequency of the charger is below tens of kilohertz to prevent the loop stability from being affected by the $CS(s)$. The Bode plots of the three loops are shown in Fig. 18. The PI compensator generates a zero ω_{z1} to perform pole-zero cancellation with the power stage pole $\omega_{\rm P2}$ in $\Delta(s)$. The PI compensator also adds a low-frequency dominant pole $\omega_{\rm P1}$ to ensure the charger system bandwidth can meet the specifications. $\omega_{\rm CS}$ and $\omega_{\rm CSCAS}$ are the poles of $CS(s)$ and $CS_{\rm CAS}(s)$, respectively. As a result, the charger system acts like a one-pole system among all loops and thus the stability is guaranteed. $T_{\rm CV}$, $T_{\rm CC}$ and $T_{\rm CAS}$ have the same phase margin since poles and zero are nearly at the same positions in three loops.

With the addition of the CBIRD function, the charger system generates a feed-forward path to compensate the $V_{\rm CV}$. $V_{\rm CV,COMP}$ acts as an external threshold voltage to determine transition timing in the charging status. Once $V_{\rm FB}$ reaches $V_{\rm CV,COMP}$, the charger enters CV mode from CC mode. It is obvious that $V_{\rm CV,COMP}$ has no effect on the stability of the CC and the CAS loops. However, when the charger operates in CV mode, $V_{\rm CV,COMP}$ becomes the reference voltage of the feedback loop. The feedback loop controls the charging current according to $V_{\rm CV,COMP}$. In the meanwhile, $V_{\rm CV,COMP}$ is related to the charging current. Thus, in the following analysis, the modeling is focused on the effect of CBIRD in the CV loop. The block diagram with the CBIRD is modeled in Fig. 19. The differentiator performs differential function with a constant circuit coefficient K. The S/H subtractor circuit simply performs the subtraction of two sampling values. The coefficient of the S/H subtractor can be defined as one. The AMDU multiplies and divides the input signal by $V_{\rm CS}$ and V_R, respectively, so that the coefficient of AMDU is defined as $V_{\rm CS}/V_R$. m is the

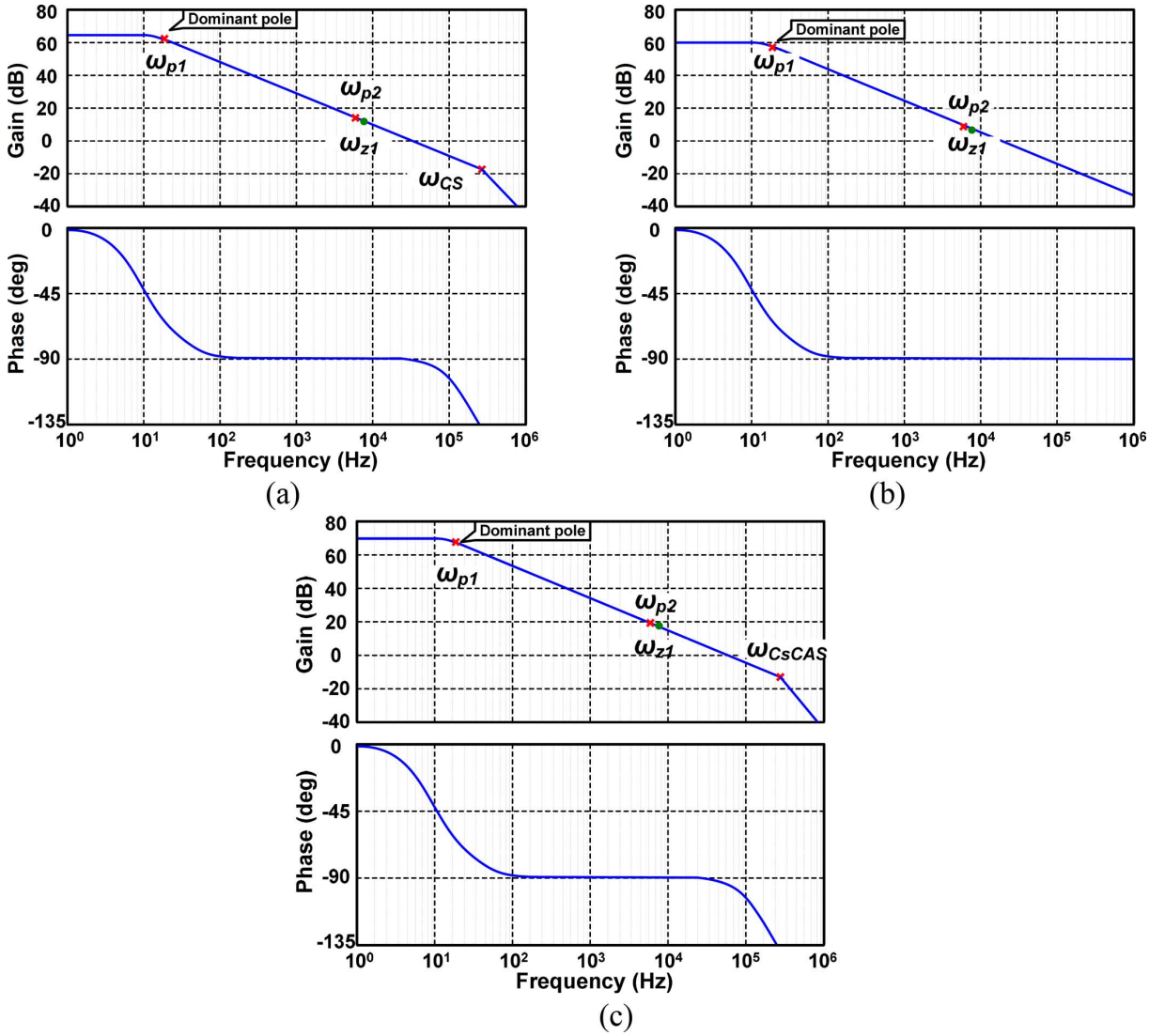


Fig. 18. Bode plots of (a) the CC loop, (b) the CV loop, and (c) the CAS loop.

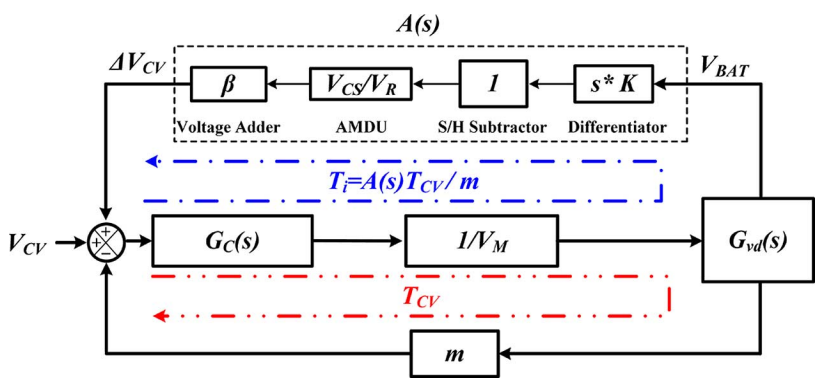


Fig. 19. Block diagram of the CV loop with the CBIRD.

ratio of the feedback resistor, which is 0.5 in this design. β is the coefficient of the voltage adder as mentioned in (14).

The transfer function of CBIRD T_i seems like a positive feedback in Fig. 19. In CC and CAS modes, the charging current is set to a certain value and regulated by the CC and the CAS loops. The compensated $V_{\mathrm{CV,COMP}}$ generated through CBIRD will not affect the charging current. In other words, CBIRD will not affect the loop stability in CC and CAS modes. However, in CV mode, $V_{\mathrm{CV,COMP}}$ is used as the reference voltage to generate the switching charger's duty. This makes $V_{\mathrm{CV,COMP}}$ relate to charging current. As the charger enters CV mode, the charging current reduces and lowers the current sense signal V_{CS}. Lower V_{CS} further reduces $V_{\mathrm{CV,COMP}}$. The drop of $V_{\mathrm{CV,COMP}}$ will result in another current drop. The above operation of CBIRD in

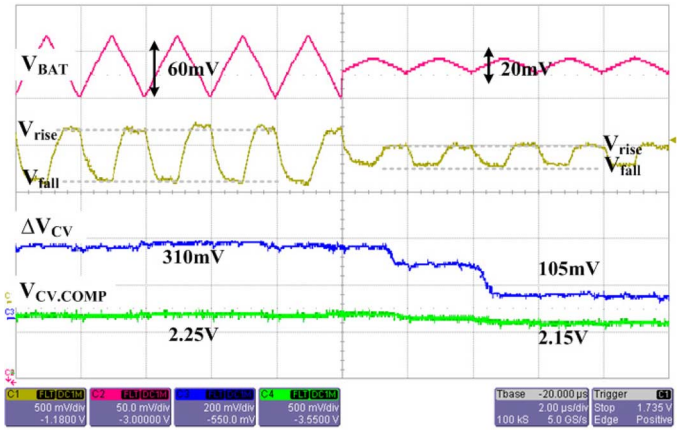


Fig. 20. Measurement results of the CBIRD circuit.

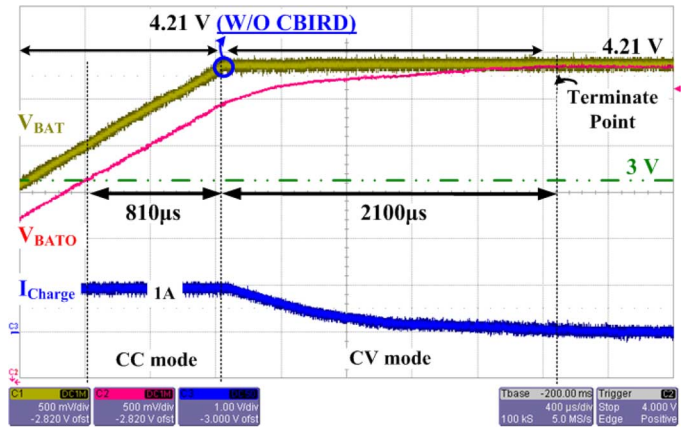


Fig. 21. Charging process during CC mode and CV mode without the BIR compensation.

CV mode will lead the compensated voltage $\Delta V_{\rm CV}$ convergent to zero. Thus, $V_{\rm CV,COMP}$ will equal to the original reference voltage $V_{\rm CV}$. T_i loop will not affect the stability of the CV loop and the transfer function is the same as that of the CV loop even with the CBIRD circuit. The charger system still behaves as a one-pole system under the designed bandwidth. The system's frequency response is not influenced in all loops with the additional CBIRD function.

V. Experimental Results

To verify the CBIRD circuit, a test signal which emulates the voltage ripple is used as the input voltage $V_{\rm BAT}$, as shown in Fig. 20. The voltage ripple is about 20 mV when the rated charging current is 2 A and the BIR is equal to 100 mΩ. Likewise, the voltage ripple is 60 mV when the BIR is 300 mΩ. According to (14), the $\Delta V_{\rm CV}$ should be 100 mV and 300 mV, because the feedback resistor ratio m is 0.5. In the measurement results, the values of $\Delta V_{\rm CV}$ are 105 mV and 310 mV, respectively. Thus, the actual values for $V_{\rm CV,COMP}$ are 2.25 V and 2.15 V, respectively, when $V_{\rm CV}$ is 2.1 V. The error percentage of the $V_{\rm CV,COMP}$ is less than 0.5%.

In the following measurements, the supply voltage of the charger V_R is 5 V. The rated voltage of the battery is designed as 4.2 V. Thus, in case of the fully charged voltage in CV mode, the original voltage reference $V_{\rm CV}$ is near 2.1 V. The switching frequency of the charger is 500 kHz and the inductor is 10 μH. In this work, the proposed charger has an external pin *CBIRD_EN* to control the CBIRD circuit as shown in Fig. 4. To emulate the battery pack, 350 mΩ resistor and 1000 μF capacitor are used to represent the BIR and the battery capacity, respectively. The selection of a small emulation capacitor can observe the whole charging process within a short time to verify the proposed function. Fig. 21 illustrates the conventional charging process without the proposed CBIRD technique. The charging current in CC mode is set to be 1 A and the full voltage is 4.2 V. The STLS circuit ensures the loop stability between the transitions of two modes. However, it is too early to transit from CC mode to CV mode in the control of the charger owing to the BIR effect. Consequently, the charging time is prolonged due to the shorten period of CC mode. As shown in Fig. 21, the charger transit from CC mode to CV mode when $V_{\rm BAT}$ reaches

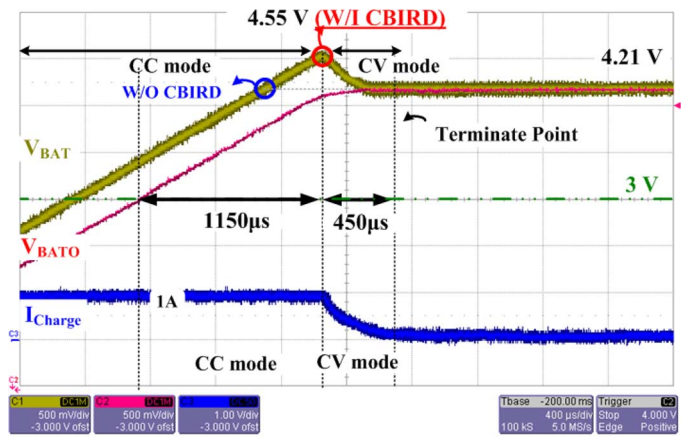


Fig. 22. Charging process with the proposed CBIRD in CC and CV modes.

the rated voltage 4.2 V. The real voltage of battery $V_{\rm BATO}$ is not fully charged so that the charger continuously delivers energy to the battery with a decreasing charging current in CV mode. The charger takes 2100 μs in CV mode until the charging process terminates.

On the other hand, Fig. 22 shows the charging process with the CBIRD function. The measurement environment is the same as that in Fig. 21. Due to the CBIRD technique, the transition point of CV mode is modified from 4.21 V to 4.55 V. Therefore, the operation period in CC mode is extended by nearly 350 μs. In other words, the BIR effect is compensated by the CBIRD technique. Compared to the result of conventional charger in Fig. 21, the proposed charger could reduce the charging time of 1300 μs. In the measurement results, the emulated capacitor charges from 0 V. However, in practical applications, the lower bound of the Li-ion battery voltage is often set at 3 V to protect the battery from being overdischarged. The charging time in CC mode from 3 V to 4.2 V is approximately 800 μs and 1150 μs without and with the proposed CBIRD technique, respectively. That is to say, the proposed charger reduces the total charging time from 2900 μs to 1600 μs . The charging time is saved by 44.8%. With the proposed CBIRD method, the charging time of a real Li-ion battery can get an improvement of 40%. This difference between 44.8% and 40% is due to the thermal effect, which decreases the BIR value, when the battery temperature

TABLE II
CHIP SPECIFICATIONS

Technology	VIS 0.25μm
Input Voltage (V_R)	4.5V ~ 5.5V
Charge Voltage	2.1V ~ 4.2V
Charge Current	500mA ~ 2A
Filter Inductor (L)	10μH
Switching Frequency (f_{SW})	500KHZ

TABLE III
COMPARISON TABLE

	TCAS II [2]	TCAS I [6]	JSSC [12]	This Work
Technology	N/A	TSMC 0.35μm	TSMC 0.18μm	VIS 0.25μm
Charger Type	LDO	LDO	Switching-based	Switching-based
Battery Type	Li-Ion	Li-Ion	Li-Ion	Li-Ion
Efficiency	83%	N/A	86%	82%@ 2A 87%@ 1A
BIR detector method	N/A	Built-in Resistor Compensator	N/A	CBIRD
Charging Time saved	N/A	40% CC time extension	N/A	40%
Maximum Charging Current	800mA	500mA	900mA	2A
Output Range	N/A	2.1V~4.2V	2.1V-4.2V	2.1V-4.2V
Switching Frequency	None	None	2.2MHz	500KHZ
Die size	N/A	1.1mm^2	1.6mm^2	3mm^2

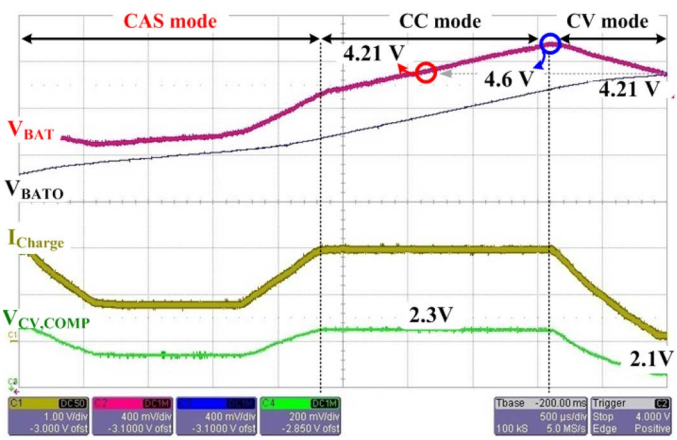


Fig. 23. Charging process with the AEDC during different operation modes.

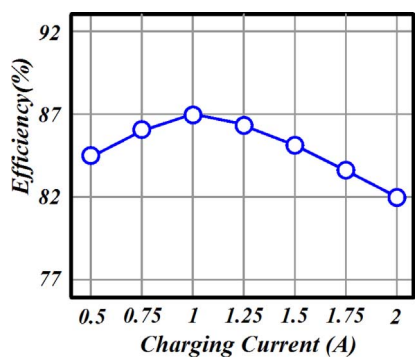


Fig. 24. Power efficiency of the proposed charger circuit.

increases during the charging process. Some measurement conditions such as the definition of ending charging voltage and current also slightly affect the measured results.

Fig. 23 shows the measurement results of the whole charging process including CC, CV, and CAS modes in the AEDC. The default charging current in CC mode is set to 2 A. Equivalent BIR resistance of 200 mΩ and equivalent capacitance of 5000 μF are used to emulate the charging status of Li-ion battery. In CAS mode, the charging current $I_{\rm charge}$ varies with the loading system's power requirement. Besides, the compensation signal $V_{\rm CV,COMP}$ is changed according to the variation of $I_{\rm charge}$. $I_{\rm charge}$ sustains at 2 A when the charger system operates in CC mode. Hence, in Fig. 23 the function of CBIRD can be proved. The transition point $V_{\rm CV,COMP}$ is compensated by the CBIRD from 4.21 V to 4.6 V. It shows that the CBIRD technique continuously calculates the BIR value under various charging conditions. The power efficiency of the proposed charger is shown in Fig. 24. The peak efficiency 87% appears at 1 A of charging current and 82% of efficiency can be achieved at the rated charging current 2 A.

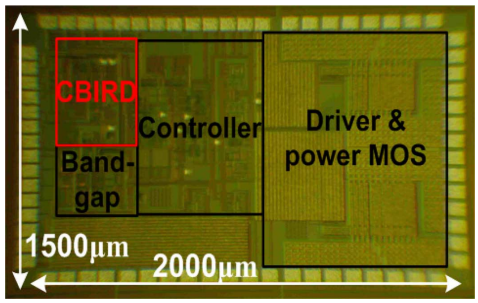


Fig. 25. Chip micrograph of the proposed switching-based charger with the CBIRD.

Overall operation specifications of the charger system are listed in Table II. The chip micrograph is shown in Fig. 25. The proposed charger system with the AEDC and the CBIRD circuit was fabricated in VIS 0.25 μm CMOS technology with an active area of 2000×1500 μm^2. Compared to prior arts [2], [6], and [12], the comparison in Table III shows the improvements in specifications.

VI. Conclusion

In this paper, a switching-based charger system with the AEDC function and the BIR compensation technique has been proposed. The AEDC mechanism can automatically decide an optimal power path based on the power requirements of the system. Furthermore, the AEDC smartly regulates the charging current according to the limitation of input power as the experimental results demonstrate. Moreover, since the effect of BIR varies from the charging current and temperature, the proposed CBIRD provides a real-time BIR detection to avoid over or under compensation in the transition voltage and to extend the charging time in CC mode. The test chip was fabricated in 0.25 μm CMOS process and occupied 3 mm^2 silicon area. Peak power efficiency of 87% and 40% charging time saving are achieved in this work.

References

[1] V. Pop, H. J. Bergveld, D. Danilov, P. P. L. Regtien, and P. H. L. Notten, *Battery Management System*. New York, NY, USA: Springer, 2008, ch. 1.

[2] M. Chen and G. A. Rincon-Mora, "Accurate, compact, and power-efficient Li-ion battery charger circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1180–1184, Nov. 2006.

[3] C.-C. Tsai, C.-Y. Lin, Y.-S. Hwang, W.-T. Lee, and T.-Y. Lee, "A multi-mode LDO-based Li-ion battery charger in 0.35 μm CMOS technology," in *Proc. 2004 IEEE Asia-Pacific Conf. Circuits and Systems*, Dec. 2004, pp. 49–52.

[4] S.-H. Yang, J.-W. Liu, and C.-C. Wang, "A single-chip 60-V bulk charger for series Li-ion batteries with smooth charge mode transition," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 7, pp. 1588–1597, Jul. 2012.

[5] B. D. Valle, C. T. Wentz, and R. Sarpeshkar, "An area and power-efficient analog Li-ion battery charger circuit," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 2, pp. 131–137, Apr. 2011.

[6] C.-H. Lin, C.-Y. Hsieh, and K.-H. Chen, "A Li-ion battery charger with smooth control circuit and built-in resistance compensator for achieving stable and fast charging," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 2, pp. 506–517, Feb. 2010.

[7] C.-H. Lin, C.-L. Chen, Y.-H. Lee, S.-J. Wang, C.-Y. Hsieh, H.-W. Huang, and K.-H. Chen, "Fast charging technique for Li-ion battery charger," in *Proc. 2008 IEEE Int. Conf. Electronics, Circuits and Systems*, Sep. 2008, pp. 618–621.

[8] C.-H. Lin, H.-W. Huang, and K.-H. Chen, "Built-in resistance compensation technique for fast charging Li-ion battery charger," in *Proc. 2008 IEEE Custom Integrated Circuits Conf., CICC*, Sep. 2008, pp. 33–36.

[9] R.-H. Peng, T.-W. Tsai, K.-H. Chen, Z.-H. Tai, Y.-H. Cheng, C.-C. Tsai, H.-Y. Luo, S.-M. Wang, L.-D. Chen, C.-C. Yang, and J.-L. Chen, "Switching-based charger with continuously built-in resistor detector (CBIRD) and analog multiplication-division unit (AMDU) for fast charging in Li-ion battery," in *Proc. 2013 Eur. Solid-State Circuits Conf., ESSCIRC*, Sep. 2013, pp. 157–160.

[10] R.-H. Peng, Y.-P. Su, T.-W. Tsai, Y.-P. Chen, K.-H. Chen, M.-J. Du, and S.-H. Cheng, "Robust switch-mode charger with bootstrap detector (BSD) and soft-start embedded in type III compensation (SSEC) technique," in *Proc. 2008 IEEE Energy Conversion Congress and Exposition*, Sep. 2008, pp. 33–36.

[11] F.-C. Yang, C.-C. Chen, J.-J. Chen, Y.-S. Hwang, and W.-T. Lee, "Hysteresis-current-controlled buck converter suitable for Li-ion battery charger," in *Proc. 2006 IEEE Int. Conf. Communications, Circuits and Systems*, Jun. 2006, vol. 4, pp. 2723–2726.

[12] R. Pagano and M. Baker, "A 0.18-μm monolithic Li-ion battery charger for wireless devices based on partial current sensing and adaptive reference voltage," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1355–1368, Jun. 2012.

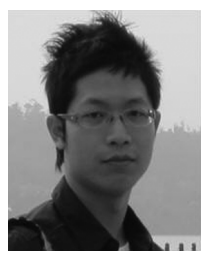
[13] Linear Technology, "Standalone linear Li-ion battery charger and dual synchronous buck converter," 2006 [Online]. Available: http://cds.linear.com/docs/en/datasheet/3552f.pdf

[14] Texas Instruments, "Lithium ion charge management IC with integrated switching controller," 2010 [Online]. Available: http://focus.ti.com/lit/ds/symlink/bq2954.pdf

[15] D. Linden and T. B. Reddy, *Handbook of Batteries*. New York, NY, USA: McGraw-Hill, 2002, ch. 35.

[16] R. Saint-Pierre, "A dynamic voltage-compensation technique for reducing charge time in Li-ion batteries," in *Proc. 15th Annual Battery Conf. Applications and Advances*, Jan. 2000, pp. 179–184.

[17] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA, USA: Kluwer, 2001.



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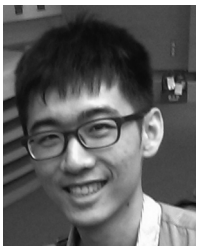

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